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EEPROM  
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EEPROM  
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DATA  
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EEPROMS

HIGH  
SPEED  
EEPROM

THE  
FUTURE

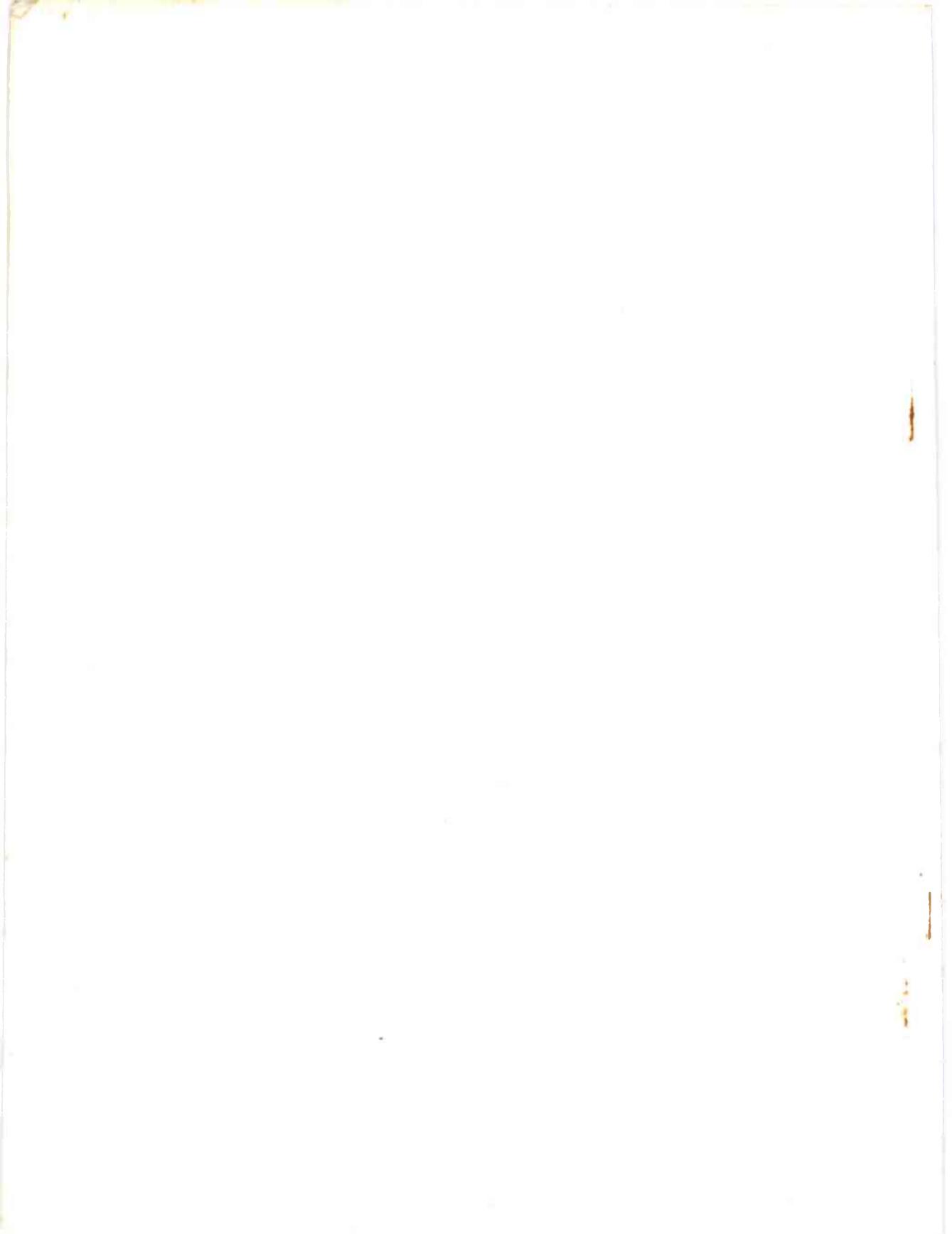
CMOS  
EEPROM

EEPROM  
PLD

### DATA BOOK

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# seeq

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## EPROMS

### EPROMS (Erasable Programmable Read Only Memories)

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# DATA BOOK

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SEEQ is your link to the future.

New products utilizing our highly advanced 1.25 micron CMOS technology continue to expand our existing EEPROM, EPROM, and data communications product offerings. As the acknowledged thin film EEPROM technology leader, SEEQ is continuing to develop advanced technologies to help solve your future system challenges.

SEEQ's clustered product strategy, as shown on the cover, utilizes our EE technology to tie together a group of focused system solutions, high density EEPROMS and EPROMS, high speed EEPROMS, EEPROM micro computers, and more. Each of these focused areas utilize our base memory technology, as well as various versions of our proprietary Q cell memory design.

SEEQ's unique EEPROM cell design, which we call our Q cell, complements our proprietary oxynitride process technology to give you the most reliable EEPROM's available from any manufacturer. Our 5516A (2K x 8 EEPROM) has an endurance failure rate of  $\leq .001\%$  per 1,000 cycles and is guaranteed for a minimum of 1 million write/erase cycles. (Intrinsic MOS has a failure rate of .05 percent per 1000 hours.)

Packaging of our products includes standard dual in-line packages and a variety of surface mount options. SEEQ products may be ordered in plastic, ceramic dip, LCC, PLCC, flatpack or if you wish, unencapsulated die.

Let SEEQ be your link to the future. Call us today for your design solution.

A handwritten signature in black ink, appearing to read 'Mike Villott'.

Mike Villott  
V.P. Marketing



**Product Previews** contain information on products under development. These specifications may be changed at any time, without notice.

**Advance Data Sheets** contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

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San Jose, CA 95131

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# SEEQ Technology

## Product Selection Guide

### 4K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #	
			ACTIVE	STANDBY		P	D	N	L	F		
2804A	512 x 8	250	80	40	C,E,M	•	•					1-31
2804A	512 x 8	300	80	40	C,E,M	•	•					1-31
2804A	512 x 8	350	80	40	C,E,M	•	•					1-31

### 16K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #	
			ACTIVE	STANDBY		P	D	N	L	F		
52B13	2K x 8	200	80	30	C	•	•					1-3
52B13	2K x 8	250	80	30	C, E, M	•	•					1-3
52B13	2K x 8	300	80	30	M	•	•					1-3
52B13	2K x 8	350	80	30	C, E	•	•					1-3
2816A	2K x 8	200	110	40	C	•	•					1-19
2816A	2K x 8	250	110	40	C, E, M	•	•					1-19
2816A	2K x 8	300	110	40	C, E, M	•	•					1-19
2816A	2K x 8	350	110	40	C	•	•					1-19
5516A	2K x 8	200	110	40	C		•					1-19
5516A	2K x 8	250	110	40	C		•					1-19
5516A	2K x 8	300	110	40	C		•					1-19
2817A	2K x 8	200	110	40	C	•	•					1-25
2817A	2K x 8	250	110	40	C, E, M	•	•					1-25
2817A	2K x 8	300	110	40	C, E, M	•	•					1-25
2817A	2K x 8	350	110	40	C	•	•					1-25
5517A	2K x 8	250	110	40	C		•					1-25
5517A	2K x 8	300	110	40	C		•					1-25

### TEMPERATURE RANGE

C = Commercial 0°C to +70°C  
 E = Extended -40°C to +85°C  
 M = Military -55°C to +125°C

TBD = To Be Determined

\*Commercial Temperature Range

### PACKAGE

P = Plastic  
 D = Cerdip  
 N = Plastic Leaded Chip Carrier  
 L = Ceramic Leadless Chip Carrier  
 F = Flat Pack

## 64K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #	
			ACTIVE	STANDBY		P	D	N	L	F		
52B33	8K x 8	200	110	40	C	•	•					1-11
52B33	8K x 8	250	110	40	C, E, M	•	•		•			1-11
52B33	8K x 8	300	110	40	C, E, M	•	•		•			1-11
52B33	8K x 8	350	110	40	C	•	•					1-11
2864	8K x 8	250	110	40	C, E, M	•	•	•	•	•		1-37
2864	8K x 8	300	110	40	C, E, M	•	•	•	•	•		1-37
2864	8K x 8	350	110	40	C, E, M	•	•	•	•	•		1-37
28C64	8K x 8	250	50	.150	C, E, M	•	•	•	•			1-43
28C64	8K x 8	300	50	.150	C, E, M	•	•	•	•			1-43
28C64	8K x 8	350	50	.150	C, E, M	•	•	•	•			1-43
28C65	8K x 8	250	50	.150	C, E, M	•	•	•	•			1-51
28C65	8K x 8	300	50	.150	C, E, M	•	•	•	•			1-51
28C65	8K x 8	350	50	.150	C, E, M	•	•	•	•			1-51

## 256K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #	
			ACTIVE	STANDBY		P	D	N	L	F		
28C256	32K x 8	250	60	.150	C,E,M		•	•	•	•		1-59
28C256	32K x 8	300	60	.150	C,E,M		•	•	•	•		1-59
28C256	32K x 8	350	60	.150	C,E,M		•	•	•	•		1-59

## FLASH™ EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE					DATA SHEET PAGE #	
			ACTIVE	STANDBY		P	D	N	L	F		
48128	16K x 8	170	100	30	C	•	•	•				1-81
48128	16K x 8	200	100	30	C	•	•	•				1-81
48128	16K x 8	250	100	30	C	•	•	•				1-81
48128	16K x 8	300	100	30	C	•	•	•				1-81
48C512	64K x 8	200	TBD	TBD	C		•	•	•			1-93
48C1024	128K x 8	200	TBD	TBD	C		•	•	•			1-93

## TEMPERATURE RANGE

C = Commercial 0°C to +70°C  
 E = Extended -40°C to +85°C  
 M = Military -55°C to +125°C

TBD = To Be Determined

\*Commercial Temperature Range

## PACKAGE

P = Plastic  
 D = Cerdip  
 N = Plastic Leaded Chip Carrier  
 L = Ceramic Leadless Chip Carrier  
 F = Flat Pack

## HIGH SPEED 16K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE				DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	
36C16	2K x 8	35	100	—	C	•				1-67
36C16	2K x 8	45	100	—	C	•				1-67
36C16	2K x 8	55	100	—	C, E, M	•				1-67
36C16	2K x 8	70	100	—	E, M	•				1-67
38C16	2K x 8	35	100	60	C	•				1-75
38C16	2K x 8	45	100	60	C	•				1-75
38C16	2K x 8	55	100	60	C, E, M	•				1-75
38C16	2K x 8	70	100	60	E, M	•				1-75

## HIGH SPEED 32K EEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE				DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	
36C32	4K x 8	35	100	—	C	•				1-67
36C32	4K x 8	45	100	—	C	•				1-67
36C32	4K x 8	55	100	—	C,E,M	•				1-67
36C32	4K x 8	70	100	—	E,M	•				1-67
38C32	4K x 8	35	100	60	C	•				1-75
38C32	4K x 8	45	100	60	C	•				1-75
38C32	4K x 8	55	100	60	C,E,M	•				1-75
38C32	4K x 8	70	100	60	E,M	•				1-75

## 64K/128K/256K UVEPROMS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ORGANIZATION	ACCESS TIME(ns)	ICC MAX. (mA*)		TEMP RANGE	PACKAGE				DATA SHEET PAGE #
			ACTIVE	STANDBY		P	D	N	L	
2764	8K x 8	160	100	30	C	•				2-3
2764	8K x 8	200	100	30	C,E,M	•				2-3
2764	8K x 8	250	100	30	C,E,M	•				2-3
2764	8K x 8	300	100	30	C	•				2-3
2764	8K x 8	350	100	30	E,M	•				2-3
2764	8K x 8	450	100	30	C,M	•				2-3
27128	16K x 8	200	100	30	C,E,M	•				2-3
27128	16K x 8	250	100	30	C,E,M	•				2-3
27128	16K x 8	300	100	30	C	•				2-3
27128	16K x 8	350	100	30	E,M	•				2-3
27128	16K x 8	450	100	30	C	•				2-3
27C256	32K x 8	200	50	.150	C	•				2-11
27C256	32K x 8	250	50	.150	C,E,M	•	•			2-11
27C256	32K x 8	300	50	.150	C,E,M	•	•			2-11
27C256	32K x 8	450	50	.150	C	•				2-11

## COMMUNICATION PRODUCTS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	ICC MAX. ACTIVE (mA*)	TEMP RANGE	PACKAGE					FUNCTION	DATA SHEET PAGE #
			P	D	N	L	F		
8003	200	C		•				Data Link Controller	3-25
8020	100	C	•	•	•			10 MHz Manchester Encoder/Decoder	3-37
8023A	100	C	•	•	•			10 MHz Manchester Encoder/Decoder	3-51
8005	300	C			•			Advanced Data Link Controller	3-67

## EEPROM MICROPROCESSORS

(See Military Section for Military and Extended Temperature Range Products.)

PART NUMBER	CLOCK RATE (MHz)	EEPROM SIZE	ICC MAX. ACTIVE (mA*)	TEMP RANGE	PACKAGE					DATA SHEET PAGE #
					P	D	N	L	F	
72720-10	10	2K x 8	150	C	•	•				3-1
72720-16	16	2K x 8	150	C	•	•				3-1

### TEMPERATURE RANGE

C = Commercial 0°C to +70°C  
 E = Extended -40°C to +85°C  
 M = Military -55°C to +125°C

TBD = To Be Determined

\*Commercial Temperature Range

### PACKAGE

P = Plastic  
 D = Ceramic Dip  
 N = Plastic Leaded Chip Carrier  
 L = Ceramic Leadless Chip Carrier  
 F = Flat Pack

# 1

## ***EEPROMS***

(Electrically Erasable Programmable Read Only Memories)



## SEEQ Technology EEPROM Alternate Source

<b>MFG.</b>	<b>Part No.</b>	<b>Description</b>	<b>SEEQ Part No.</b>
A.M.D.	2817A	2K X 8 EEPROM	2817A
A.M.D.	9864	8K X 8 EEPROM	2864
A.M.D.	2864B	8K X 8 EEPROM	28C64
ATMEL	28C64	8K X 8 EEPROM	28C64
EXEL	2804A	512 X 8 EEPROM	2804A
EXEL	46C16-55	2K X 8 EEPROM	36C16-55
EXEL	2816A	2K X 8 EEPROM	2816A
EXEL	2864	8K X 8 EEPROM	28C64
EXEL	2865	8K X 8 EEPROM	28C65
FUJITSU	28C64	8K X 8 EEPROM	28C64
FUJITSU	28C65	8K X 8 EEPROM	28C65
G.I.	28C64	8K X 8 EEPROM	28C64
HITACHI	58064	8K X 8 EEPROM	52B33
INTEL	2816	2K X 8 EEPROM	52B13
INTEL	2816A	2K X 8 EEPROM	52B13
INTEL	2817A	2K X 8 EEPROM	2817A
NATIONAL	9816A	2K X 8 EEPROM	2816A
NATIONAL	9817A	2K X 8 EEPROM	2817A
SAMSUNG	2816A	2K X 8 EEPROM	2816A
SAMSUNG	2817A	2K X 8 EEPROM	2817A
XICOR	2616	2K X 8 EEPROM	36C16-45
XICOR	2816H	2K X 8 EEPROM	38C16-45
XICOR	2804A	512 X 8 EEPROM	2804A
XICOR	2816A	2K X 8 EEPROM	2816A
XICOR	2864A	8K X 8 EEPROM	28C64
XICOR	2864B	8K X 8 EEPROM	28C64
XICOR	28256	32K X 8 EEPROM	28C256

# SEEQ Technology PROM Replacement Chart

MFG.	Part No.	Description	SEEQ Part No.
A.M.D.	AM27PS291DC	2K X 8 PROM	36C16-45
A.M.D.	AM27PS291DM	2K X 8 PROM	36C16-55
A.M.D.	AM27PS291ADM	2K X 8 PROM	36C16-55
A.M.D.	AM27S291ADC	2K X 8 PROM	36C16-35
CYPRESS	CY7C291-35	2K X 8 PROM	36C16-35
CYPRESS	CY7C291-50	2K X 8 PROM	36C16-45
FUJITSU	MB7138Y-SKZ	2K X 8 PROM	36C16-35
FUJITSU	MB7138H-SKZ	2K X 8 PROM	36C16-45
FUJITSU	MB7138E-WZ	2K X 8 PROM	36C16-45
HARRIS	6-76161	2K X 8 PROM	36C16-45
M.M.I.	63S1681NS	2K X 8 PROM	36C16-45
M.M.I.	63S1681ANS	2K X 8 PROM	36C16-35
NATIONAL	DM77S291	2K X 8 PROM	36C16-55
NATIONAL	DM87S291	2K X 8 PROM	36C16-55
RAYTHEON	29681ASM	2K X 8 PROM	36C16-55
RAYTHEON	29681ASC	2K X 8 PROM	36C16-55
RAYTHEON	29681SC	2K X 8 PROM	36C16-55
RAYTHEON	29683ASC	2K X 8 PROM	36C16-45
RAYTHEON	29683ASM	2K X 8 PROM	36C16-55
SIGNETICS	82S291	2K X 8 PROM	36C16-45
T.I.	27C291-35	2K X 8 PROM	36C16-45
T.I.	27C291-50	2K X 8 PROM	36C16-45
T.I.	TBP28S166N	2K X 8 PROM	36C16-45
WAFRSCAL	57C291-40	2K X 8 PROM	36C16-35
WAFRSCAL	57C291-55	2K X 8 PROM	36C16-55
NATIONAL	DM87S421	4K X 8 PROM	36C32-55
NATIONAL	DM87S421A	4K X 8 PROM	36C32-45
NATIONAL	DM77S421	4K X 8 PROM	36C32-55
NATIONAL	DM77S421A	4K X 8 PROM	36C32-55
RAYTHEON	29671ASC	4K X 8 PROM	36C32-45
RAYTHEON	29671ASM	4K X 8 PROM	36C32-55
RAYTHEON	29673SC	4K X 8 PROM	36C32-55
RAYTHEON	29673SM	4K X 8 PROM	36C32-55

#### Features

- Input Latches
- TTL Byte Erase/Byte Write
- 1 ms (52B13H) or 9 ms Byte Erase/Byte Write
- Power Up/Down Protection
- 10,000 Erase/Write Cycles per Byte Minimum
- 5V ± 10% Operation
- Fast Read Access Time — 200 ns
- Infinite Number of Read Cycles
- Chip Erase and Byte Erase
- DiTrace™
- JEDEC Approved Byte Wide Memory Pinout
- Military And Extended Temperature Range Available

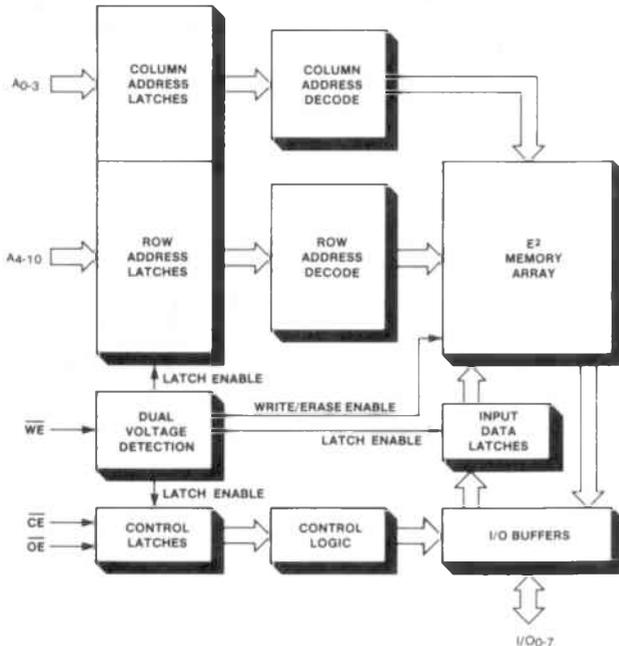
#### Description

SEEQ's 52B13 and 52B13H are 2048 x 8 bit, 5 volt electrically erasable programmable read only memories (EEPROM) with input latches on all address, data and control (chip and output enable) lines. Data is latched and electrically written by either a TTL or a 21 V pulse on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written a minimum of 10,000 times. They are direct pin-for-pin replacement for SEEQ's 52B13.

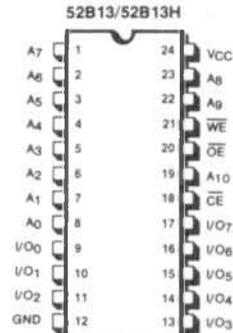
The 52B13 and 52B13H are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications for the 52B13 and 52B13H will be found in military avionics systems, programmable character generators, self-calibrating instruments/

(continued on next page)

#### Block Diagram



#### Pin Configuration



#### Pin Names

A0-A10	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O0-7	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

# 52B13/52B13H

machines, programmable industrial controllers, and an assortment of other systems. Designing the 52B13 and 52B13H into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance. Extended temperature and military grade versions are available.

## Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1s) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation EEPROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal to be applied to  $\overline{WE}$  to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of  $\overline{WE}$ .

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycle is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to  $\overline{WE}$ , enabling the chip, and enabling the outputs. Data is available  $t_{CE}$  time after Chip Enable is applied or  $t_{AA}$  time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

## DiTrace™

SEEQ's family of EEPROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to wafer level in an extra column of EEPROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection ( $V_{CC} = 5V \pm 10\%$ )

Mode \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	I/O (9-11, 13-17)
Read <sup>1</sup>	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$
Standby <sup>1</sup>	$V_{IH}$	Don't Care	$V_{IH}$	High Z
Byte Erase <sup>2</sup>	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN} = V_{IH}$
Byte Write <sup>2</sup>	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$
Chip Erase <sup>2</sup>	$V_{IL}$	$V_{OE}$	$V_{IL}$	$D_{IN} = V_{IH}$
Write/Erase Inhibit	$V_{IH}$	Don't Care	Don't Care	High Z

### NOTES:

1.  $\overline{WE}$  may be from  $V_{IH}$  to 6V in the read and standby mode

2. We may be at  $V_{IL}$  (TTL  $\overline{WE}$  Mode) or from 15 to 21V (High Voltage  $\overline{WE}$  Mode) in the byte erase, byte write, or chip erase mode of the 52B13/52B13H.

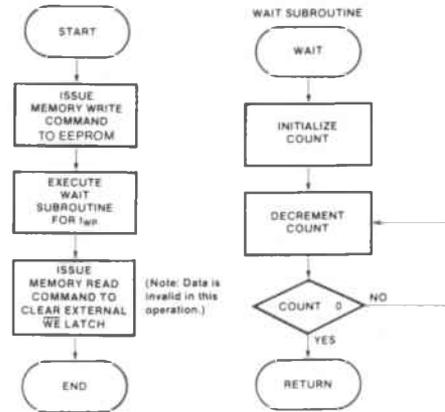
### Power Up/Down Considerations

SEEQ's "52B" E<sup>2</sup> family has internal circuitry to minimize false erase or write during system V<sub>CC</sub> power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

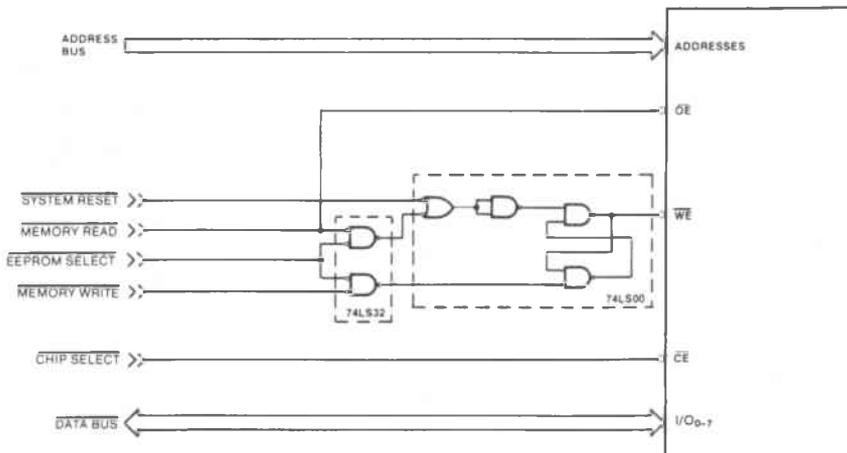
1. V<sub>CC</sub> is less than 3 V.<sup>(1)</sup>
2. A negative Write Enable transition has not occurred when V<sub>CC</sub> is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the mode selection table.

### Typical EEPROM Write/Erase Routine



### Microprocessor Interface Circuit Example for Byte Write/Erase



**NOTE:**  
1. Characterized. Not tested.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65° C to +150° C

Under Bias ..... -10° C to +80° C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

### WE During Writing/Erasing

with Respect to Ground ..... +22.5V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	52B13-200/-250/-350 52B13H-200/-250/-350
V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0° C to 70° C

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

## D.C. Operating Characteristics During Read or Write/Erase (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Min.	Nom. <sup>1</sup>	Max.	Unit	Test Conditions
I <sub>IN</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>O</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
I <sub>WE</sub>	Write Enable Leakage Read Mode			10	μA	WE = V <sub>IH</sub>
	TTL W/E Mode			10	μA	WE = V <sub>IL</sub>
	High Voltage W/E Mode			1.5	mA	WE = 22V, CE = V <sub>IL</sub>
	High Voltage W/E Inhibit Mode			1.5	mA	WE = 22V, CE = V <sub>IH</sub>
	Chip Erase — TTL Mode			10	μA	WE = V <sub>IL</sub>
I <sub>CC1</sub>	V <sub>CC</sub> Standby Current		15	30	mA	CE = V <sub>IH</sub>
			50	80	mA	CE = OE = V <sub>IL</sub>
I <sub>CC2</sub>	V <sub>CC</sub> Active Current					
V <sub>IL</sub>	Input Low Voltage	-0.1		0.8	V	
V <sub>IH</sub>	Input High Voltage	2		V <sub>CC</sub> + 1	V	
V <sub>WE</sub>	WE Read Voltage	2		V <sub>CC</sub> + 1	V	
	WE Write/Erase Voltage TTL Mode		-0.1	0.8	V	
		High Voltage Mode	14		22	V
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA
V <sub>OE</sub>	OE Chip Erase Voltage	14		22	V	I <sub>OE</sub> = 10 μA

### Notes:

1. Nominal values are for T<sub>A</sub> = 25° C and V<sub>CC</sub> = 5.0V.

## A.C. Operating Characteristics During Read (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Device Number Extension	52B13 52B13H		Unit	Test Conditions
			Min.	Max.		
$t_{AA}$	Address Access Time	-200 -250 -350		200 250 350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid	-200 -250 -350		200 250 350	ns	$\overline{OE} = V_{IL}$
$t_{OE}^{(1)}$	Output Enable to Data Valid	-200 -250 -350		80 90 100	ns	$\overline{CE} = V_{IL}$
$t_{DF}^{(2)}$	Output Enable to High Impedance	-200 -250 -350	0 0 0	60 70 80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

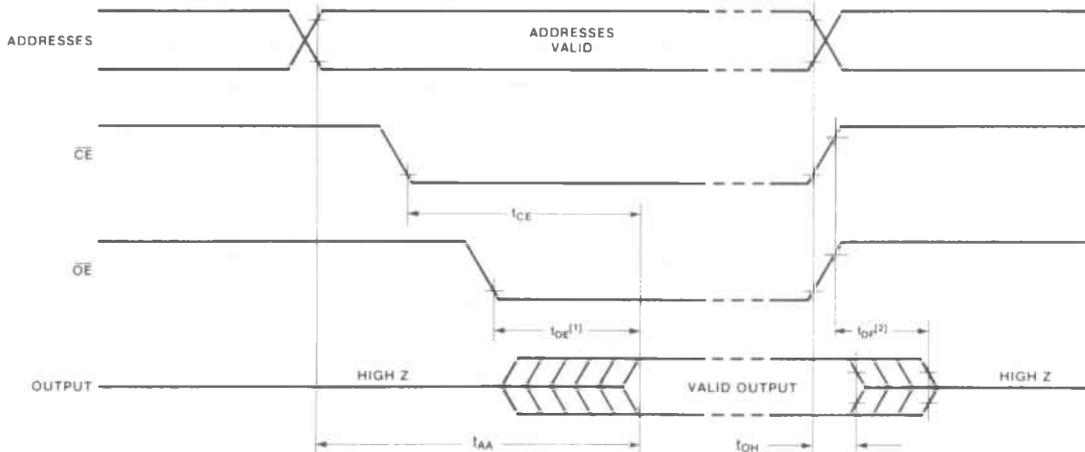
### Capacitance<sup>[3]</sup> $T_A=25^\circ\text{C}$ , $f=1\text{ MHz}$

Symbol	Parameter	Max.	Unit	Conditions
$C_{IN}$	Input Capacitance	10	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	10	pF	$V_{OUT} = 0V$
$C_{V_{CC}}$	$V_{CC}$ Capacitance	500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
$C_{V_{WE}}$	$V_{WE}$ Capacitance	10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

### A.C. Test Conditions

Output Load: 1 TTL gate and  $C_L = 100\text{ pF}$   
 Input Rise and Fall Times:  $\leq 20\text{ ns}$   
 Input Pulse Levels: 0.45V to 2.4V  
 Timing Measurement Reference Level:  
 Inputs 1V and 2V  
 Outputs 0.8V and 2V

### Read Timing



#### NOTES:

- $\overline{OE}$  may be delayed to  $t_{AA} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{AA}$ .
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
- This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.

## A.C. Operating Characteristics During Write/Erase (Over the operating $V_{CC}$ and temperature range)

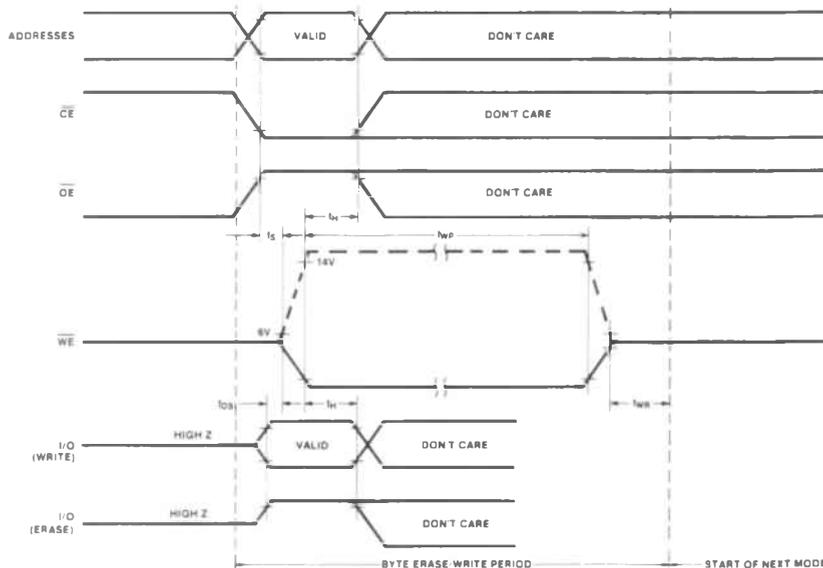
Symbol	Parameter	Min.	Max.	Units
$t_s$	$\overline{CE}$ , $\overline{OE}$ or $A_n$ Setup to $\overline{WE}$	50		ns
$t_{ds}$	Data Setup to $\overline{WE}$	15		ns
$t_w^{[1]}$	$\overline{WE}$ to $\overline{CE}$ , $\overline{OE}$ , $A_n$ or Data Change	50		ns
$t_{wp}^{[1]}$	Write Enable, $\overline{WE}$ , Pulse Width	52B13	9	ms
		52B13H	1	ms
$t_{wr}^{[2]}$	$\overline{WE}$ to Mode Change	50		ns
	$\overline{WE}$ to next Byte Write/Erase Cycle			
	$\overline{WE}$ to start of a Read Cycle		2	$\mu$ s

## 52B13/52B13H High Voltage Write Specifications

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	52B13		52B13H		Units
		Min.	Max.	Min.	Max.	
$t_{WP}$	Write Enable Pulse Width	9	20	1	10	ms
	Byte Write/Erase Chip Erase	9	20	9	20	ms
$V_{WE}$	$\overline{WE}$ Write/Erase Voltage High Voltage Mode	14	22	14	22	V

## Byte Erase or Byte Write Timing



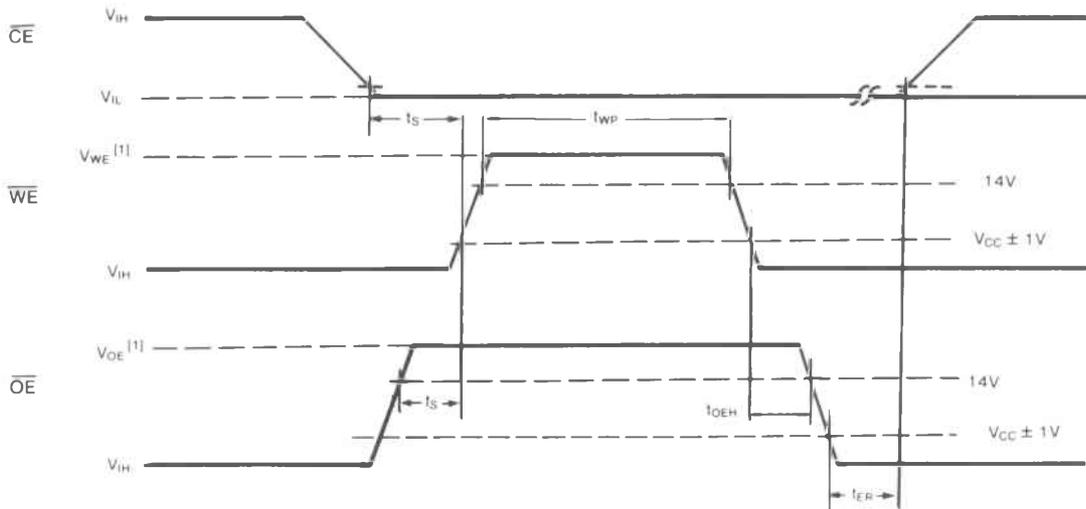
### NOTES:

- After  $t_h$ , hold time, from  $\overline{WE}$ , the inputs,  $\overline{CE}$ ,  $\overline{OE}$ , address and Data are latched and are "Don't Cares" until  $t_{wr}$ , write recovery time, after the trailing edge of  $\overline{WE}$ .
- The Write Recovery Time,  $t_{wr}$ , is the time after the trailing edge of  $\overline{WE}$  that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

## Chip Erase Specifications

Symbol	Parameter	Min.	Max.	Units
$t_s$	CE, OE Setup to WE	1		$\mu\text{s}$
$t_{OEH}$	OE Hold Time	1		$\mu\text{s}$
$t_{WP}$	WE Pulse Width	10		ms
$t_{ER}$	Erase Recovery Time		10	$\mu\text{s}$

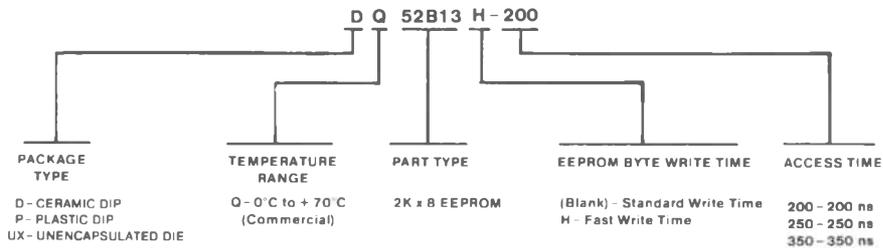
## Chip Erase Timing



### NOTES:

1.  $V_{WE}$  and  $V_{OE}$  can be from 15V to 21V in the high voltage mode for chip erase on 52B13.

## Ordering Information





## 52B33/52B33H 64K Electrically Erasable PROM

October 1987

### Features

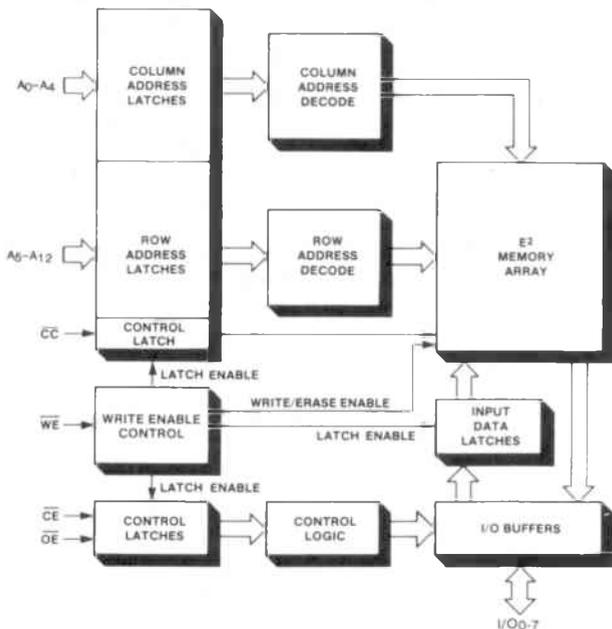
- **High Write Endurance Over Temperature Range**  
— 52B33/52B33H; 10,000 cycles/byte minimum
- **Input Latches**
- **Fast TTL Byte Write Time**  
— 1 ms for 52B33H  
— 9 ms for 52B33
- **5 V ± 10% V<sub>CC</sub>**
- **Power Up/Down Protection**
- **200 ns Read Access Time**
- **DiTrace™**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **Military And Extended Temperature Range Available**

### Description

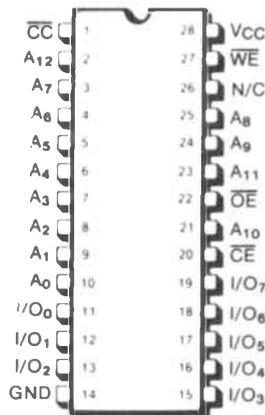
SEEQ's 52B33 is a 8192 x 8 bit, 5 volt electrically erasable programmable read only memory (EEPROM) which is specified over a 0°C to 70°C temperature range. Data retention is specified to be greater than 10 years. The device has input latches on all addresses, data, and control (chip and output) lines. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written there is no limit to the number of times data may be read. The erase time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times. For applications requiring a faster byte write or erase time, a 52B33H is available at 1 ms, giving a 10 times speed increase.

(continued on next page)

### Block Diagram



### Pin Configuration



### Pin Names

A0-A4	ADDRESSES - COLUMN (LOWER ORDER BITS)
A5-A12	ADDRESSES - ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O0-7	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
CC	CHIP CLEAR
N/C	NO CONNECT

The pin configuration is to the JEDEC approved byte wide memory pinout. EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by EEPROMs. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into these systems is simplified because of the fast access time and input latches. The specified 200 ns access time eliminates or reduces the number of microprocessor wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

## Device Operation

SEEQ's 52B33 has six modes of operation (see Table 1) and requires only TTL inputs to operate these modes. The "H" members of the family operate in the same manner as the other devices except that a faster write enable pulse width of 1 ms is specified during byte erase or write.

### Read

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{CE}$  is brought to a TTL low in order to enable the chip. The write enable ( $\overline{WE}$ ) pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ( $\overline{OE}$ ) to a TTL low. During read, the address,  $\overline{CE}$ ,  $\overline{OE}$ , and I/O latches are transparent.

### Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub> = V <sub>IH</sub>
Byte Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Chip Clear	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub> or V <sub>IH</sub>
Write/Erase Inhibit	V <sub>IH</sub>	Don't Care	Don't Care	Don't Care	High Z

#### NOTE:

1. Characterized. Not tested.

### Write

To write in to a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs and I/O lines. All inputs can be released after the write enable hold time ( $t_H$ ) and the next input conditions can be established while the byte is being erased. During this operation, the write enable must be held at a TTL low for 9 ms ( $t_{WP}$ ). A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the 52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

### Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

### DiTrace™

SEEQ's family of EEPROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

### Power Up/Down Considerations

SEEQ's "52B" E<sup>2</sup> family has internal circuitry to minimize false erase or write during system V<sub>CC</sub> power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. V<sub>CC</sub> is less than 3 V.<sup>(1)</sup>
2. A negative Write Enable transition has not occurred when V<sub>CC</sub> is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the mode selection table.

**Absolute Maximum Stress Rating\***

## Temperature

Storage .....	-65°C to +100°C
Under Bias .....	-10°C to +80°C

## All Inputs or Outputs with

Respect to Ground .....	+6V to -0.3V
-------------------------	--------------

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

52B33, 52B33H	
V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**D.C. Operating Characteristics During Read or Erase/Write** (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I <sub>IN</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>O</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
I <sub>WE</sub>	Write Enable Leakage			10	μA	WE = V <sub>IL</sub>
I <sub>CC1</sub>	V <sub>CC</sub> Standby Current		18	40	mA	CE = V <sub>IH</sub>
I <sub>CC2</sub>	V <sub>CC</sub> Active Current		60	110	mA	CE = OE = V <sub>IL</sub>
V <sub>IL</sub>	Input Low Voltage	-0.1		0.8	V	
V <sub>IH</sub>	Input High Voltage	2		V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA

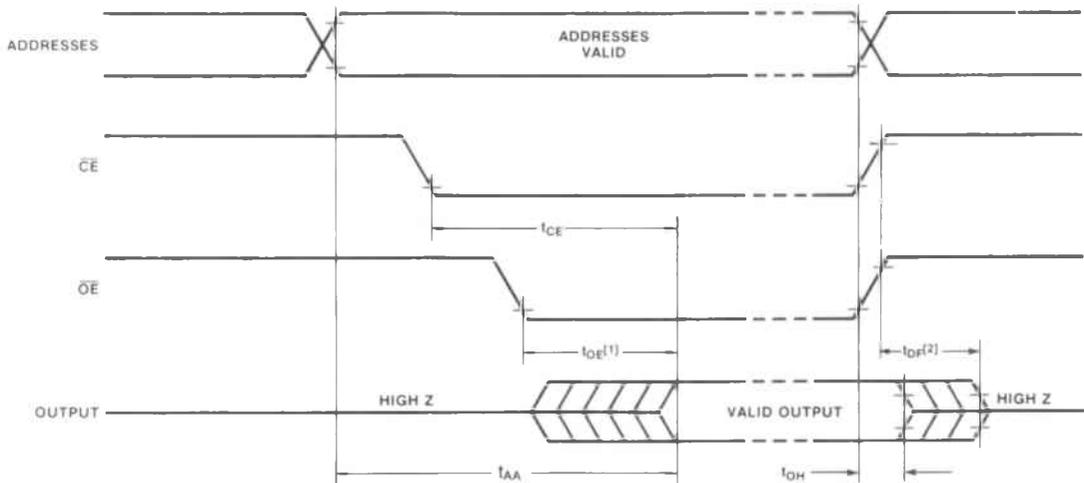
## Notes:

1. Nominal values are for T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5.0 V

## AC Operating Characteristics During Read (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H		Unit	Test Conditions
			Min.	Max.		
$t_{AA}$	Address Access Time	-200 -250 -350		200 250 350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid	-200 -250 -350		200 250 350	ns	$\overline{OE} = V_{IL}$
$t_{OE}^{[1]}$	Output Enable to Data Valid	-200 -250 -350		80 90 100	ns	$\overline{CE} = V_{IL}$
$t_{DF}^{[2]}$	Output Enable to High Impedance	-200 -250 -350	0 0 0	60 70 80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$C_{IN}/C_{OUT}^{[3]}$	Input and Output Capacitance	All		10	pF	$V_{IN} = 0\text{ V}$ for $C_{IN}$ , $V_{OUT} = 0\text{ V}$ for $C_{OUT}$ , $T_A = 25^\circ\text{C}$

### Read Cycle Timing



#### NOTES:

- $\overline{OE}$  may be delayed to  $t_{AA} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{AA}$ .
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
- This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
- After  $t_{WH}$ , hold time, from  $\overline{WE}$ , the inputs  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{CC}$ , Address and Data are latched and are "Don't Cares" until  $t_{WR}$ , Write Recovery Time, after the trailing edge of  $\overline{WE}$ .
- The Write Recovery Time,  $t_{WR}$ , is the time after the trailing edge of  $\overline{WE}$  that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.

**A.C. Test Conditions**Output Load: 1 TTL gate and  $C_L = 100$  pFInput Rise and Fall Times:  $\leq 20$  ns

Input Pulse Levels: 0.45 V to 2.4 V

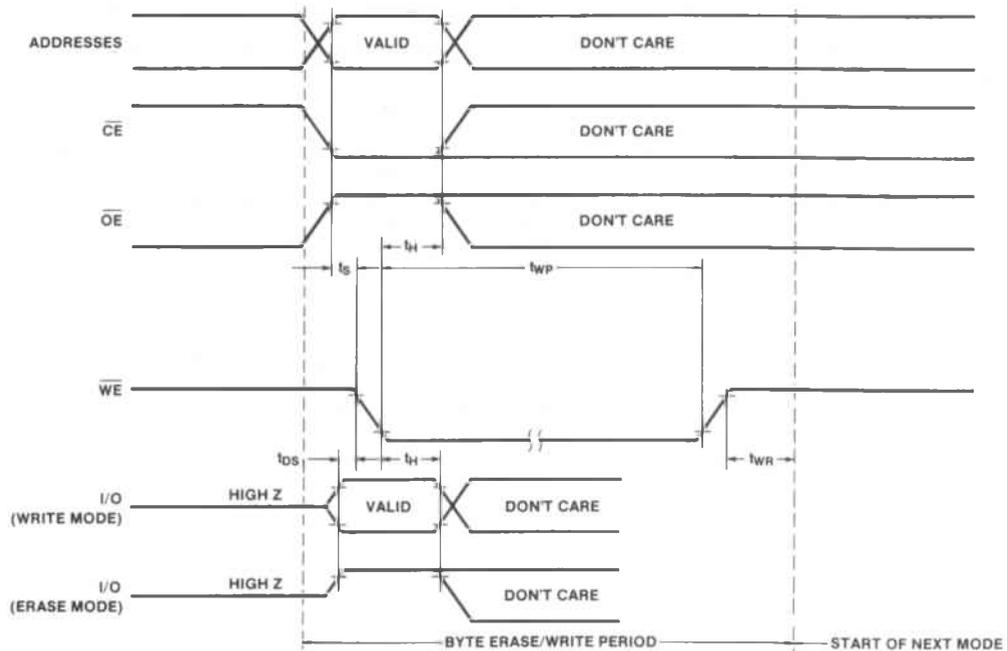
Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

**A.C. Operating Characteristics During Write/Erase** (Over the operating  $V_{CC}$  and temperature range)

Symbol	Parameter	Min.	Max.	Units
$t_S$	CE, $\overline{OE}$ or Address Setup to $\overline{WE}$	50		ns
$t_{DS}$	Data Setup to $\overline{WE}$	15		ns
$t_H^{(4)}$	$\overline{WE}$ to CE, OE, Address or Data Change	50		ns
$t_{WP}$	Write Enable ( $\overline{WE}$ ) Pulse Width Byte Modes — 52B33	9		ms
	Byte Modes — 52B33H	1		
$t_{WR}^{(5)}$	$\overline{WE}$ to Mode change			
	$\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle	1		$\mu$ S

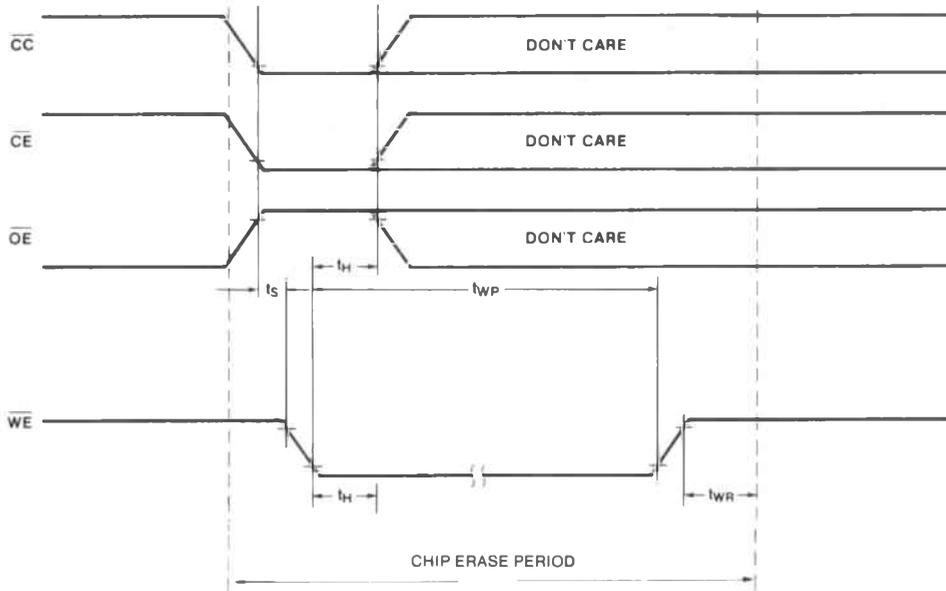
**Byte Erase or Byte Write Cycle Timing**

(Notes 4 and 5 are on previous page)

**A.C. Operating Characteristics During Chip Erase** (Over the operating  $V_{CC}$  and temperature range)

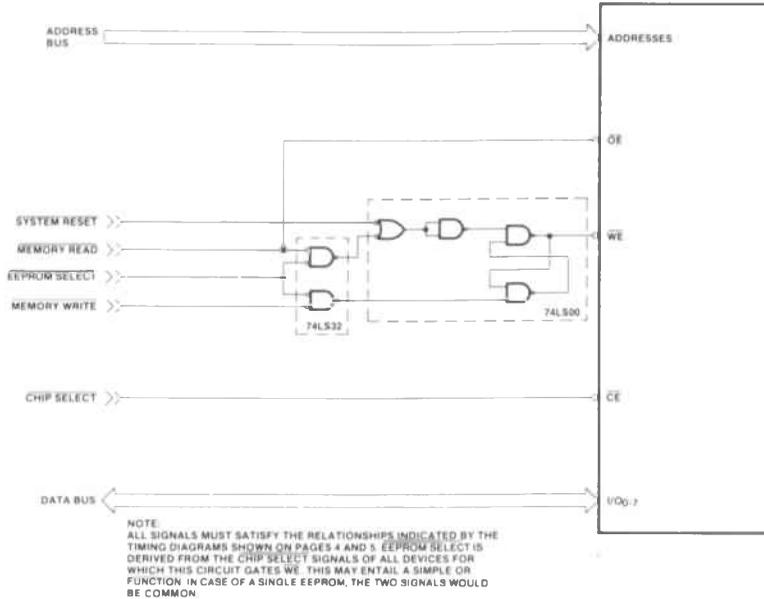
Symbol	Parameter	Min.	Max.	Units
$t_s$	$\overline{CC}$ , $\overline{CE}$ , $\overline{OE}$ Setup to $\overline{WE}$	50		ns
$t_H^{[4]}$	$\overline{WE}$ to $\overline{CE}$ , $\overline{OE}$ , $\overline{CC}$ change	50		ns
$t_{WP}$	Write Enable ( $\overline{WE}$ ) Pulse Width Chip Erase — 52B33 Chip Erase — 52B33H	10		ms
$t_{WR}^{[5]}$	$\overline{WE}$ to Mode change $\overline{WE}$ to Start of Next Byte Write Cycle	50		ns
	$\overline{WE}$ to Start of Read Cycle		1	$\mu s$

**TTL Chip Erase Timing**

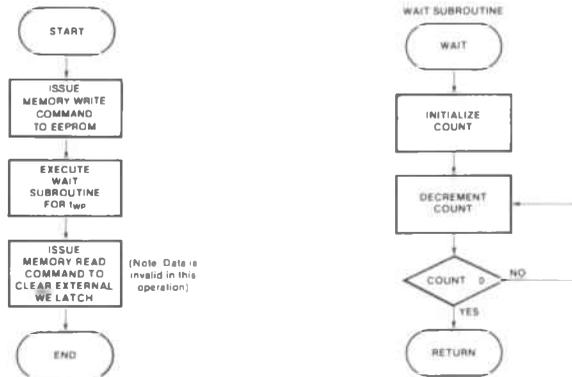


NOTE: Address, Data are don't care during Chip Erase.

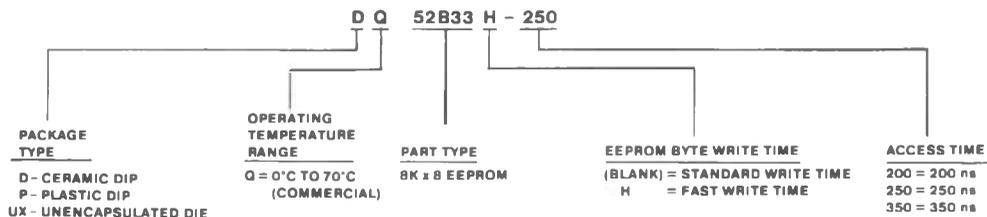
## Microprocessor Interface Circuit Example for Byte Write/Erase



## Typical EEPROM Write/Erase Routine



## Ordering Information





## 4K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1987

### Features

- **High Endurance**  
— 10,000 Cycles/Byte Minimum
- **On-Chip Timer**  
— Automatic Erase and Write Time Out
- **All Inputs Latched by Write or Chip Enable**
- **Direct Replacement to 512 x 8 EEPROMS**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**  
— 80 mA max. Active Current  
— 40 mA max. Standby Current
- **10 Year Data Retention**
- **JEDEC Standard Byte-Wide Pinout**

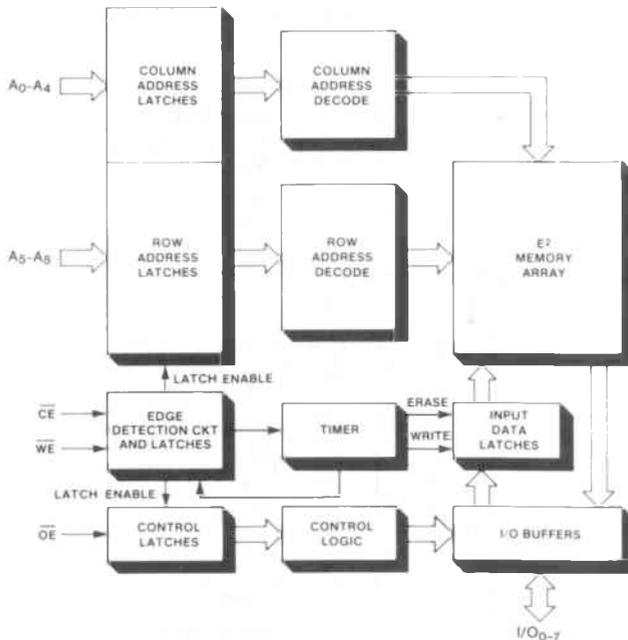
### Description

SEEQ's 2804A is a 5 V only, 512 x 8 electrically erasable programmable read only memory (EEPROM). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times that a byte may be written, is 10 thousand cycles for the 2804A.

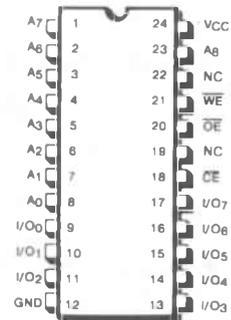
This device has an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable ( $\overline{WE}$ ) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the micro-computer system for other tasks during the write time. The write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

(Continued on page 2)

### Block Diagram



### Pin Configuration



### Pin Names

A <sub>0</sub> -A <sub>4</sub>	COLUMN ADDRESSES
A <sub>5</sub> -A <sub>8</sub>	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)

## Device Operation

There are four operational modes (see Table 1) and only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of  $\overline{CE}$  or  $\overline{WE}$  and data is latched on the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode. The 2804A ignores attempts to read or write while the internal write cycle is in progress.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$   
 Under Bias .....  $-10^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$

### All Inputs or Outputs with

Respect to Ground .....  $+6\text{V}$  to  $-0.3\text{V}$

## Recommended Operating Conditions

2804A	
Temperature Range	(Ambient) $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
$V_{CC}$ Supply Voltage	$5\text{V} \pm 10\%$

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
$T_{DR}$	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

## DC Operating Characteristics $T_A=0^{\circ}$ to $70^{\circ}\text{C}$ ; $V_{CC}=5\text{V} \pm 10\%$ , unless otherwise noted.

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
$I_{CC}$	Active $V_{CC}$ Current		80	mA	$\overline{CE}=\overline{OE}=V_{IL}$ ; All I/O open; Other Inputs = 5.5 V
$I_{SA}$	Standby $V_{CC}$ Current		40	mA	$\overline{CE}=V_{IH}$ , $\overline{OE}=V_{IL}$ ; All I/O's Open; Other Inputs = 5.5 V
$I_{IL}$	Input Leakage Current		10	$\mu\text{A}$	$V_{IN}=5.5\text{V}$
$I_{OL}$	Output Leakage Current		10	$\mu\text{A}$	$V_{OUT}=5.5\text{V}$
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2.0	6	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL}=2.1\text{mA}$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH}=-400\mu\text{A}$

**NOTE:**

1. Characterized Not tested

## Mode Selection (Table 1)

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>
Standby	$V_{IH}$	X	X	HI Z
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>
Write Inhibit	X	$V_{IL}$	X	HI Z/D <sub>OUT</sub>
	X	X	$V_{IH}$	HI Z/D <sub>OUT</sub>

X - Any TTL Level

## Power Up/Down Considerations

The 2804A has internal circuitry to minimize a false write during system  $V_{CC}$  power up or down. This circuitry prevents writing under any one of the following conditions.

- $V_{CC}$  is less than 3 V.<sup>(1)</sup>
- A negative Write Enable ( $\overline{WE}$ ) transition has not occurred when  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the Mode Selection table.

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**AC Characteristics**Read Operation  $T_A=0^\circ$  to  $70^\circ\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ , unless otherwise noted.

Symbol	Parameter	Limits				Units
		2804A-250		2804A-300		
		Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	250		300		ns
$t_{CE}$	Chip Enable Access Time		250		300	ns
$t_{AA}$	Address Access Time		250		300	ns
$t_{OE}$	Output Enable Access Time		90		100	ns
$t_{LZ}$	$\overline{CE}$ to Output in Low Z	10		10		ns
$t_{HZ}$	$\overline{CE}$ to Output in HI Z		100		100	ns
$t_{OLZ}$	$\overline{OE}$ to Output in Low Z	50		50		ns
$t_{OHZ}$	$\overline{OE}$ to Output in HI Z		100		100	ns
$t_{OH}^{(1)}$	Output Hold from Address Change	20		20		ns
$t_{PU}^{(1)}$	$\overline{CE}$ to Power-up Time	0		0		ns
$t_{PD}^{(1)}$	$\overline{CE}$ to Power Down Time		50		50	ns

**Capacitance**<sup>[2]</sup>  $T_A=25^\circ\text{C}$ ,  $f=1\text{ MHz}$ 

Symbol	Parameter	Max	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0\text{ V}$

**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(1)}$	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

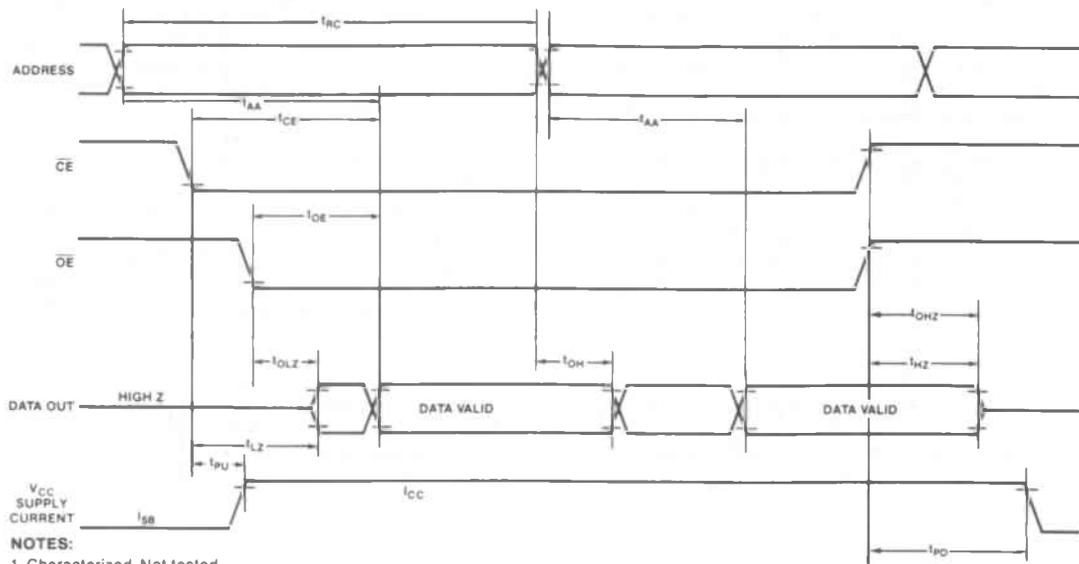
**A.C. Test Conditions**Output Load: 1 TTL gate and  $C_L = 100\text{ pF}$ Input Rise and Fall Times:  $<20\text{ ns}$ 

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

**Read Cycle Timing****NOTES:**

1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

## AC Characteristics

TTL WRITE CYCLE  $T_A=0^\circ$  to  $70^\circ\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ , unless otherwise noted.

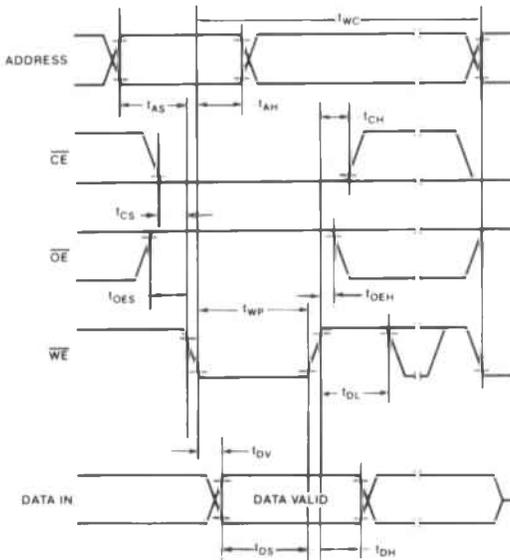
Symbol	Parameter	2804A-250		2804A-300		Units
		Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	10		10		ms
$t_{AS}$	Address Set Up Time	10		10		ns
$t_{AH}$	Address Hold Time	50		70		ns
$t_{CS}$	Write Set Up Time	0		0		ns
$t_{CH}$	Write Hold Time	0		0		ns
$t_{CW}$	$\overline{CE}$ to End of Write Input	150		150		ns
$t_{OES}$	$\overline{OE}$ Set Up Time	10		10		ns
$t_{OEH}$	$\overline{OE}$ Hold Time	10		10		ns
$t_{WP}^{[1]}$	$\overline{WE}$ Write Pulse Width	150		150		ns
$t_{DL}$	Data Latch Time	50		50		ns
$t_{DV}^{[2]}$	Data Valid Time		1		1	$\mu\text{s}$
$t_{DS}$	Data Set Up Time	50		50		ns
$t_{DH}$	Data Hold Time	0		0		ns

**NOTES:**

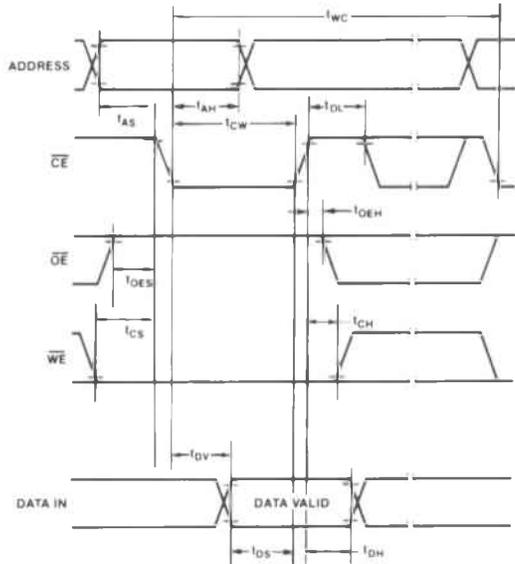
1.  $\overline{WE}$  is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1  $\mu\text{s}$  maximum after the initiation of a write cycle. Characterized, not tested.

### TTL Byte Write Cycle

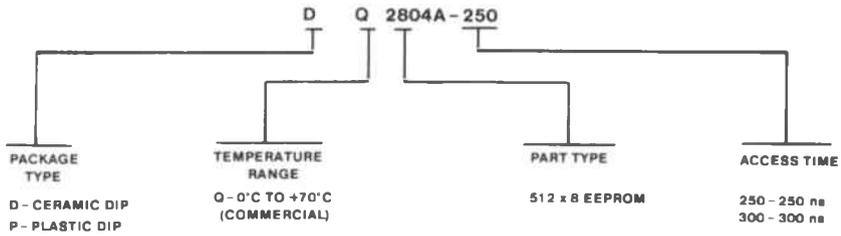
#### $\overline{WE}$ CONTROLLED WRITE CYCLE



#### $\overline{CE}$ CONTROLLED WRITE CYCLE



Ordering and Package Information





### Features

- **High Endurance Write Cycles**
  - 5516A: 1,000,000 Cycles/Byte Minimum
  - 2816A: 10,000 Cycles/Byte Minimum
- **On-Chip Timer**
  - Automatic Erase and Write Time Out
  - 2 ms Byte Write Time (2816AH)
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **200 ns max. Access Time**
- **Low Power Operation**
  - 110 mA max. Active Current
  - 40 mA max. Standby Current
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range Available.**

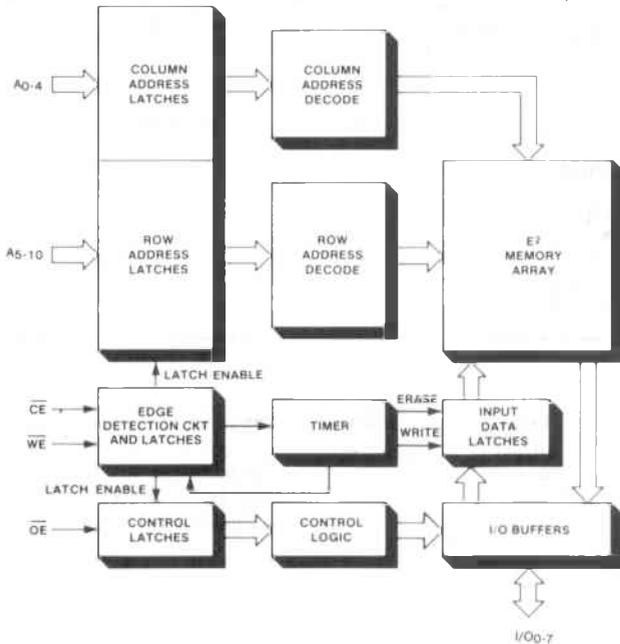
### Description

SEEQ's 5516A and 2816A are 5V only, 2Kx8 electrically erasable programmable read only memories (EEPROMs). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times that a byte may be written, is 1 million for the 5516A and 10 thousand for the 2816A. The 5516A's extraordinary high endurance was accomplished using SEEQ's proprietary oxyntride EEPROM process and its innovative "Q cell" design. The 5516A is ideal for systems that require frequent updates.

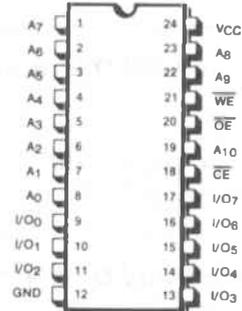
Both EEPROMs have an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable (WE) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system for other tasks during the write time. The standard 2816A and 5516A's write time is 10 ms, while the 2816AH's write time

(continued on next page)

### Block Diagram



### Pin Configuration



### Pin Names

A <sub>0</sub> -A <sub>10</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

is a fast 2 ms. Once a byte is written, it can be read in 200 ns. The inputs are TTL for both the byte write and read mode.

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode<sup>[2]</sup>, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of  $\overline{CE}$  or  $\overline{WE}$  and data is latched on the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

## Mode Selection (Table 1)

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	High Z
Byte Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Write Inhibit	X	V <sub>IL</sub>	X	High Z/D <sub>OUT</sub>
	X	X	V <sub>IH</sub>	High Z/D <sub>OUT</sub>

X: any TTL level

## Power Up/Down Considerations

The 2816A/5516A has internal circuitry to minimize a false write during system V<sub>CC</sub> power up or down. This circuitry prevents writing under any one of the following conditions.

1. V<sub>CC</sub> is less than 3 V.<sup>[3]</sup>
2. A negative Write Enable ( $\overline{WE}$ ) transition has not occurred when V<sub>CC</sub> is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65°C to +150°C

Under Bias ..... -10°C to +80°C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	5516A/5516AH 2816A/2816AH
Temperature Range (Ambient)	0°C to 70°C
V <sub>CC</sub> Supply Voltage	5 V ± 10%

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000 1,000,000 [1]	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

### NOTES:

1. 5516A-1 million cycles/byte
2. Chip Erase is an optional mode
3. Characterized Not tested

## DC Operating Characteristics $T_A=0^\circ$ to $70^\circ\text{C}$ , $V_{CC}=5\text{ V} \pm 10\%$ unless otherwise noted

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
$I_{CC}$	Active $V_{CC}$ Current		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = 5.5 V
$I_{SB}$	Standby $V_{CC}$ Current		40	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O's Open; Other Inputs = 5.5 V
$I_{LI}$	Input Leakage Current		10	$\mu\text{A}$	$V_{IN} = 5.5\text{ V}$
$I_{LO}$	Output Leakage Current		10	$\mu\text{A}$	$V_{OUT} = 5.5\text{ V}$
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2.0	6	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1\text{ mA}$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400\ \mu\text{A}$

## AC Characteristics

Read Operation  $T_A=0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC}=5\text{ V} \pm 10\%$ , unless otherwise noted

Symbol	Parameter	Limits								Units
		5516A/5516AH-200		5516A/5516AH-250		5516A/5516AH-300		2816A-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	200		250		300		350		ns
$t_{CE}$	Chip Enable Access Time		200		250		300		350	ns
$t_{AA}$	Address Access Time		200		250		300		350	ns
$t_{OE}$	Output Enable Access Time		90		90		100		100	ns
$t_{LZ}$	$\overline{CE}$ to Output in Low Z	10		10		10		10		ns
$t_{HZ}$	$\overline{CE}$ to Output in High Z		100		100		100		100	ns
$t_{OLZ}$	$\overline{OE}$ to Output in Low Z	50		50		50		50		ns
$t_{OHZ}$	$\overline{OE}$ to Output in High Z		100		100		100		100	ns
$t_{OH}^{(1)}$	Output Hold from Addr Change	20		20		20		20		ns
$t_{PU}^{(1)}$	$\overline{CE}$ to Power-up Time	0		0		0		0		ns
$t_{PD}^{(1)}$	$\overline{CE}$ to Power Down Time		50		50		50		50	ns

## Capacitance<sup>(2)</sup> $T_A=25^\circ\text{C}$ , $f=1\text{ MHz}$

Symbol	Parameter	Max	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0\text{ V}$

## A.C. Test Conditions

Output Load: 1 TTL gate and  $C_L = 100\text{ pF}$

Input Rise and Fall Times:  $<20\text{ ns}$

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## E.S.D. Characteristics

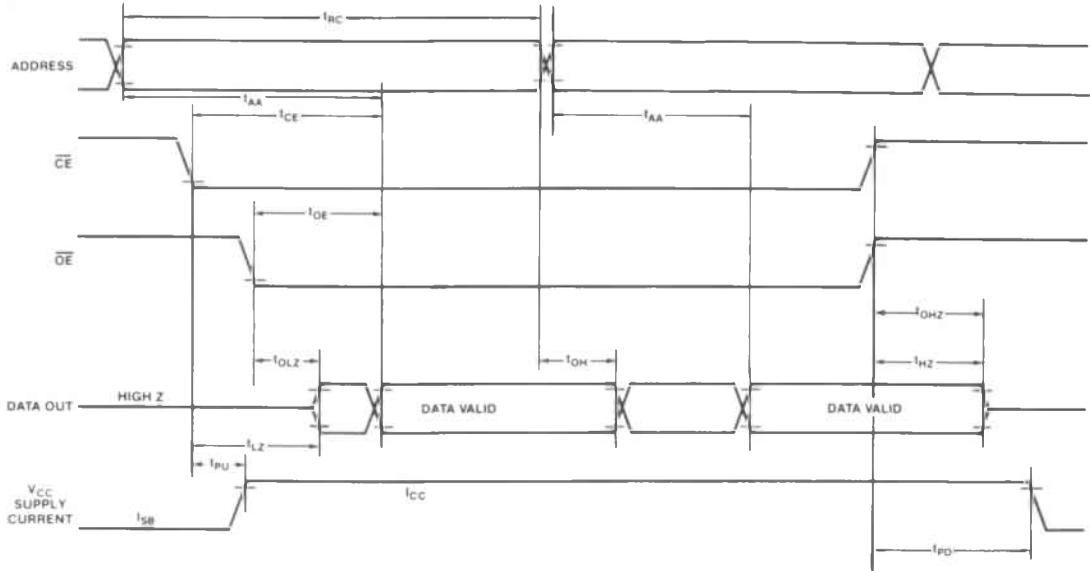
Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(1)}$	E.S.D. Tolerance	$>2000\text{ V}$	MIL-STD 883 Test Method 3015

### NOTES:

1 Characterized. Not tested

2 This parameter measured only for the initial qualification and after process or design changes which may affect capacitance

## Read Cycle Timing



## AC Characteristics

**Write Operation**  $T_A=0^\circ$  to  $70^\circ\text{C}$ ,  $V_{CC}=5\text{ V} \pm 10\%$  unless otherwise noted

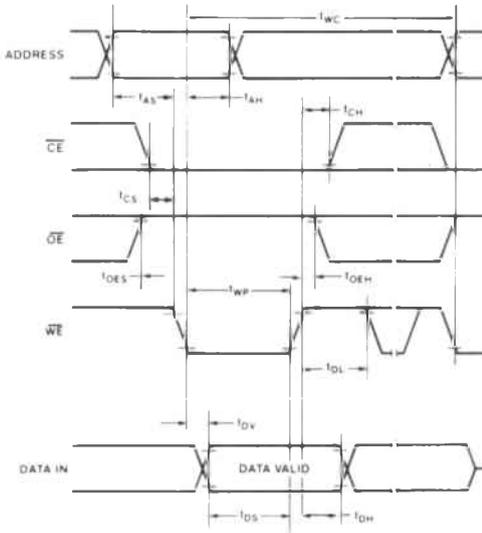
Symbol	Parameter	Limits								Units
		5516A-200 2816A/2816AH-200		5516A-250 2816A/2816AH-250		5516A-300 2816A/2816AH-300		2816A-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{wc}$	Write Cycle Time	2		2		2		—		ms
		10		10		10		10		
$t_{AS}$	Address Set Up Time	10		10		10		10		ns
$t_{AH}$	Address Hold Time	50		50		70		70		ns
$t_{CS}$	Write Set Up Time	0		0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		0		ns
$t_{CW}$	OE to End of Write Input	150		150		150		150		ns
$t_{OES}$	OE Set Up Time	10		10		10		10		ns
$t_{OEH}$	OE Hold Time	10		10		10		10		ns
$t_{wp}^{1)}$	WE Write Pulse Width	150		150		150		150		ns
$t_{DL}$	Data Latch Time	50		50		50		50		ns
$t_{DVL}^{2)}$	Data Valid Time		1		1		1		1	$\mu\text{s}$
$t_{DS}$	Data Set Up Time	50		50		50		50		ns
$t_{DH}$	Data Hold Time	0		0		0		0		ns

**Notes:**

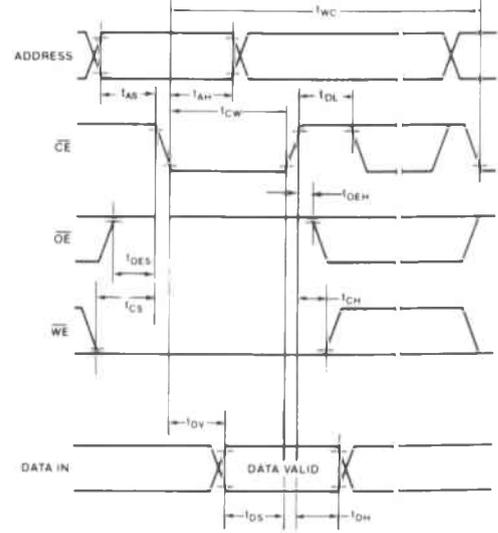
- 1 WE is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
- 2 Data must be valid within 1  $\mu\text{s}$  maximum after the initiation of a write cycle.

## TTL Byte Write Cycle

### $\overline{WE}$ CONTROLLED WRITE CYCLE



### $\overline{CE}$ CONTROLLED WRITE CYCLE



## Ordering Information

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	EEPROM BYTE WRITE TIME	ACCESS TIME
D - CERAMIC DIP P - PLASTIC DIP UX - UNENCAPSULATED DIE	Q - 0°C to +70°C (Commercial)	D Q 5516A - 200 D Q 2816A H - 200	(Blank) - Standard Write Time H - Fast Write Time	200 - 200 ns 250 - 250 ns 300 - 300 ns 350 - 350 ns



### Features

- **Ready/Busy Line for End-of-Write**
- **High Endurance Write Cycles**
  - 5517A: 1,000,000 Cycles/Byte Minimum
  - 2817A: 10,000 Cycles/Byte Minimum
- **On-Chip Timer**
  - Automatic Byte Erase Before Byte Write
  - 2 ms Byte Write Time (2817AH)
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Supply**
- **200 ns max. Access Time**
- **10 Year Data Retention for Each Write**
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range Available**

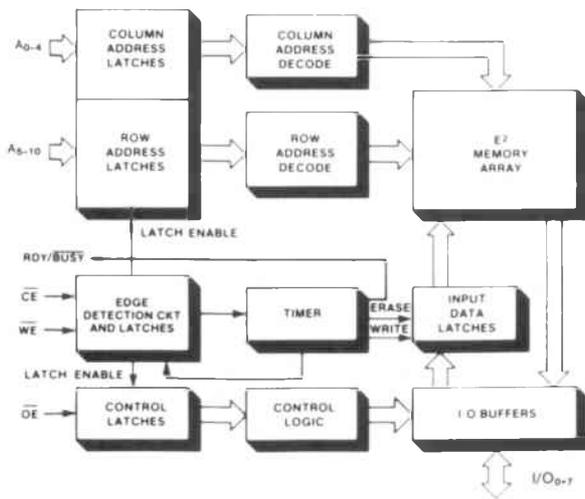
### Description

SEEQ's 5517A and 2817A are 5V only, 2Kx8 electrically erasable programmable read only memories (EEPROMs). They are packaged in a 28 pin package and have a ready/busy pin. These EEPROMs are ideal for applications which require non-volatility

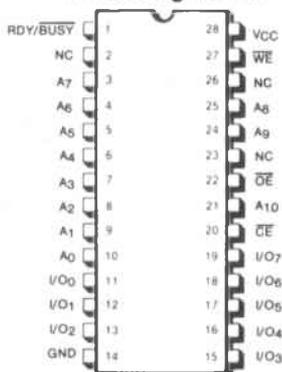
and in-system data modification. The endurance, the minimum number of times which a byte may be written, is 1 million for the 5517A and 10 thousand for the 2817A. The 5517A's extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative "Q cell" design. The 5517A is ideal for systems that require frequent updates and/or high reliability. System reliability is enhanced greatly over lower specified endurance EEPROMs while still maintaining 10 year data retention.

Both EEPROMs have an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard 5517A/2817A's write time is 10 ms, while the 2817AH's write time is a fast 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for either a write or read mode. The inputs are TTL for both the byte write and read mode. Data retention is specified for 10 years.

### Block Diagram



### Pin Configuration



### Pin Names

A <sub>0</sub> -A <sub>10</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
NC	NO CONNECT

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode<sup>[2]</sup>, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the  $RDY/\overline{BUSY}$  output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the  $RDY/\overline{BUSY}$  pin to a TTL high. The  $RDY/\overline{BUSY}$  pin is an open drain output and a typical 3K  $\Omega$  pull-up resistor to  $V_{CC}$  is required. The pull-up resistor value is dependent on the number of OR-tied 2817A  $RDY/\overline{BUSY}$  pins.

## Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	$RDY/\overline{BUSY}$
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>	High Z
Standby	$V_{IH}$	X	X	High Z	High Z
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>	$V_{OL}$
Write Inhibit	X	$V_{IL}$	X	High Z/D <sub>OUT</sub>	High Z
	X	X	$V_{IH}$	High Z/D <sub>OUT</sub>	High Z

X: Any TTL level

## Recommended Operating Conditions

5517A 2817A/2817AH	
$V_{CC}$ Supply Voltage	5 V $\pm$ 10%
Temperature Range (Ambient)	0°C to 70°C

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000 1,000,000 [1]	Cycles/Byte	MIL-STD 883 Test Method 1033
$T_{DR}$	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

### NOTES:

- 5517A — 1 million cycles/byte
- Chip Erase is an optional mode.
- Characterized. Not tested.

## Power Up/Down Considerations

The 2817A/5517A has internal circuitry to minimize a false write during system  $V_{CC}$  power up or down. This circuitry prevents writing under any one of the following conditions.

- $V_{CC}$  is less than 3 V.<sup>[3]</sup>
- A negative Write Enable ( $\overline{WE}$ ) transition has not occurred with  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65°C to +150°C  
Under Bias ..... -10°C to +80°C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. Operating Characteristics (Over the operating V<sub>CC</sub> and temperature range)

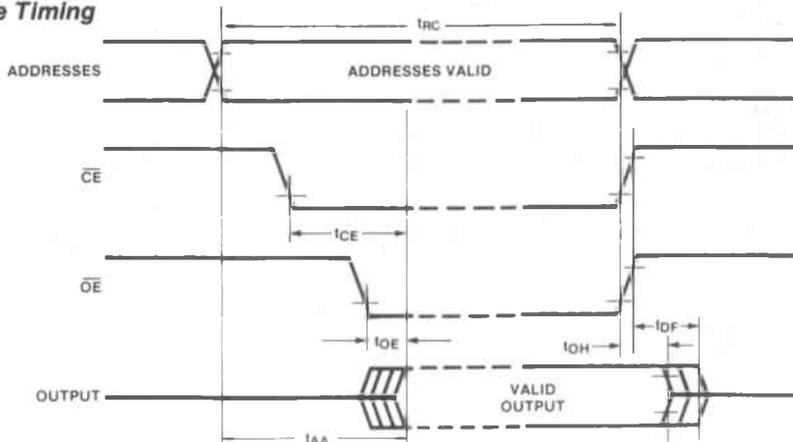
Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current (Includes Write Operation)		110	mA	CE = OE = V <sub>IL</sub> ; All I/O Open; Other Inputs = 5.5 V
I <sub>SB</sub>	Standby V <sub>CC</sub> Current		40	mA	CE = V <sub>IH</sub> , OE = V <sub>IL</sub> ; All I/O Open; Other Inputs = 5.5 V
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = 5.5 V
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = 5.5 V
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

## A.C. Characteristics

### Read Operation (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Limits								Units	Test Conditions
		2817AH-200 2817A-200		2817AH-250 5517A-250 2817A-250		2817AH-300 5517A-300 2817A-300		2817A-350			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read Cycle Time	200		250		300		350		ns	CE = OE = V <sub>IL</sub>
t <sub>CE</sub>	Chip Enable Access Time		200		250		300		350	ns	OE = V <sub>IL</sub>
t <sub>AA</sub>	Address Access Time		200		250		300		350	ns	CE = OE = V <sub>IL</sub>
t <sub>OE</sub>	Output Enable Access Time		75		90		100		100	ns	CE = V <sub>IL</sub>
t <sub>DF</sub>	Output Enable High to Output Not being Driven		60		60		60		80	ns	CE = V <sub>IL</sub>
t <sub>OH</sub>	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		0		ns	CE or OE = V <sub>IL</sub>

### Read Cycle Timing



## Capacitance<sup>[1]</sup> T<sub>A</sub>=25°C, f=1 MHz

Symbol	Parameter	Max	Conditions
C <sub>IN</sub>	Input Capacitance	6 pF	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	Data (I/O) Capacitance	10 pF	V <sub>I/O</sub> = 0 V

## A.C. Test Conditions

Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF

Input Rise and Fall Times: <20 ns

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V <sub>ZAP</sub> <sup>[2]</sup>	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

## AC Characteristics

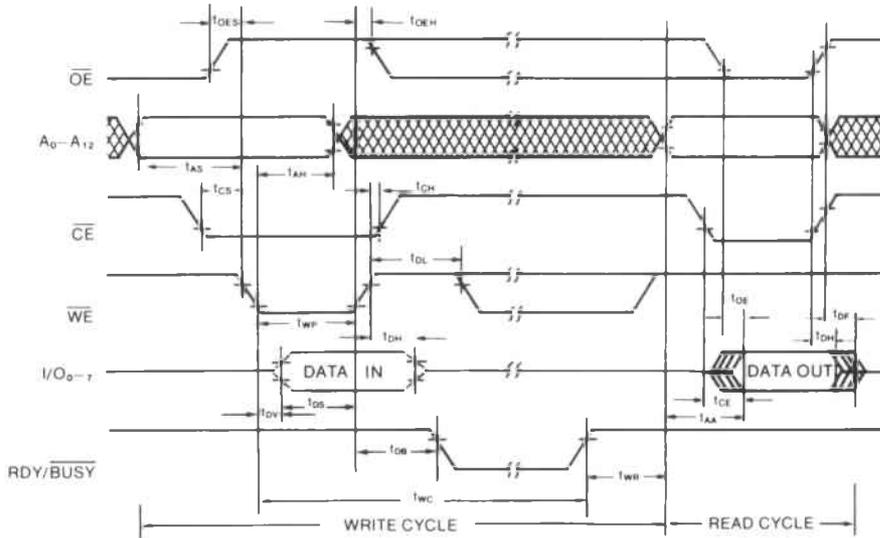
Write Operation (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Limits								Units
		2817AH-200 2817A-200		2817AH-250 5517A-250 2817A-250		2817AH-300 5517A-300 2817A-300		2817A-350		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>AS</sub>	Address to Write Set Up Time	10		10		10		10		ns
t <sub>CS</sub>	$\overline{CE}$ to Write Set Up Time	10		10		10		10		ns
t <sub>WP</sub> <sup>[3]</sup>	$\overline{WE}$ Write Pulse Width	120		150		150		150		ns
t <sub>AH</sub>	Address Hold Time	50		50		50		70		ns
t <sub>DS</sub>	Data Set Up Time	50		50		50		50		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		0		ns
t <sub>CH</sub>	$\overline{CE}$ Hold Time	0		0		0		0		ns
t <sub>OES</sub>	$\overline{OE}$ Set Up Time	10		10		10		10		ns
t <sub>OEH</sub>	$\overline{OE}$ Hold Time	10		10		10		10		ns
t <sub>DL</sub>	Data Latch Time	50		50		50		50		ns
t <sub>DV</sub> <sup>[4]</sup>	Data Valid Time		1		1		1		1	μs
t <sub>DB</sub>	Time to Device Busy		120		120		120		120	ns
t <sub>WR</sub>	Write Recovery Time Before Read Cycle		10		10		10		10	μs
t <sub>wc</sub>	Byte Write Cycle Time	2817A/5517A	10		10		10		10	ms
		2817AH	2		2		2			ms

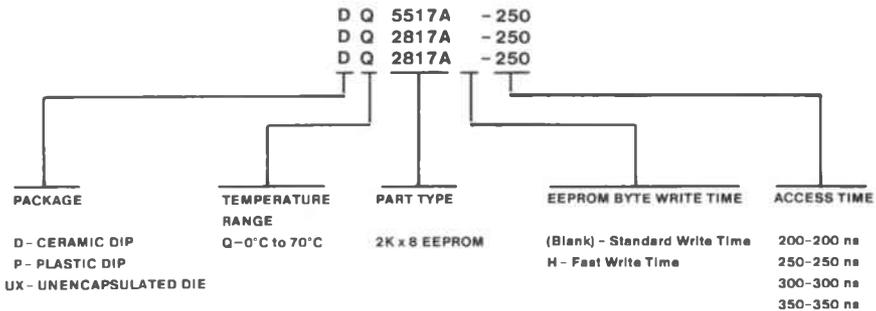
### NOTES:

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.
3.  $\overline{WE}$  is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
4. Data must be valid within 1 ms maximum after the initiation of a write cycle.

## Write Cycle Timing



## Ordering Information





#### Features

- **Ready/Busy Pin**
- **High Endurance Write Cycles**  
— 10,000 Cycles/Byte Minimum
- **On-Chip Timer**  
— Automatic Byte Erase Before Byte Write  
— 2 ms Byte Write (2864H)
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Military and Extended Temperature Range Available**

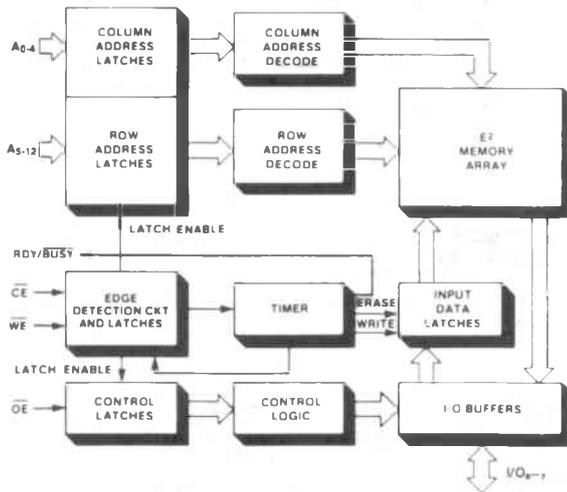
#### Description

SEEQ's 2864 is a 5 V only, 8K x 8 NMOS electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/busy pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is a minimum of 10 thousand cycles.

The EEPROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, a 2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

These two timer EEPROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

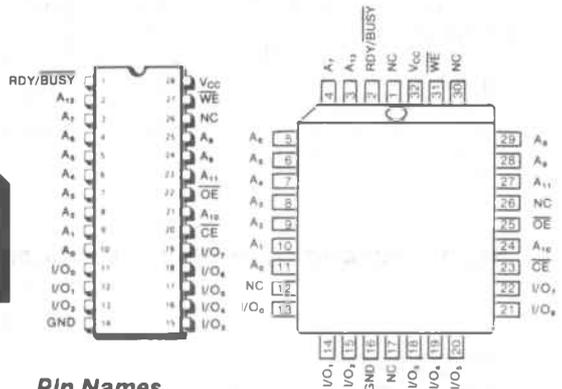
#### Block Diagram



#### Pin Configuration

DUAL-IN-LINE  
TOP VIEW

PLASTIC LEADED CHIP CARRIER  
TOP VIEW



#### Pin Names

A <sub>0-4</sub>	ADDRESSES — COLUMN (LOWER ORDER BITS)
A <sub>5-12</sub>	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE); DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
N/C	NO CONNECT

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the  $RDY/\overline{BUSY}$  output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the  $RDY/\overline{BUSY}$  pin to a TTL high. The  $RDY/\overline{BUSY}$  pin is an open drain output and a typical 3K  $\Omega$  pull-up resistor to  $V_{CC}$  is required. The pull-up resistor value is dependent on the number of OR-tied  $RDY/\overline{BUSY}$  pins. If  $RDY/\overline{BUSY}$  is not used it can be left unconnected.

## Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	$RDY/\overline{BUSY}$ (1)*
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>	High Z
Standby	$V_{IH}$	X	X	High Z	High Z
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>	$V_{OL}$
Write	X	$V_{IL}$	X	High Z/D <sub>OUT</sub>	High Z
Inhibit	X	X	$V_{IH}$	High Z/D <sub>OUT</sub>	High Z

\*Pin 1 has an open drain output and requires an external 3K resistor to  $V_{CC}$ . The value of the resistor is dependent on the number of OR-tied  $RDY/\overline{BUSY}$  pins.

## Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

## Power Up/Down Considerations

The 2864 has internal circuitry to minimize a false write during system  $V_{CC}$  power up or down. This circuitry prevents writing under any one of the following conditions.

1.  $V_{CC}$  is less than 3 V.<sup>(1)</sup>
2. A negative Write Enable ( $\overline{WE}$ ) transition has not occurred when  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

Temperature	
Storage	-65°C to +150°C
Under Bias	-10°C to +80°C

All Inputs or Outputs with Respect to Ground +6 V to -0.3 V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	2864H-250/H-300 2864-250/-300	2864-350
$V_{CC}$ Supply Voltage	5 V $\pm$ 10%	5 V $\pm$ 10%
Temperature Range (Ambient)	0°C to 70°C	0°C to 70°C

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
$T_{DR}$	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

NOTE: 1 - Characterized. Not tested.

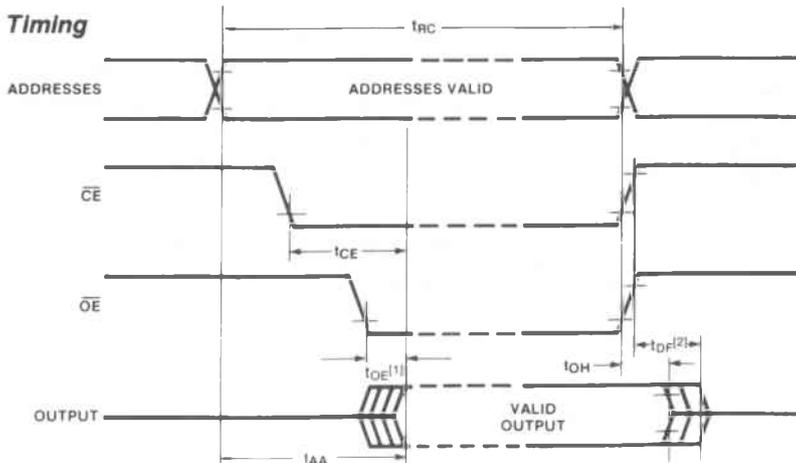
## DC Operating Characteristics (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max.
I <sub>SB</sub>	Standby V <sub>CC</sub> Current		40	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max.
I <sub>LI</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>LO</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

## AC Characteristics Read Operation (Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Limits						Units	Test Conditions
		2864H-250 2864-250		2864H-300 2864-300		2864-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
t <sub>CE</sub>	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
t <sub>AA</sub>	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
t <sub>OE</sub>	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
t <sub>DF</sub>	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
t <sub>OH</sub>	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

### Read Cycle Timing



**NOTES:**

1.  $\overline{OE}$  MAY BE DELAYED TO t<sub>AA</sub> - t<sub>OE</sub> AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON t<sub>AA</sub>.
2. t<sub>DF</sub> IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$ , WHICHEVER OCCURS FIRST.

## Capacitance $T_A^{[1]} = 25^\circ\text{C}$ ; $f = \text{MHz}$

Symbol	Parameter	Max.	Conditions
C <sub>IN</sub>	Input Capacitance	6 pF	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	Data (I/O) Capacitance	10 pF	V <sub>I/O</sub> = 0 V

## AC Test Conditions

Output Load: 1 TTL gate and  $C_L = 100 \text{ pF}$   
 Input Rise and Fall Times: <20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

## E.S.D. Characteristics<sup>[4]</sup>

Symbol	Parameter	Value	Test Conditions
V <sub>ZAP</sub>	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

## AC Characteristics

**Write Operation** (Over operating temperature and V<sub>CC</sub> range)

Symbol	Parameter	Limits						Units
		2864H-250 2864-250		2864H-300 2864-300		2864-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	"H" Family Only		2		2		—	ms
t <sub>AS</sub>	Address to WE Set Up Time	10		10		10		ns
t <sub>CS</sub>	CE to Write Set Up Time	0		0		0		ns
t <sub>WP</sub> <sup>[2]</sup>	WE Write Pulse Width	150		150		150		ns
t <sub>AH</sub>	Address Hold Time	50		50		70		ns
t <sub>DS</sub>	Data Set Up Time	50		50		50		ns
t <sub>DH</sub>	Data Hold Time	20		20		20		ns
t <sub>CH</sub>	CE Hold Time	0		0		0		ns
t <sub>OES</sub>	OE Set Up Time	10		10		10		ns
t <sub>OEH</sub>	OE Hold Time	10		10		10		ns
t <sub>DL</sub>	Data Latch Time	50		50		50		ns
t <sub>DV</sub> <sup>[3]</sup>	Data Valid Time		1		1		1	μs
t <sub>DB</sub>	Time to Device Busy		200		200		200	ns
t <sub>WR</sub>	Write Recovery Time Before Read Cycle		10		10		10	μs

### Notes:

1. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance
2. WE is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 μs maximum after the initiation of a write cycle.
4. Characterized. Not tested.





### Features

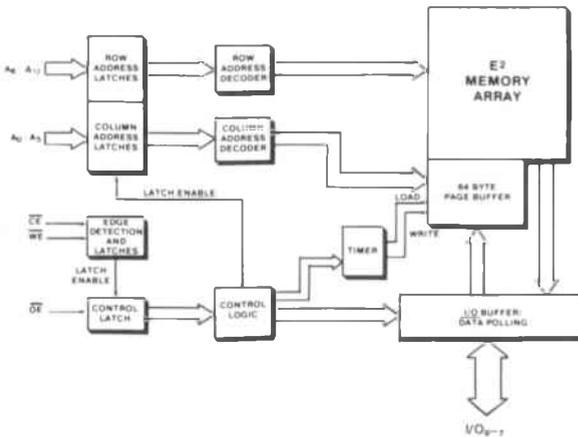
- **CMOS Technology**
- **Low Power**
  - 50 mA Active
  - 150  $\mu$ A Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160  $\mu$ s Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - DATA Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **250 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**
- **Military and Extended Temperature Range Available**

### Description

SEEQ's 28C64 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Plastic Leaded Chip Carrier (PLCC). The 28C64 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and it's innovative "Q-Cell" design. System reliability, in all applications, is higher because of the low failure rate of the Q-Cell.

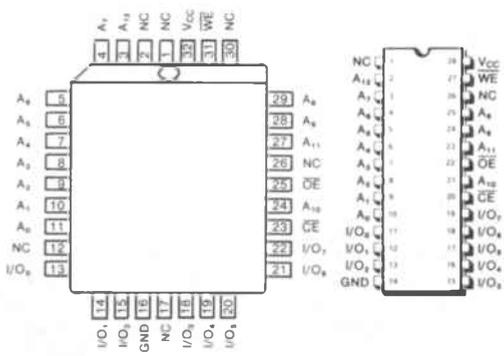
The 28C64 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor

### Pin Configuration



PLASTIC LEADED CHIP CARRIER  
TOP VIEW

DUAL-IN-LINE  
TOP VIEW



### Pin Names

A <sub>0-8</sub>	ADDRESSES—COLUMN
A <sub>9-A<sub>12</sub></sub>	ADDRESSES—ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECTION

for other tasks while the part is busy writing. The 28C64's write cycle time is 10 ms. An automatic erase is performed before a write. The  $\overline{\text{DATA}}$  polling feature of the 28C64 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 250 ns. Data retention is specified for 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and  $\overline{\text{WE}}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

### Mode Selection

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	$V_{\text{IL}}$	$V_{\text{IL}}$	$V_{\text{IH}}$	$D_{\text{OUT}}$
Standby	$V_{\text{IH}}$	X	X	HI Z
Write	$V_{\text{IL}}$	$V_{\text{IH}}$	$V_{\text{IL}}$	$D_{\text{IN}}$
Write Inhibit	X	$V_{\text{IL}}$	X	HI Z/ $D_{\text{OUT}}$
	X	X	$V_{\text{IH}}$	HI Z/ $D_{\text{OUT}}$
Chip Erase	$V_{\text{IL}}$	$V_{\text{H}}$	$V_{\text{IL}}$	X

X: Any TTL level  
 $V_{\text{H}}$ : High Voltage

### Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{\text{CE}}$  is brought to a TTL low in order to enable the chip. The  $\overline{\text{WE}}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{\text{OE}}$ ) to a TTL low. During read, the address,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and I/O latches are transparent.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{\text{WE}}$ ) pin of a selected ( $\overline{\text{CE}}$  low) device. This combined with Output Enable ( $\overline{\text{OE}}$ ) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{\text{WP}}$  time. Data is latched on the rising edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred first. An automatic erase is performed before data is written.

### Write Cycle Control Pins

For system design simplification, the 28C64 is designed such that either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{\text{OE}}$  setup and hold are with respect to the later of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ ; data setup and hold is with respect to the earlier of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ .

To simplify the following discussion, the  $\overline{\text{WE}}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

## Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the 28C64 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated within  $t_{BLC}$  after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle (DATA polling).

## Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the 28C64 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will

not start the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

## DATA Polling

The 28C64 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. DATA polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C64 is **still writing**, the device will present the ones-complement of the last byte written. When the 28C64 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.

A DATA polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. DATA polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a DATA polling read is the same as a normal read.

## Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

## Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$  and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a write in the Mode Selection table.

**Absolute Maximum Stress Range\*****Temperature**

Storage ..... -65°C to +150°C

Under Bias ..... -10°C to +80°C

**All Input or Output Voltages**

with Respect to Ground..... +6 V to -0.3 V

\*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	28C64-250	28C64-300	28C64-350
Temperature Range (Ambient)	0°C to 70°C	0°C to 70°C	0°C to 70°C
V <sub>CC</sub> Power Supply	5 V ± 10%	5 V ± 10%	5 V ± 10%

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

**DC Characteristics** (Over operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max.; Max read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = ANY TTL LEVEL
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		150	μA	$\overline{CE} = V_{CC} - 0.3$ ; Other inputs = V <sub>IL</sub> to V <sub>IH</sub> ; All I/O Open
I <sub>IL</sub> [2]	Input Leakage Current		1	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>OL</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>WI</sub> [1]	Write Inhibit Voltage	3.8		V	

**Notes:**

1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

## AC Test Conditions

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times:  $< 20$  ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

## Capacitance<sup>(1)</sup> $T_A = 25$ C, $f = 1$ MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

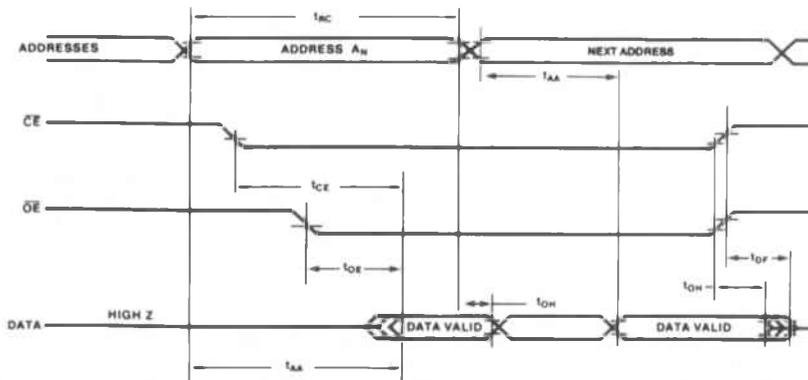
## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	$> 2000$ V	MIL-STD 883 Test Method 3015

## AC Characteristics Read Operation (Over operating temperature and $V_{CC}$ Range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		28C64-250		28C64-300		28C64-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		150		150	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output or Chip Enable High to output not being driven	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

### Read/Data Polling Cycle Time



**NOTES:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested

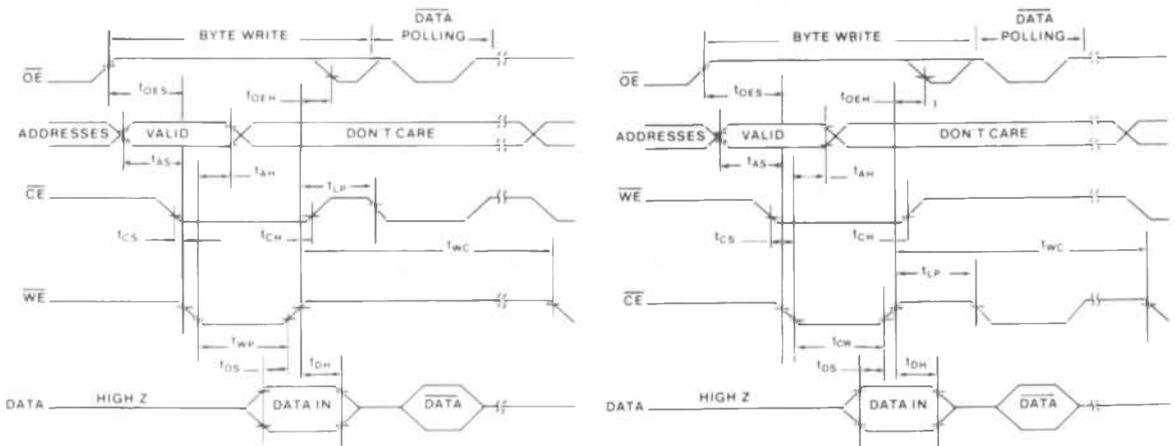
## AC Characteristics Write Operation (Over the operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits						Units
		28C64-250		28C64-300		28C64-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time		10		10		10	ms
t <sub>AS</sub>	Address Set-up Time	10		10		10		ns
t <sub>AH</sub>	Address Hold Time (see note 1)	150		150		150		ns
t <sub>CS</sub>	Write Set-up Time	0		0		0		ns
t <sub>CH</sub>	Write Hold Time	0		0		0		ns
t <sub>CW</sub>	$\overline{CE}$ Pulse Width (note 2)	150		150		150		ns
t <sub>OES</sub>	$\overline{OE}$ High Set-up Time	10		10		10		ns
t <sub>OEH</sub>	$\overline{OE}$ High Hold Time	10		10		10		ns
t <sub>WP</sub>	$\overline{WE}$ Pulse Width (note 2)	150		150		150		ns
t <sub>DS</sub>	Data Set-up Time	50		50		50		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		ns
t <sub>BLC</sub>	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	300	0.2	300	0.2	300	us
t <sub>LP</sub>	Last Byte Loaded to DATA Polling		200		200		200	ns

### Write Timing

#### $\overline{WE}$ CONTROLLED WRITE CYCLE

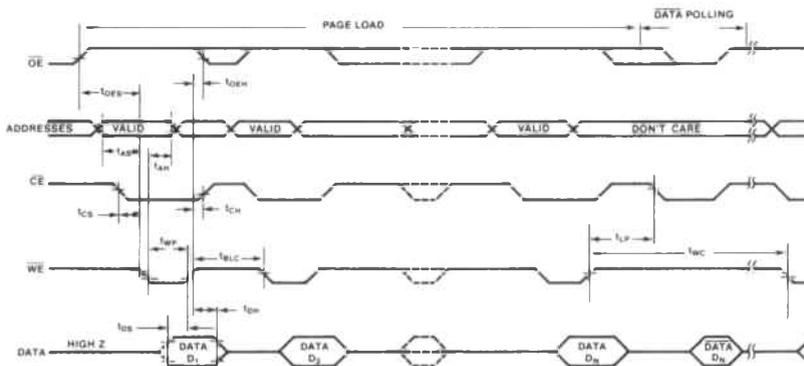
#### $\overline{CE}$ CONTROLLED WRITE CYCLE



#### Notes:

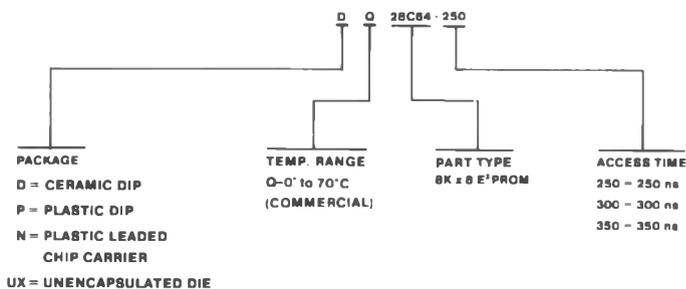
1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3.  $t_{BLC}$  min. is the minimum time before the next byte can be loaded.  $t_{BLC}$  max. is the minimum time the byte load timer waits before initiating internal write cycle.

**Page Write Timing**



EEPROMS

**Ordering Information**





## 64K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1987

### Features

- CMOS Technology
- Low Power
  - 50 mA Active
  - 150  $\mu$ A Standby
- Page Write Mode
  - 64 Byte Page
  - 160  $\mu$ s Average Byte Write Time
- Byte Write Mode
- Write Cycle Completion Indication
  - DATA Polling
  - RDY/BUSY Pin
- On Chip Timer
  - Automatic Erase Before Write
- High Endurance
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- Power Up/Down Protection Circuitry
- 250 ns Maximum Access Time
- JEDEC Approved Byte Wide Pinout
- Military and Extended Temperature Range Available

### Description

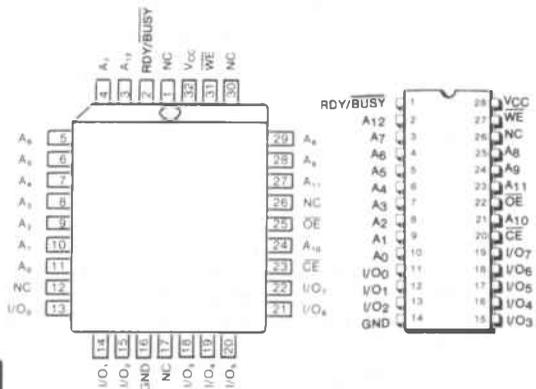
SEEQ's 28C65 is a CMOS 5V only, 8K x 8 electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Plastic Leaded Chip Carrier (PLCC). The 28C65 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and it's innovative "Q-Cell" design. System reliability, in all applications, is high because of the low failure rate of the Q-Cell.

The 28C65 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor

### Pin Configuration

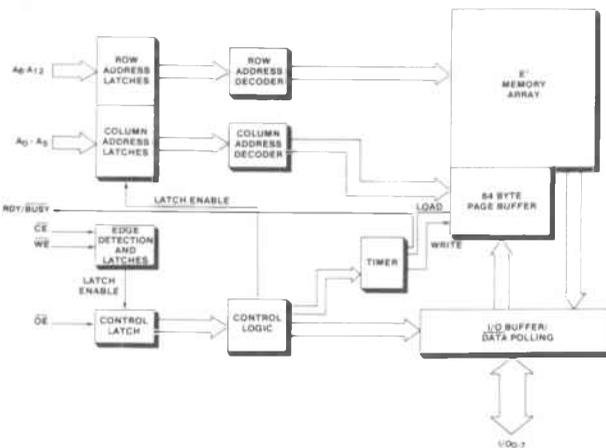
PLASTIC LEADED CHIP CARRIER  
TOP VIEW

DUAL-IN-LINE  
TOP VIEW



### Pin Names

A <sub>0-5</sub>	ADDRESSES — COLUMN
A <sub>6-A12</sub>	ADDRESSES ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
NC	NO CONNECTION



for other tasks while the part is busy writing. The 28C65's write cycle time is 10 ms. An automatic erase is performed before a write. The  $\overline{\text{DATA}}$  polling feature of the 28C65 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 250 ns. Data retention is specified for 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and  $\overline{\text{WE}}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

### Mode Selection

MODE	CE	OE	WE	I/O	RDY/BUSY <sup>(1)</sup>
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	HI Z
Standby	V <sub>IH</sub>	X	X	HI Z	HI Z
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>	V <sub>OL</sub>
Write Inhibit	X	V <sub>IL</sub>	X	HI Z/D <sub>OUT</sub>	HI Z
	X	X	V <sub>IH</sub>	HI Z/D <sub>OUT</sub>	HI Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub>	V <sub>IL</sub>	X	HI Z

X: Any TTL level  
V<sub>H</sub>: High Voltage

### Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{\text{CE}}$  is brought to a TTL low in order to enable the chip. The  $\overline{\text{WE}}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{\text{OE}}$ ) to a TTL low. During read, the address,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and I/O latches are transparent.

### NOTES:

1. RDY/BUSY Pin 1 (Pin 2 on PLCC) has an open drain output and requires an external 3K resistor to V<sub>cc</sub>. The value of the resistor is dependent on the number of OR-tied RDY/BUSY pins.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{\text{WE}}$ ) pin of a selected ( $\overline{\text{CE}}$  low) device. This combined with Output Enable ( $\overline{\text{OE}}$ ) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{wp}$  time. Data is latched on the rising edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred first. An automatic erase is performed before data is written.

### Write Cycle Control Pins

For system design simplification, the 28C65 is designed such that either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{\text{OE}}$  setup and hold are with respect to the later of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ ; data setup and hold is with respect to the earlier of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ .

To simplify the following discussion, the  $\overline{\text{WE}}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC characteristics.

## Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the 28C65 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated within  $t_{BLC}$  after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle (DATA polling).

## Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the 28C65 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will not start the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

## DATA Polling

The 28C65 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time.

DATA polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C65 is **still writing**, the device will present the ones-complement of the last byte written. When the 28C65 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.

A DATA polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. DATA polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a DATA polling read is the same as a normal read.

## READY/BUSY Pin

28C65 provides write cycle status on this pin. RDY/BUSY output goes to a TTL low immediately after the falling edge of  $\overline{WE}$ . RDY/BUSY will remain low during the byte load or page load cycle and continues to remain at a TTL low while the write cycle is in progress. An internal timer times out the required write cycle time and at the end of this time, the device signals RDY/BUSY pin to a TTL high. This pin can be polled for write cycle status or used to initiate a rising edge triggered interrupt indicating write cycle completion. The RDY/BUSY pin is an open drain output and a typical 3 K pull-up resistor to  $V_{CC}$  is required. The pull-up value is dependent on the number of OR-tied RDY/BUSY pins. If RDY/BUSY is not used it can be left unconnected.

## Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

## Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}V$
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}V$  and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a write in the Mode Selection table.

## Absolute Maximum Stress Range\*

### Temperature

Storage ..... -65°C to +150°C  
 Under Bias ..... -10°C to +80°C

### All Input or Output Voltages

with Respect to Ground ..... +6 V to -0.3 V

\*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	28C65-250	28C65-300	28C65-350
Temperature Range (Ambient)	0°C to 70°C	0°C to 70°C	0°C to 70°C
V <sub>CC</sub> Power Supply	5 V ± 10%	5 V ± 10%	5 V ± 10%

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

## DC Characteristics (Over operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max.; Max read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = ANY TTL LEVEL
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		150	μA	$\overline{CE} = V_{CC} - 0.3$ ; Other inputs = V <sub>IL</sub> to V <sub>IH</sub> ; All I/O Open
I <sub>IL</sub> [2]	Input Leakage Current		1	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>OL</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>WI</sub> [1]	Write Inhibit Voltage	3.8		V	

**Notes:**

1. Characterized. Not tested.
2. Inputs only. Does not include I/O.

## AC Test Conditions

Output Load: 1 TTL gate and  $C_L = 100$  pF

Input Rise and Fall Times:  $< 20$  ns

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## Capacitance<sup>(1)</sup> $T_A = 25$ C, $f = 1$ MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

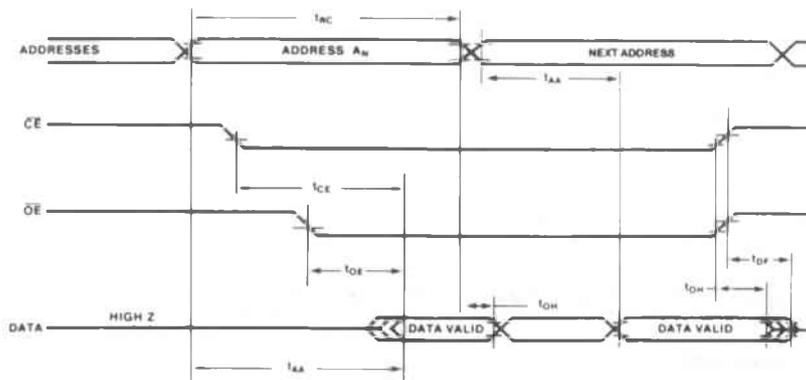
## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	$> 2000$ V	MIL-STD 883 Test Method 3015

## AC Characteristics Read Operation (Over operating temperature and $V_{CC}$ Range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		28C65-250		28C65-300		28C65-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$CE = OE = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$OE = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$CE = OE = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		150		150	ns	$CE = V_{IL}$
$t_{DF}$	Output or Chip Enable High to output not being driven	0	60	0	80	0	80	ns	$CE = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$CE = OE = V_{IL}$

### Read/Data Polling Cycle Time



**Notes:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

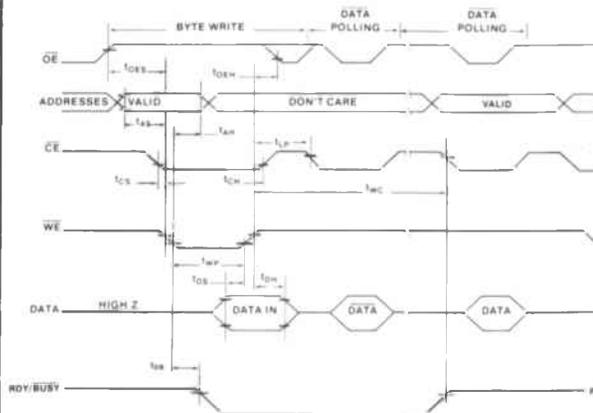
### AC Characteristics

**Write Operation** (Over the operating  $V_{CC}$  and temperature range)

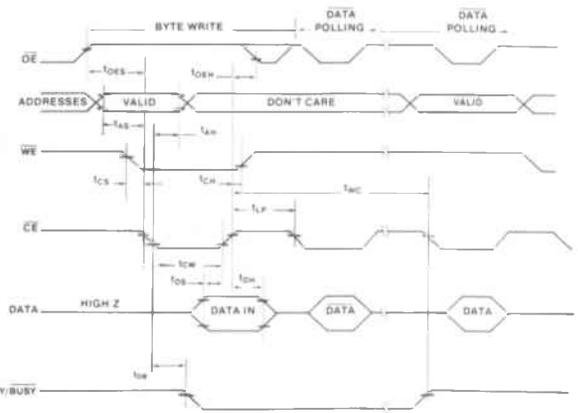
Symbol	Parameter	Limits						Units
		28C65-250		28C65-300		28C65-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time		10		10		10	ms
$t_{AS}$	Address Set-up Time	10		10		10		ns
$t_{AH}$	Address Hold Time (see note 1)	150		150		150		ns
$t_{CS}$	Write Set-up Time	0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		ns
$t_{CW}$	CE Pulse Width (note 2)	150		150		150		ns
$t_{OES}$	OE High Set-up Time	10		10		10		ns
$t_{OEH}$	OE High Hold Time	10		10		10		ns
$t_{WP}$	WE Pulse Width (note 2)	150		150		150		ns
$t_{DS}$	Data Set-up Time	50		50		50		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{BLC}$	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	300	0.2	300	0.2	300	us
$t_{LP}$	Last Byte Loaded to DATA Polling		200		200		200	ns
$t_{DB}$	Time to Device Busy		100		100		100	ns

### Write Timing

**WE CONTROLLED WRITE CYCLE**



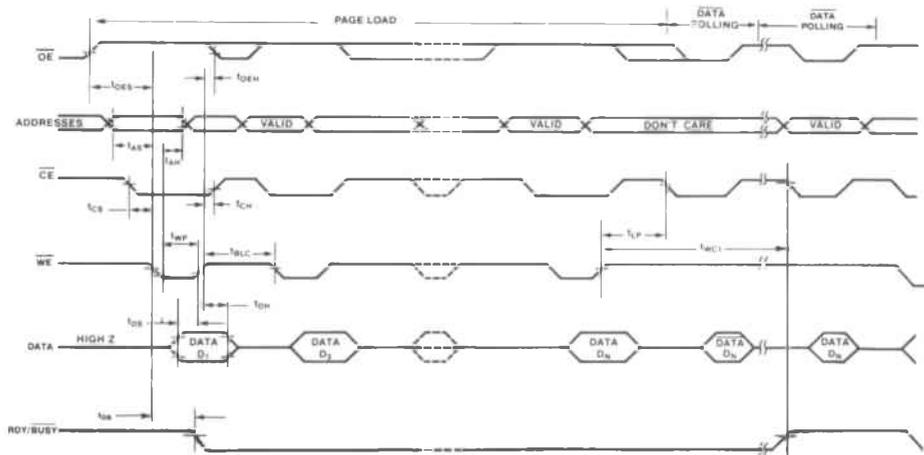
**CE CONTROLLED WRITE CYCLE**



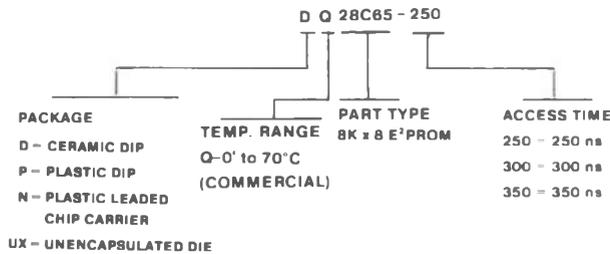
**NOTES:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3.  $t_{BLC}$  min. is the minimum time before the next byte can be loaded.  $t_{BLC}$  max. is the minimum time the byte load timer waits before initiating the internal write cycle.

## Page Write Timing



## Ordering Information





## 256K Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1987

### Features

- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 150  $\mu$ A Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 us Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - DATA Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **250 ns Maximum Access Time**
- **Military and Extended Temperature Range Available.**

### Description

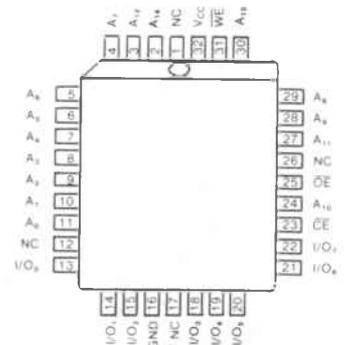
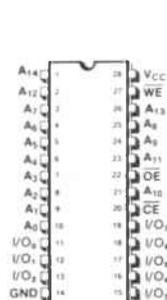
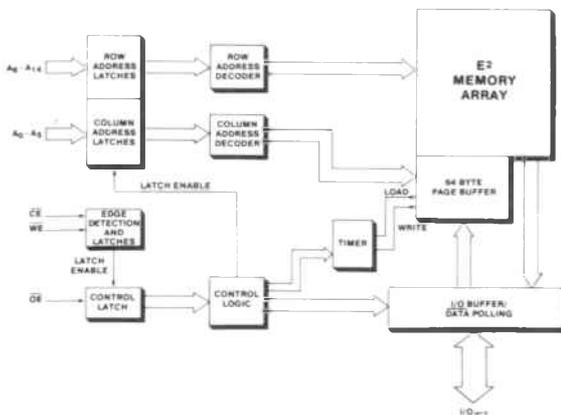
SEEQ's 28C256 is a CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The 28C256 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative "Q-Cell" design. System reliability in all applications is higher because of the low failure rate of the Q-Cell.

The 28C256 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the micro-

### Pin Configuration

DUAL-IN-LINE  
TOP VIEW

PLASTIC LEADED CHIP CARRIER  
TOP VIEW



### Pin Names

A <sub>0-5</sub>	ADDRESSES - COLUMN
A <sub>6-14</sub>	ADDRESSES - ROW
$\bar{C}E$	CHIP ENABLE
$\bar{O}E$	OUTPUT ENABLE
$\bar{W}E$	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE)/DATA OUTPUT (READ)

processor for other tasks while the part is busy writing. The 28C256's write cycle time is 10 ms maximum. An automatic erase is performed before a write. The DATA polling feature of the 28C256 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 250 ns. Data retention is greater than 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the aforementioned three input lines.

**Table 1**

### Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	HI Z
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Write Inhibit	X	X	V <sub>IH</sub>	HI Z/D <sub>OUT</sub>
	X	V <sub>IL</sub>	X	HI Z/D <sub>OUT</sub>
Chip Erase	V <sub>IL</sub>	V <sub>H</sub>	V <sub>IL</sub>	X

X: any TTL level  
V<sub>H</sub>: High Voltage

### Reads

A read is typically accomplished by presenting the addresses of the desired byte to the address inputs. Once the address is stable,  $\overline{CE}$  is brought to a TTL low in order to enable the chip. The  $\overline{WE}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{OE}$ ) to a TTL low. During read, the addresses,  $\overline{CE}$ ,  $\overline{OE}$ , and input data latches are transparent.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This combined with Output Enable ( $\overline{OE}$ ) being high initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{WP}$  time. Data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred first. An automatic erase is performed before data is written.

The 28C256 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

### Write Cycle Control Pins

For system design simplification, the 28C256 is designed such that either the  $\overline{CE}$  or  $\overline{WE}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{CE}$  or  $\overline{WE}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{OE}$  set up and hold are with respect to the later of  $\overline{CE}$  or  $\overline{WE}$ ; data set up and hold is with respect to the earlier of  $\overline{WE}$  or  $\overline{CE}$ .

To simplify the following discussion, the  $\overline{WE}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

### Write Mode

One to 64 bytes of data can be randomly loaded into the device. The part latches row addresses, A6-A14, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of  $t_{WC}$ . This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the 28C256 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated in ( $t_{BLC}$ ) after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can now be read to determine the end of write cycle (DATA Polling).

### Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will inhibit the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

### DATA Polling

The 28C256 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. DATA polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C256 is still writing, the device will present the ones-complement of the last byte written. When the 28C256 has completed its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A DATA polling read should not be done until a minimum of  $t_{LP}$  microseconds after the last byte is written. Timing for a DATA polling read is the same as a normal read once the  $t_{LP}$  specification has been met.

### Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

### Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$  V
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$  V and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

**Absolute Maximum Stress Range\***

Temperature  
 Storage..... -65°C to +150°C  
 Under Bias..... -10°C to +80°C  
 All input or Output Voltages  
 with Respect to V<sub>SS</sub>..... +6 V to -0.3 V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

28C256	
Temperature Range	(Ambient) 0°C to 70°C
V <sub>CC</sub> Supply Voltage	5 V ± 10%

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**DC Characteristics Read Operation** (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		60	mA	CE=OE=V <sub>IL</sub> ; All I/O open; Other Inputs = V <sub>CC</sub> Max. Min. read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	CE=V <sub>IH</sub> , OE=V <sub>IL</sub> ; All I/O open; Other Inputs = V <sub>IL</sub> to V <sub>IH</sub>
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		150	µA	CE=V <sub>CC</sub> -0.3 Other Inputs = V <sub>IL</sub> to V <sub>IH</sub> All I/O Open
I <sub>IL</sub> <sup>[2]</sup>	Input Leakage Current		1	µA	V <sub>IN</sub> =V <sub>CC</sub> Max.
I <sub>OL</sub> <sup>[3]</sup>	Output Leakage Current		10	µA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> =-400 µA
V <sub>WI</sub> <sup>[1]</sup>	Write Inhibit Voltage	3.8		V	

**NOTES:**

- 1 Characterized. Not tested.
- 2 Inputs only. Does not include I/O.
- 3 For I/O only.

**AC Test Conditions**

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times: <20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**Capacitance<sup>(1)</sup>**  $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

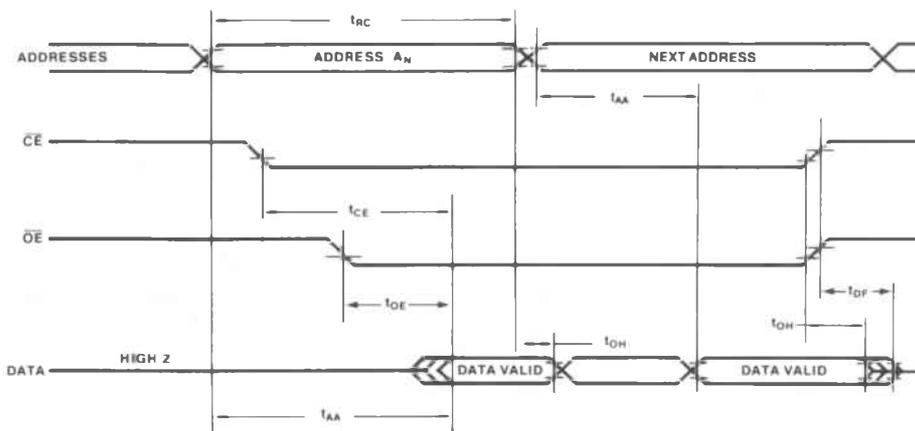
**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	> 2000 V.	MIL-STD 883 Test Method 3015

**AC Characteristics Read Operation** (Over operating temperature and  $V_{CC}$  range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		28C256-250		28C256-300		28C256-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		90		90	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output or Chip Enable High to output in Hi-Z	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

**Read/DATA Polling Cycle**



**Notes:**

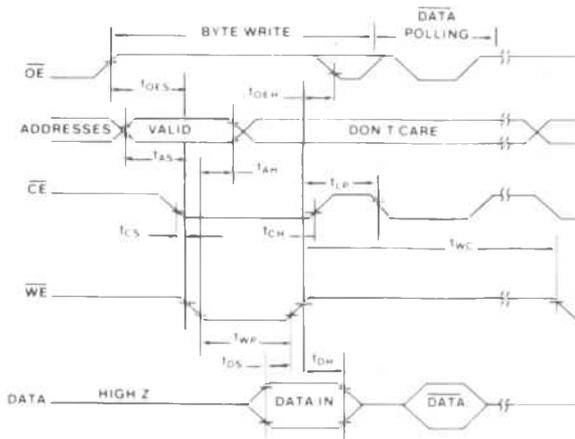
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

**AC Characteristics Write Operation** (Over the operating temperature and  $V_{CC}$  range, unless otherwise specified)

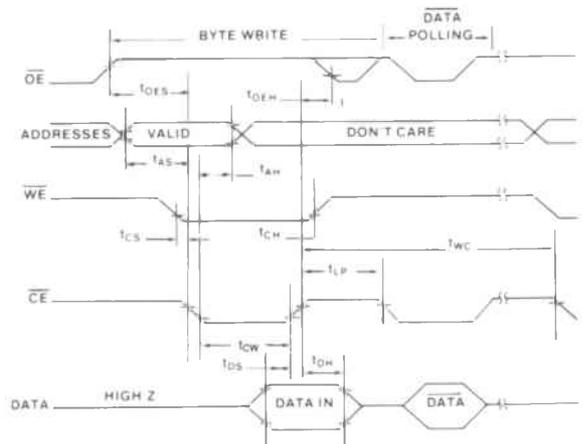
Symbol	Parameter	Limits						Units
		28C256-250		28C256-300		28C256-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time		10		10		10	ms
$t_{AS}$	Address Set-up Time	20		20		20		ns
$t_{AH}$	Address Hold Time (see note 1)	150		150		150		ns
$t_{CS}$	Write Set-up Time	0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		ns
$t_{CW}$	$\overline{CE}$ Pulse Width (note 2)	150		150		150		ns
$t_{OES}$	$\overline{OE}$ High Set-up Time	20		20		20		ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	20		20		20		ns
$t_{WP}$	$\overline{WE}$ Pulse Width (note 2)	150		150		150		ns
$t_{DS}$	Data Set-up Time	50		50		50		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{BLC}$	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	300	0.2	300	0.2	300	us
$t_{LP}$	Last Byte Loaded to DATA Polling Output		600		600		600	us

**Write Timing**

**$\overline{WE}$  CONTROLLED WRITE CYCLE**



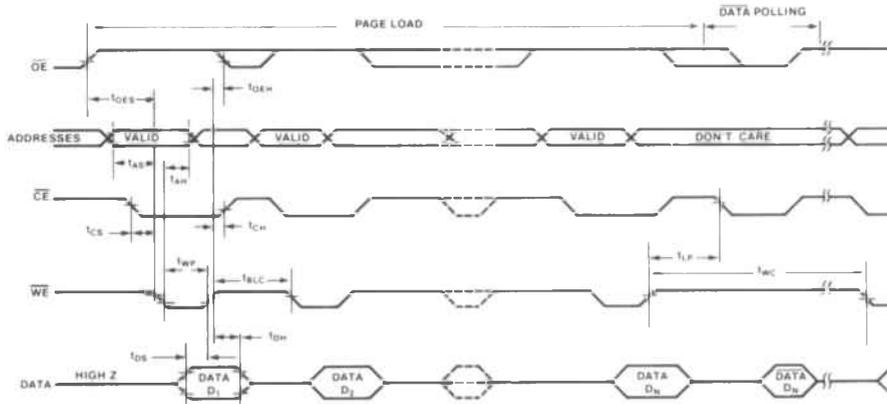
**$\overline{CE}$  CONTROLLED WRITE CYCLE**



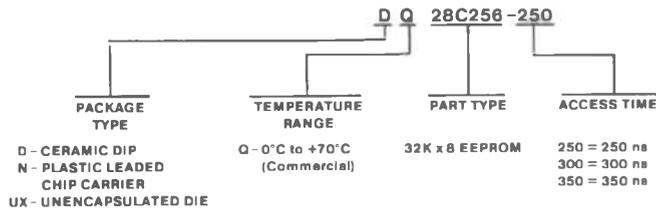
**Notes:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3.  $t_{BLC}$  min. is the minimum time before the next byte can be loaded.  $t_{BLC}$  max. is the minimum time the byte load timer waits before initiating internal write cycle.

**Page Write Timing**



**Ordering Information**

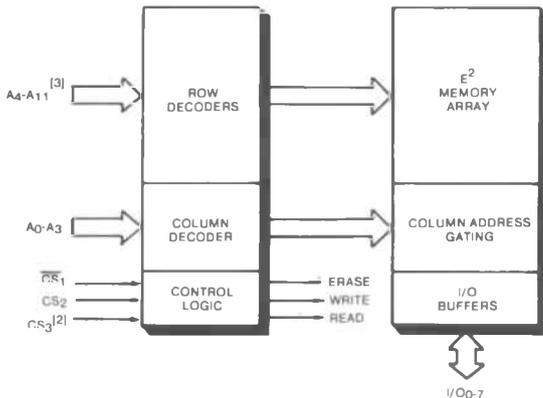




### Features

- **High Speed:**
  - 35 ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 350 mW
- **10 Year Data Retention**
- **High Output Drive**
  - Sink 16 mA At 0.45 V
  - Source 4 mA At 2.4 V
- **5V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **50 ms Chip Erase**
- **Fast Byte Write**
  - 5 ms/Byte
- **Automatic byte clear before write**
- **Jedec approved byte wide pinout**
- **Direct replacement for bipolar PROMS**
- **Slim 300 mil Packaging Available**
- **Military and Extended Temperature Range Available.**

### Block Diagram



### Pin Names

A <sub>0</sub> -A <sub>3</sub>	ADDRESSES — COLUMN
A <sub>4</sub> -A <sub>11</sub> <sup>[3]</sup>	ADDRESSES — ROW
$\overline{CS}_1$ CS <sub>2</sub> CS <sub>3</sub>	CHIP SELECT INPUTS
I/O	DATA INPUT (WRITE) DATA OUTPUT (READ)

### Description

SEEQ's 36C16/32 are high speed 2K x 8 / 4K x 8 Electrically Erasable Programmable Read Only Memories, manufactured using SEEQ's advanced 1.25 micron CMOS process.

The 36C16/32 are intended as bipolar PROM replacements in high speed applications. The 35 ns maximum read access time meets the requirements of many of today's high performance processors. In addition they offer in-system reprogrammability. The endurance, the number of times the part can be erased/written, is specified to be greater than 100 cycles. The 36C16/32 are built using SEEQ's proprietary oxynitride EEPROM process and its innovative "DQ cell" design. System reliability in applications where writes are frequent is increased because of the low endurance-failure rate of the DQ-cell.

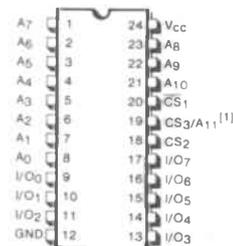
Data retention is specified to be greater than 10 years.

The 36C16/32 are available in 24 pin Slim 300 mil CERAMIC DIP and PLASTIC DIP. 24/28 pin full featured EEPROM versions are also available (38C16/32). All parts are available in commercial as well as military temperature ranges.

### Pin Configuration

#### DUAL-IN-LINE TOP VIEW

#### 36C16/36C32 (24 pins)



- NOTES: 1. Pin 19 is A<sub>11</sub> on the 36C32.  
2. CS<sub>3</sub> is on the 36C16 only.  
3. A<sub>4</sub>-A<sub>10</sub> on 36C16.

**Device Operation**  
**Operational Modes**

MODE PIN	CS <sub>1</sub>	CS <sub>2</sub>	CS <sub>3</sub> <sup>[2]</sup>	I/O
Read	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	HI Z
	X	V <sub>IL</sub>	X	
	X	X	V <sub>IL</sub>	
Write	V <sub>H</sub> <sup>[1]</sup>	V <sub>IL</sub>	X	D <sub>IN</sub>

X: Any TTL level

**Read**

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, the chip select inputs should be brought to the proper levels in order to enable the outputs (see Table above).

**Write**

To write into a particular location, addresses and data must be valid, CS<sub>2</sub> must be TTL low and a V<sub>H</sub><sup>[1]</sup> pulse has to be applied to CS<sub>1</sub> for 5ms. An automatic internal byte clear is done prior to the byte write. The byte clear feature is transparent to the user.

**NOTES:**

1. V<sub>H</sub> - High Voltage.
2. CS<sub>3</sub> applies only to the 36C16. This pin becomes A<sub>1,1</sub> in the 36C32 and a don't care during operational modes.

## Absolute Maximum Rating

### Temperature

Storage..... -65°C to +150°C

Under Bias..... -10°C to +80° C

### All Inputs and Outputs

with Respect to Ground..... -0.5 V to +7 V

### Dedicated High Voltage Inputs

with Respect to Ground..... -0.5 V to +14V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	36C16 36C32
V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

## DC Operating Characteristics (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		100	mA	CS <sub>2</sub> =CS <sub>3</sub> =V <sub>IH</sub> ; $\overline{CS}_1=V_{IL}$ ; All inputs = V <sub>CC</sub> Max. Max read/write cycle time
I <sub>IN</sub>	Input Leakage Current		1	μA	0.1V ≥ V <sub>IN</sub> ≤ V <sub>CC</sub> Max.
I <sub>OUT</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2	V <sub>CC</sub> + 1	V	
V <sub>H</sub>	Input High Voltage During Write/Chip Erase	10.8	13.2	V	For $\overline{CS}_1$ Input Only
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =16 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> =-4 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
I <sub>OS</sub> <sup>(1)</sup>	Output Short Circuit Current	-20	-90	mA	V <sub>CC</sub> =V <sub>CC</sub> Max, V <sub>OUT</sub> =0
V <sub>CI</sub> <sup>(1)</sup>	Input Clamp Voltage	-1.5		V	V <sub>IN</sub> Pulse width ≤ 10ns

**NOTE:**

1. Only one output at a time for less than one second.

## AC Test Conditions

Output Load: 10 TTL gates and total  $C_L = 30$  pF  
 Input Rise and Fall Times:  $< 5$  ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

## Capacitance <sup>(1)</sup> $T_A=25^\circ\text{C}$ , $f=1$ MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0\text{V}$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0\text{V}$

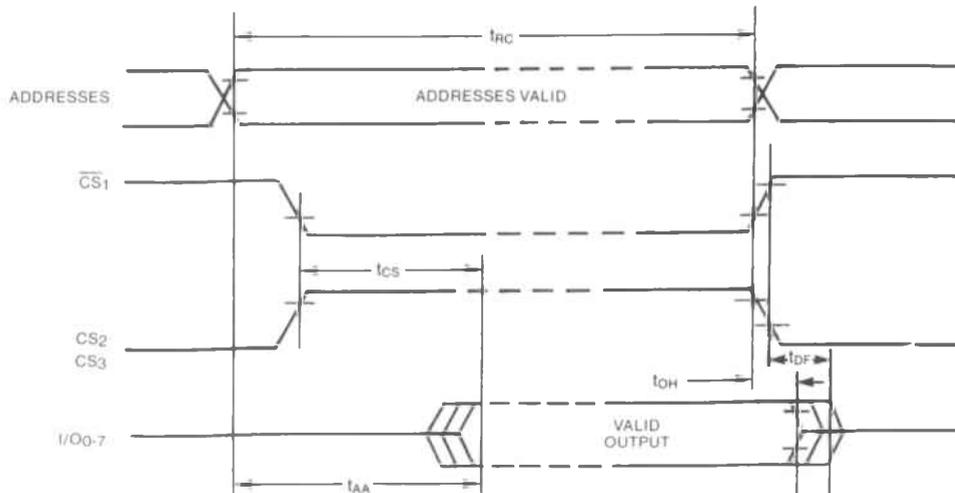
## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	$>2000$ V	MIL-STD 883 Test Method 3015

## AC Characteristics Read Operation (Over operating temperature and $V_{CC}$ Range, unless otherwise specified)

Symbol	Parameter	Limits						Units
		36C16-35 36C32-35		36C16-45 36C32-45		36C16-55 36C32-55		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	35		45		55		ns
$t_{CS}$	Chip Select Access Time		25		30		35	ns
$t_{AA}$	Address Access Time		35		45		55	ns
$t_{DF}$	Output Enable to Output not being Driven		25		25		30	ns
$t_{OH}$	Output Hold from Address Change or Chip Select whichever occurs first	0		0		0		ns

## Read Cycle Timing



**Notes:**

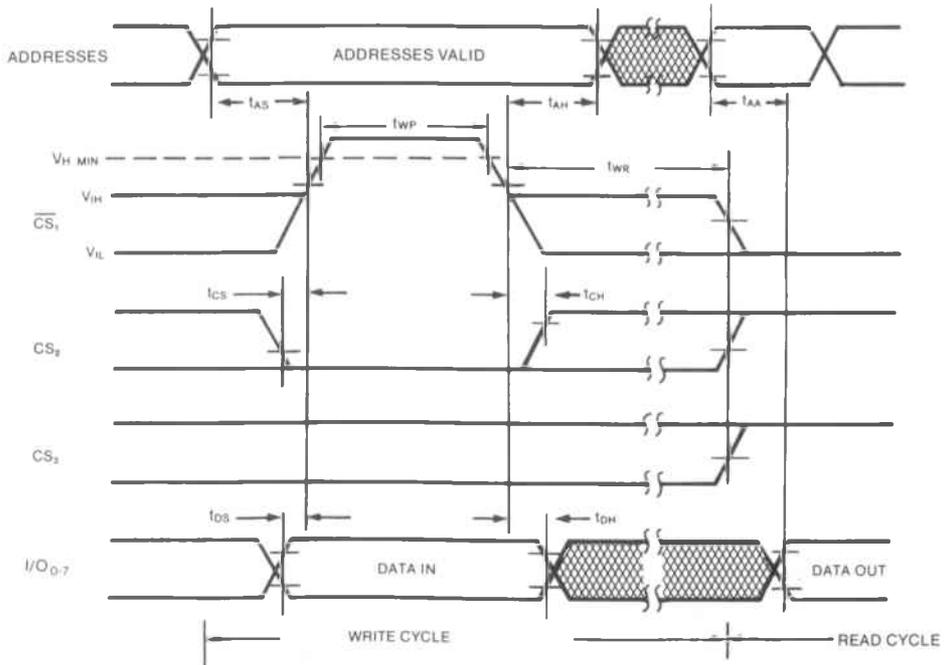
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized Not tested.

**AC Characteristics Write Operation (All Speeds)**

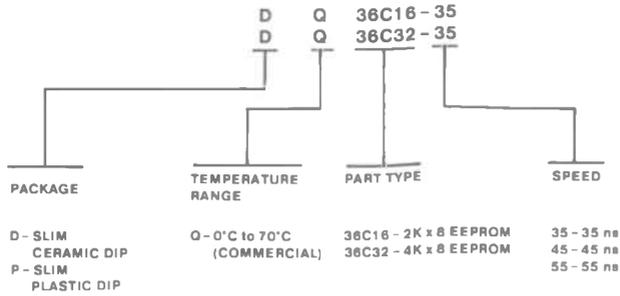
(Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	36C16 36C32		Units
		Min.	Max.	
$t_{WP}$	Write Pulse Width	5	50	ms
$t_{AS}$	Address Set-up Time	0		$\mu$ s
$t_{AH}$	Address Hold Time	0.5		$\mu$ s
$t_{CS}$	CS <sub>2</sub> Set-up Time	0		$\mu$ s
$t_{CH}$	CS <sub>2</sub> Hold Time	0		$\mu$ s
$t_{DS}$	Data Set-up Time	0		$\mu$ s
$t_{DH}$	Data Hold Time	0		$\mu$ s
$t_{WR}$	Write Recovery		10	$\mu$ s

**Write Cycle Timing**



## Ordering Information



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## High Speed CMOS Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1987

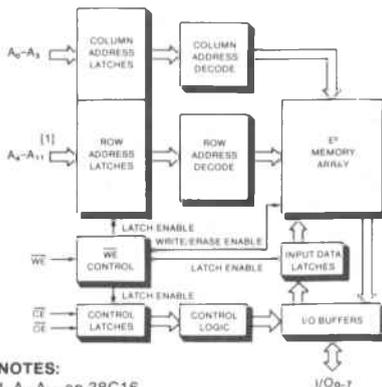
### Features

- **High Speed:**
  - 35 ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 350 mW
- **High Endurance:**
  - 10,000 Cycles/Byte Minimum
  - 10 Year Data Retention
- **On-Chip Timer and Latches**
  - Automatic Byte Erase Before Write
  - Fast Byte Write: 5 ms/Byte
- **High Speed Address/Data Latching**
- **50 ms Chip Erase**
- **5V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **DATA Polling of Data Bit 7**
- **Jedec approved Byte Wide Pinout**
  - 38C16: 2816A Pin Compatible
  - 38C32: 28C64 Pin Compatible
- **Military and Extended Temperature Range Available.**

### Pin Names

A <sub>0</sub> -A <sub>3</sub>	ADDRESSES — COLUMN
A <sub>4</sub> -A <sub>11</sub> <sup>[1]</sup>	ROW ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)

### Block Diagram



#### NOTES:

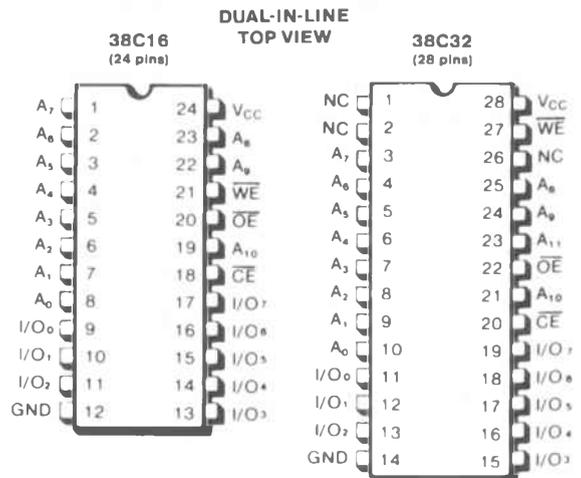
1. A<sub>4</sub>-A<sub>10</sub> on 38C16.
2. NC — No Connect

### Description

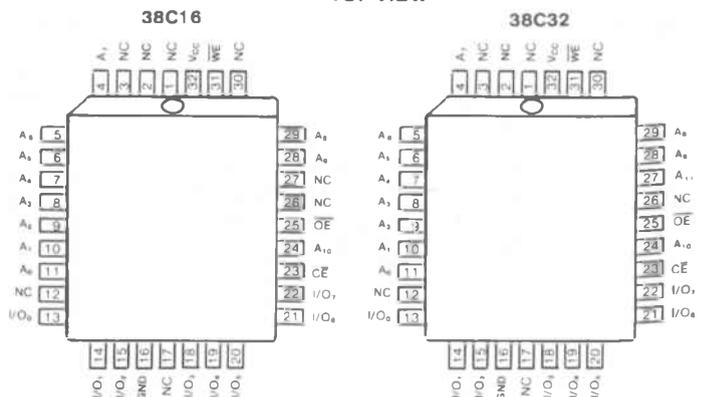
SEEQ's 38C16/32 are high speed 2K x 8 / 4K x 8 Electrically Erasable Programmable Read Only Memories (EEPROM), manufactured using SEEQ's advanced 1.25 micron CMOS process.

The 38C16/32 are ideal for high speed applications which require non-volatility and in-system reprogrammability. The endurance, the number of times a byte may be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinarily high endurance

### Pin Configuration



### PLASTIC LEADED CHIP CARRIER TOP VIEW



was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative "DQ cell" design. System reliability in applications where writes are frequent is increased because of the low endurance-failure rate of the DQ-cell. The 35 ns maximum access time meets the requirements of many of today's high performance processors. The 38C16/32 have an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time. DATA Polling can be used to determine the end of a write cycle. All inputs are TTL compatible for both write and read modes.

Data retention is specified to be greater than 10 years.

The 38C16 and 38C32 are both available in CERAMIC DIP, PLASTIC DIP and PLCC packages. 24 pin versions of both 38C16 and 38C32 intended for bipolar PROM replacement are also available (36C16/36C32). All parts are available in commercial as well as military temperature ranges.

## Device Operation

### Operational Modes

MODE PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>
Standby	$V_{IH}$	X	X	HI Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>
Write Inhibit	X	X	$V_{IH}$	HI Z/D <sub>OUT</sub>
	$V_{IH}$	X	X	HI Z
	X	$V_{IL}$	$V_{IH}$	HI Z/D <sub>OUT</sub>
	$V_{IL}$	$V_{IL}$	$V_{IL}$	No Operation (HI Z)
Chip Erase <sup>[1]</sup>	$V_{IH}$	$V_H$ <sup>[2]</sup>	$V_{IH}$	HI Z

X: Any TTL level

### Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable,  $\overline{CE}$  is brought to a TTL low in order to enable the chip. The  $\overline{WE}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ( $\overline{OE}$ ) to a TTL low. During read, the address,  $\overline{CE}$ ,  $\overline{OE}$ , and I/O latches are transparent.

#### NOTES:

1. Chip erase is an optional mode.
2.  $V_H$  — High Voltage.

### Write

To write into a particular location, addresses must be valid and a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This initiates a write cycle. During a write cycle, all inputs except for data are latched on the falling edge of  $\overline{WE}$  (or  $\overline{CE}$ , whichever one occurred last). Write enable needs to be at a TTL low only for the specified  $t_{WP}$  time. Data is latched on the rising edge of  $\overline{WE}$  (or  $\overline{CE}$ , which ever one occurred first). An automatic byte erase is performed before data is written.

### DATA Polling

The EEPROM has a specified  $t_{WC}$  write cycle time of 5ms. The typical device has a write cycle time faster than the  $t_{WC}$ . DATA polling is a method to indicate the completion of a timed write cycle. During the internal write cycle, the complement of the data bit 7 is presented at output 7 when a read is performed. Once the write cycle is finished, the true data is presented at the outputs. A software routine can be used to "poll", i.e. read the output, for true or complemented data bit 7. The polling cycle specifications are the same as for a read cycle. During data polling, the addresses are don't care.

### Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

### Power Up/Down Considerations

Protection against false write during  $V_{CC}$  power up/down is provided through on chip circuitry. Writing is prevented under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$ .
1. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$  V and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than those specified for a byte write in the Mode Selection table.

**Absolute Maximum Rating**

Temperature  
 Storage..... -65°C to +150°C  
 Under Bias..... -10°C to +80°C  
 All Inputs and Outputs  
 with Respect to Ground..... -0.5 V to +7 V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	38C16 38C32
V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range (Ambient)	0°C to 70°C

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**DC Operating Characteristics** (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		100	mA	$\overline{CE}=\overline{OE}=V_{IL}$ ; All I/O open; All other inputs = V <sub>CC</sub> Max. Max read/write cycle time
I <sub>SB</sub>	Stand by V <sub>CC</sub> Current		60	mA	$\overline{CE}=V_{IH}$ ; All I/O open; All other inputs TTL don't care;
I <sub>IN</sub>	Input Leakage Current		1	μA	0.1V > V <sub>IN</sub> <= V <sub>CC</sub> Max.
I <sub>OUT</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =2 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> =-400 μA, V <sub>CC</sub> Min.
V <sub>WI</sub> <sup>[1]</sup>	Write Inhibit Voltage	3.8		V	

NOTES:  
 1. Characterized. Not tested.

## AC Test Conditions

Output Load: 1 TTL gate and total  $C_L = 30$  pF  
 Input Rise and Fall Times:  $< 5$  ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**Capacitance**<sup>[1]</sup>  $T_A=25^\circ\text{C}$ ,  $f=1$  MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

## E.S.D. Characteristics

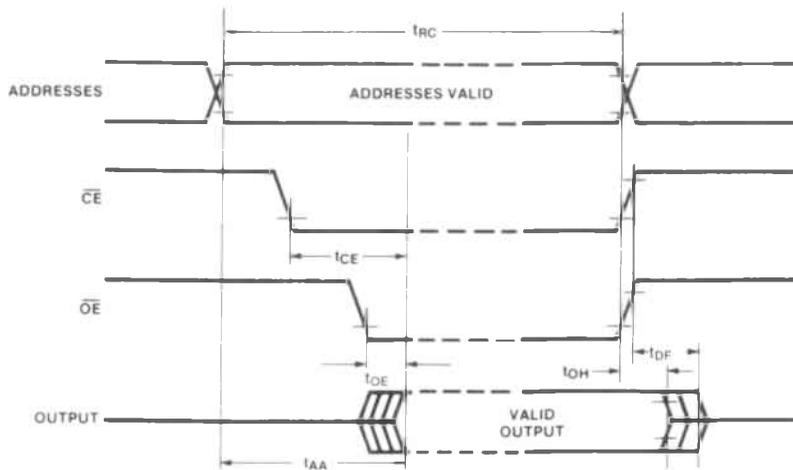
Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{[2]}$	E.S.D. Tolerance	$>2000$ V	MIL-STD 883 Test Method 3015

## AC Characteristics Read Operation

(Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		38C16-35 38C32-35		38C16-45 38C32-45		38C16-55 38C32-55			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	35		45		55		ns	$\overline{CE}=\overline{OE}=V_{IL}$
$t_{CE}$	Chip Enable Access Time		25		30		35	ns	$\overline{OE}=V_{IL}$
$t_{AA}$	Address Access Time		35		45		55	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$t_{OE}$	Output Enable Access Time		20		25		30	ns	$\overline{CE}=V_{IL}$
$t_{DF}$	Output Or Chip Enable To Output Float		15		20		30	ns	$\overline{CE}=V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable Or Output Enable Which ever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE}=V_{IL}$

## Read Cycle Timing



**NOTES:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

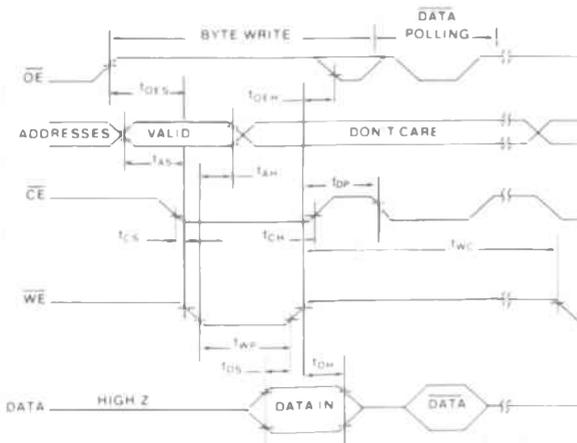
## AC Characteristics Write Operation

(Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

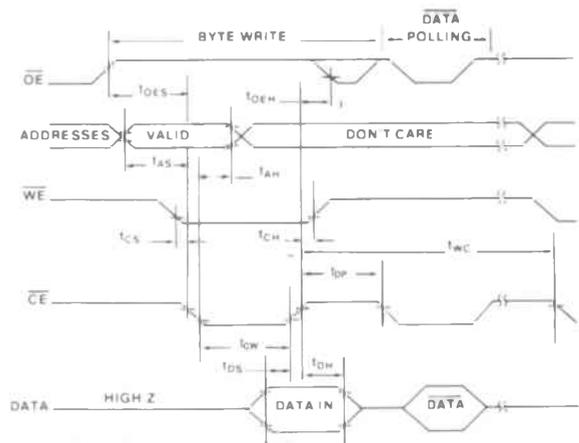
Symbol	Parameter	38C16-35 38C32-35		38C16-45 38C32-45		38C16-55 38C32-55		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time		5		5		5	ms
t <sub>AS</sub>	Address Set-up Time	0		0		0		ns
t <sub>AH</sub>	Address Hold Time	25		25		30		ns
t <sub>CS</sub>	Write Set-up Time	0		0		0		ns
t <sub>CH</sub>	Write Hold Time	0		0		0		ns
t <sub>CW</sub>	CE Pulse Width	20		25		30		ns
t <sub>OES</sub>	OE High Set-up Time	5		5		5		ns
t <sub>OEH</sub>	OE High Hold Time	0		0		0		ns
t <sub>WP</sub>	WE Pulse Width	20		25		30		ns
t <sub>DS</sub>	Data Set-up Time	20		25		30		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		ns
t <sub>DP</sub>	Time to DATA Polling from Byte Latch		35		45		55	ns

## Write Cycle Timing

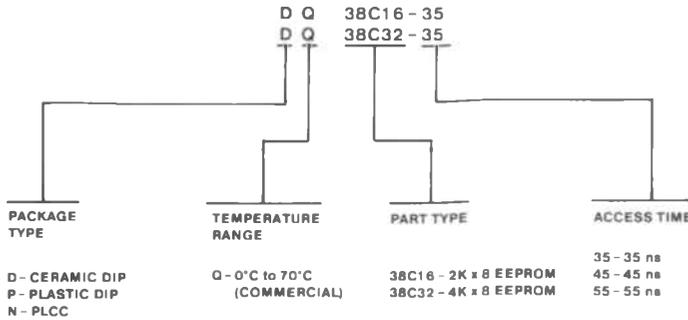
WE CONTROLLED WRITE CYCLE



CE CONTROLLED WRITE CYCLE



**Ordering Information**



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### Features

- 128K (16K x 8)
- Pin Compatible to 27128 EPROM
- Low Cost Non-Volatile Memory
- Chip Erase . . . Electrically
  - 20 seconds
- Fast Byte Write
  - 2 ms/byte
- 170 ns Access Time
  - 5 V ± 10% V<sub>CC</sub>
  - 0°C to 70°C Temperature Range
- Single High Voltage Power Supply for Write and Erase
- FLASH™ EEPROM Memory Cell Technology
  - 100 Cycle Endurance
  - 10 Years Data Retention
- JEDEC Approved Byte-wide Pin Configuration

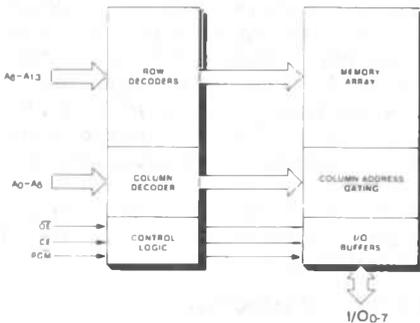
### Description

SEEQ's 48128 is a new 128K (16K x 8) memory device which combines both EEPROM and EPROM technologies to give a high density, low cost, non-volatile, Electrically Erasable Programmable Read Only Memory. The 48128 is a bulk erasable memory, and is an ideal memory device for applications with high density and infrequent in-system updates, such as program store. The 170 nsec read access time meets the performance requirements of many of today's popular microprocessors. The 48128 can be electrically erased as fast as 12 seconds. Once the chip is erased, a byte write may be performed. Only a single high voltage supply is required for chip erase or byte write.

The 48128 has two major features: first it electrically erases in seconds instead of minutes for a UV type EPROM. Before a byte can be written, the entire chip must first be erased. For the 48128, the total erasure time is **12 seconds**. This is approximately 50 times faster than an EPROM's 15 to 30 minute erasure time. Second, the 48128 has a 2 ms/byte write time, which is five times faster than the 10 msec single byte write specification of other electrically programmable non-volatile memories. Once the memory is written, data is retained for more than 10 years. Data may be read as fast as 170 nsecs over the temperature range and at worst case V<sub>CC</sub>.

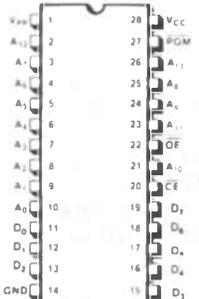
The 48128 is the first of a family. It has a double polysilicon, floating gate structure and is manufactured using n-channel technology. Erasing, like EEPROMs, is by electron tunneling while writing uses hot electron injection as in EPROMs. The cell uses a high quality SEEQ proprietary thin oxide process. This product offers the high density and low cost advantages of EPROMs as well as in-system circuit programmability of EEPROMs.

### Block Diagram

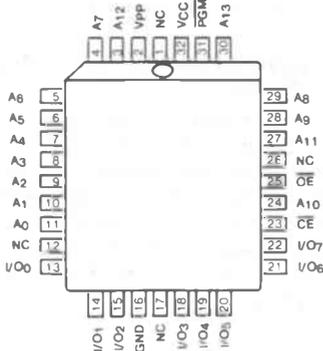


### Pin Configuration

DUAL-IN-LINE TOP VIEW



PLASTIC LEADED CHIP CARRIER TOP VIEW



### Pin Names

A <sub>0-6</sub>	ADDRESSES — COLUMN
A <sub>8-13</sub>	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
I/O <sub>0-7</sub>	DATA INPUTS/OUTPUTS
PGM	PROGRAM

# 48128 FLASH™ EEPROM

## Read

The read cycle operation is the same as EPROMs. With the chip selected and valid addresses applied, data is valid at the specified data sheet limit after the Output Enable has been valid. During a read cycle, PGM is at TTL high. The  $V_{pp}$  input is a logical don't care.

## Chip Erase

Erasure, i.e. all memory locations reset to a logic '1' state is performed by raising the  $V_{pp}$  pin to the high voltage with  $\overline{OE}$  held at a TTL high level. Address pins  $A_1$ ,  $A_2$  and  $A_0$  must also be brought to high voltage. Afterwards, either PGM or  $\overline{CE}$  will start the erasure cycle. The chip is then erased by either of the methods described in the timing diagrams. For either erasure method, the minimum and maximum  $t_{ERASE}$  time specification must be met. Long term device reliability may be affected by exceeding the maximum  $t_{ERASE}$  time.

There are three possible erasure algorithms. For the first case, all bits in the memory can be erased by applying a TTL high (or low) level to  $A_3$  for the specified  $t_{ERASE}$  time (i.e. 6 seconds), then switching to the TTL low (or high) level and held for  $t_{ERASE}$  to have complete erasure. Note that the TTL levels can be applied in either order when using this method of chip erase. A partial erasure or device damage can occur if the  $A_3$  erase timing requirements are not met.

A series of pulses may also be applied to  $A_3$  or a series of writes with  $A_1$ ,  $A_2$  and  $A_0$  at  $V_{EA}$  may be used to erase the memory. This algorithm eliminates a need for a 6 second timer to erase one memory section as in the previously described TTL level erase method. Each pulse applied partially erases the memory. To completely erase the memory, the minimum chip erase time specification (i.e.  $t_{ERASE}$ ) must be met. The number of cycles that must be applied to effectively meet the erase time will depend on the pulse width used. The number of cycles is determined by dividing the 48128's  $t_{ERASE}$  time by the lesser of  $A_3$  or PGM pulse width. It is important to note that the memory must be effectively erased for the minimum  $t_{ERASE}$  time. Consequently if a duty cycle other than 50% is used, then the number of pulses is determined by the smallest pulse width in the cycle. For example, the 48128's minimum pulse width is 90 usec and erasure time is 6 seconds.

The number of cycles is therefore 66,700 if a 250 usec and 90 usec  $A_3$  low and high pulse, respectively, is used. The maximum  $t_{ERASE}$  specification must not be exceeded by the number of cycles times the largest pulse width applied.

## Byte Write

Once the chip is fully erased, the 48128 can be programmed by applying a high voltage to the  $V_{pp}$  pin and having the  $V_{CC}$ ,  $\overline{OE}$ , and  $\overline{CE}$  pins in the proper logic states as shown in the Mode Table. A 100 usec typical PGM pulse is then applied after data is valid. The next address is then made valid and the PGM pulse is applied after new data is valid. This is repeated for all addresses which are to be written. Once all the addresses have been written, one write loop has been completed. This "address looping" write algorithm is repeated until minimum effective 2 msec (i.e. 20 loops using a 100 usec PGM pulse width) byte write time is achieved for all bytes.

In order to write to the 48128, the chip must normally be erased first. However the write mode also supports partial writing in order to further enhance the total memory programming speed and flexibility. For this mode, those memory locations which were previously in the erased state (e.g. FF Hex) need not be addressed if they will remain unprogrammed. Memory addresses are not affected by rewriting an FF (Hex). Therefore, processor time can be saved by only writing to those locations in which the data will change from the erased state.

## High Voltage Protection

The 48128 requires a single 20V power supply and has a maximum operating voltage condition of 20.5V for both the write and chip erase. There is also an absolute maximum  $V_{pp}$  voltage of 22V.

**Exceeding this 22V  $V_{pp}$  will cause damage to the device.**

It is recommended that  $V_{pp}$  and  $V_{EA}$  rise times be controlled in order to minimize overshoots. Also, a 0.1 $\mu$ F capacitor should be placed between  $V_{pp}$  and ground to further insure against overshoots during write and erase operations. If  $V_{pp}$  is toggled using a mechanical switch, a voltage de-bounce circuit must be connected between the switch and the  $V_{pp}$  pin.

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## High Voltage Recovery Time

The internal word and bit lines are charged to the high voltage  $V_{pp}$  during a chip erase or write cycle. A  $t_{wr}$  recovery time is required before a valid read cycle can begin to allow discharging from the  $V_{pp}$  level.

## Programming Equipment

Programming support is available or planned to be available from the following suppliers: Stag, Oliver Advanced Engineering, Digilec, Sunrise Electronics. The programming method in this datasheet is designed to permit in-circuit programming of the 48128.

## Mode Selection

Mode	Function (Pin)	CE (20)	OE (22)	PGM (27)	V <sub>PP</sub> (1)	A <sub>1</sub> , A <sub>2</sub> , A <sub>6</sub> (9, 8, 4)	A <sub>3</sub> (7)	V <sub>CC</sub> (28)	D <sub>0</sub> -D <sub>7</sub> (11-13,15-19)
Read		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	Address	A <sub>3</sub>	V <sub>CC</sub>	D <sub>OUT</sub>
Standby		V <sub>IH</sub>	X	X	X	X	X	V <sub>CC</sub>	HI Z
Write		V <sub>IL</sub>	V <sub>IH</sub>	TTL Pulse	V <sub>PP</sub>	Address	A <sub>3</sub>	V <sub>CC</sub>	D <sub>IN</sub>
Verify		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	Address	A <sub>3</sub>	V <sub>CC</sub>	D <sub>OUT</sub>
Chip Erase		V <sub>IL</sub>	V <sub>IH</sub>	TTL Pulse	V <sub>PP</sub>	V <sub>EA</sub>	TTL Pulse	V <sub>CC</sub>	D <sub>IN</sub> =V <sub>IH</sub>

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65°C to +150°C

Under Bias ..... -10°C to +80°C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

### V<sub>PP</sub> During Programming with

Respect to Ground ..... +22V to -0.6V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	48128-170, 48128-200 48128-250, 48128-300
V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range	(Ambient) 0°C to 70°C

# 48128 FLASH™ EEPROM

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	100	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

## DC Characteristics (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>IH</sub>	Input Leakage Current High		10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>IL</sub>	Input Leakage Current Low		-10	μA	V <sub>IN</sub> = 0.1V
I <sub>OUT</sub>	Output Leakage Current	High	10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
		Low	-10	μA	V <sub>OUT</sub> = 0.1V
V <sub>PP</sub>	V <sub>PP</sub> Program/Erase High Voltage	19.5	20.5	V	
V <sub>PP1</sub>	V <sub>PP</sub> Voltage During Read	0.0	21.5	V	
I <sub>PP</sub>	V <sub>PP</sub> Current	Standby Mode	5	mA	CE = V <sub>IH</sub> , V <sub>PP</sub> = V <sub>CC</sub> Max.
		Read Mode	5	mA	V <sub>PP</sub> = V <sub>CC</sub> Max.
		Erase Mode	30	mA	V <sub>PP</sub> = 21.5 V, PGM = V <sub>IL</sub>
		Write Mode	30	mA	V <sub>PP</sub> = 21.5 V, PGM = V <sub>IL</sub>
V <sub>EA</sub>	A <sub>1</sub> , A <sub>2</sub> , and A <sub>6</sub> Voltage During Erase	15.0	21.5	V	
I <sub>EA</sub>	A <sub>1</sub> , A <sub>2</sub> , and A <sub>6</sub> Current During Erase		50	μA	A <sub>1</sub> = A <sub>2</sub> = A <sub>6</sub> = V <sub>EA</sub> Max.
I <sub>CC1</sub>	V <sub>CC</sub> Standby Current		30	mA	CE = V <sub>IH</sub>
I <sub>CC2</sub>	V <sub>CC</sub> Active Current		100	mA	CE = OE = V <sub>IL</sub>
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +1	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

# 48128 FLASH™ EEPROM

## Capacitance<sup>[3]</sup> $T_A=25^\circ\text{C}$ , $f=1\text{ MHz}$

Symbol	Parameter	Max	Unit	Conditions
$C_{IN}$	Input Capacitance	6	pF	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Output Capacitance	10	pF	$V_{OUT} = 0\text{ V}$

## AC Test Conditions

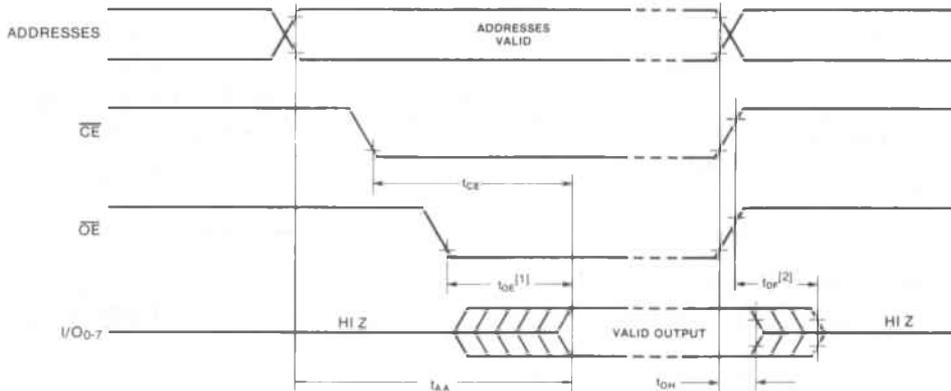
Input Rise and Fall Times (10% to 90%) . . . . . 20 ns  
 Input Pulse Levels . . . . . 0.45 V to 2.4 V  
 Input Timing Reference Level. . . 1.0 V and 2.0 V  
 Output Timing Reference Levels. . . 0.8 V and 2.0 V

## AC Characteristics

**Read Operation** (Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	Limits (ns)								Test Conditions
		48128-170		48128-200		48128-250		48128-300		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{AA}$	Address Access Time		170		200		250		300	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid		170		200		250		300	$\overline{OE} = V_{IL}$
$t_{OE}$	Output Enable to Data Valid		60		75		100		120	$\overline{CE} = V_{IL}$
$t_{DF}$	Output Enable to Output Float	0	50	0	60	0	60	0	105	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Chip Enable, Addresses, or Output Enable	0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

### READ CYCLE TIMING



**NOTES:**

- $\overline{OE}$  may be delayed up to  $t_{AA} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{AA}$
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first
- This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.

# 48128 FLASH™ EEPROM

## AC Characteristics

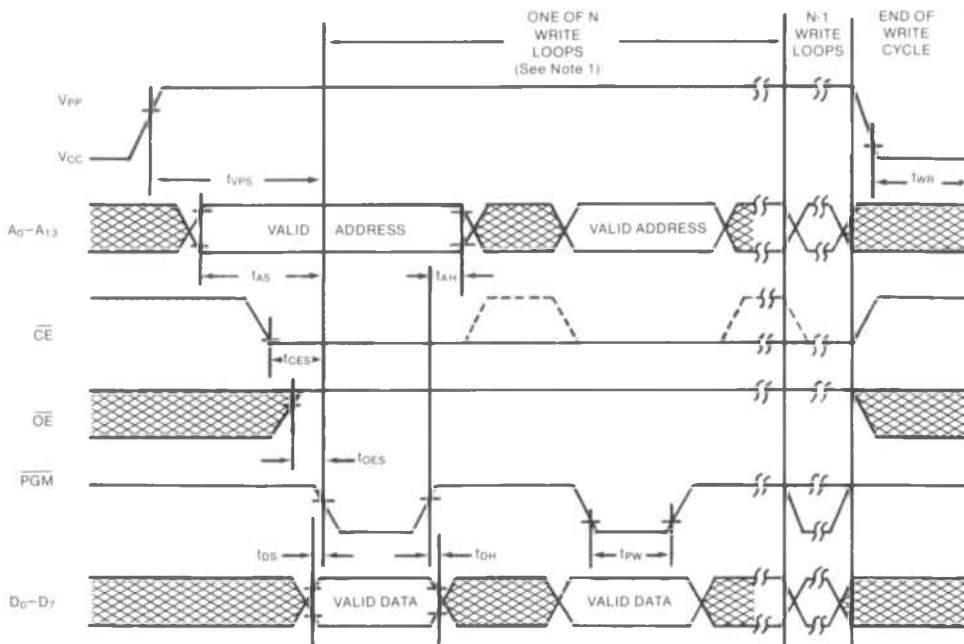
**Write Operation** (Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{wc}$	Write time per byte	2		ms
$t_{AS}$	Address Setup Time	0		ns
$t_{OES}$	Output Enable Setup Time	100		ns
$t_{CES}$	$\overline{CE}$ Setup Time	0		ns
$t_{DS}$	Data Setup Time	0		ns
$t_{VPS}$	$V_{PP}$ Setup Time	2		$\mu$ s
$t_{OEH}$	$\overline{OE}$ Hold Time	0		ns
$t_{CEH}$	$\overline{CE}$ Hold Time	0		ns
$t_{AH}$	Address Hold Time	0		ns
$t_{DH}$	Data Hold Time	0		ns
$t_{pw}$	PGM Pulse Width	90	120	$\mu$ s
$t_{wr}$	High Voltage Write Recovery Time Before A Read Cycle		2	$\mu$ s

### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and may be removed simultaneously or after  $V_{PP}$ .
- The write procedure is described under the Byte Write section in the data sheet. The number of "write loops" is given in the recommended operating conditions section. It is determined by dividing the minimum byte write time by the PGM pulse with. The minimum byte write time is 2 msec.

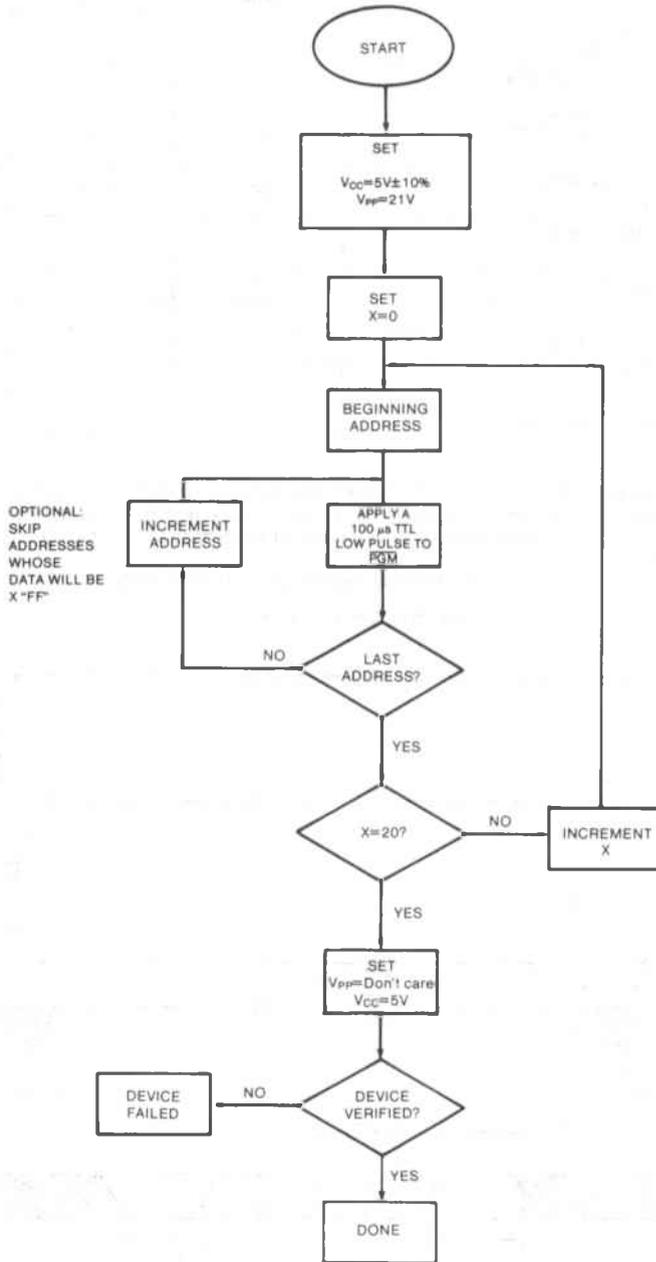
### WRITE TIMING



### NOTE:

- The 48128 requires N write loops. After N write loops, the device will be fully programmed. The value of N is a function of  $t_{pw}$ .

## Write Algorithm



# 48128 FLASH™ EEPROM

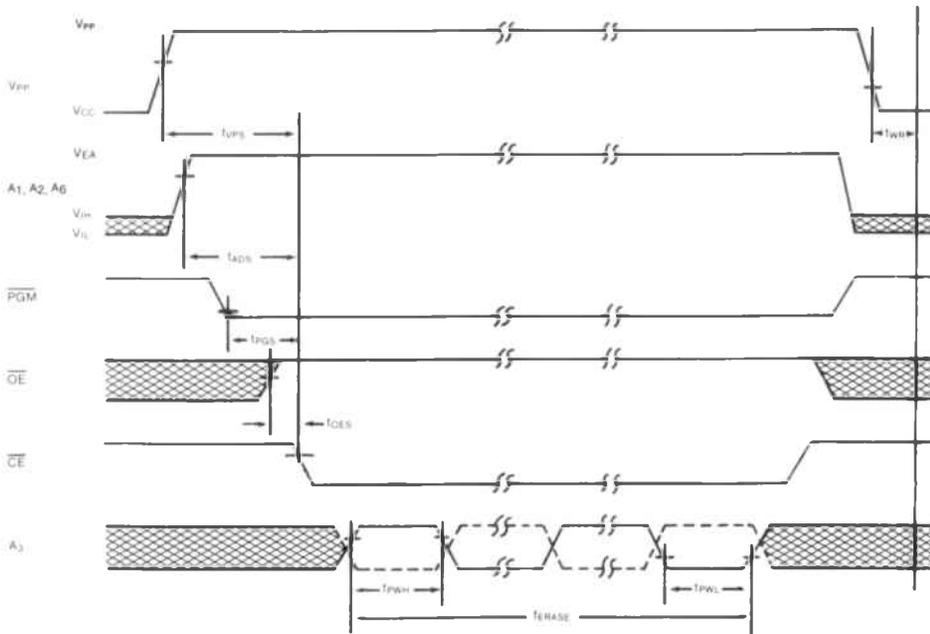
## AC Erase Characteristics Option 1

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>ERASE</sub> (note 2)	A <sub>3</sub> Total High/Low Time to Erase Memory	12	16	sec.
t <sub>ERH</sub>	A <sub>3</sub> Cumulative High Time to Erase Memory	6	8	sec.
t <sub>ERL</sub>	A <sub>3</sub> Cumulative Low Time to Erase Memory	6	8	sec.
t <sub>PWH</sub> (note 3)	A <sub>3</sub> High Pulse Width to Erase Memory	90	3 x 10 <sup>8</sup>	μs
t <sub>PWL</sub> (note 3)	A <sub>3</sub> Low Pulse Width to Erase Memory	90	3 x 10 <sup>8</sup>	μs
t <sub>PGS</sub>	PGM Setup Time	0		ns
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	2		μs
t <sub>ADS</sub>	A <sub>1</sub> , A <sub>2</sub> , A <sub>6</sub> Setup Time	2		μs
t <sub>OES</sub>	OE Setup Time	0		ns
t <sub>WR</sub>	Erase Recovery Time Before A Read Cycle		2	μs

### NOTES:

- V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, A<sub>1</sub>, A<sub>2</sub> and A<sub>6</sub> and may be removed after V<sub>PP</sub>, A<sub>1</sub>, A<sub>2</sub> and A<sub>6</sub>.
- The 48128 is erased by toggling A<sub>3</sub> between TTL levels. Both TTL low and TTL high times must meet the t<sub>PWH</sub> and t<sub>PWL</sub> specification. Total erasure occurs when the cumulative A<sub>3</sub> low time (t<sub>ERL</sub>) and cumulative A<sub>3</sub> high time (t<sub>ERH</sub>) each meet the minimum t<sub>ERASE</sub> requirement.
- The total number of pulses to A<sub>3</sub> is determined by the minimum high or low pulse width used.

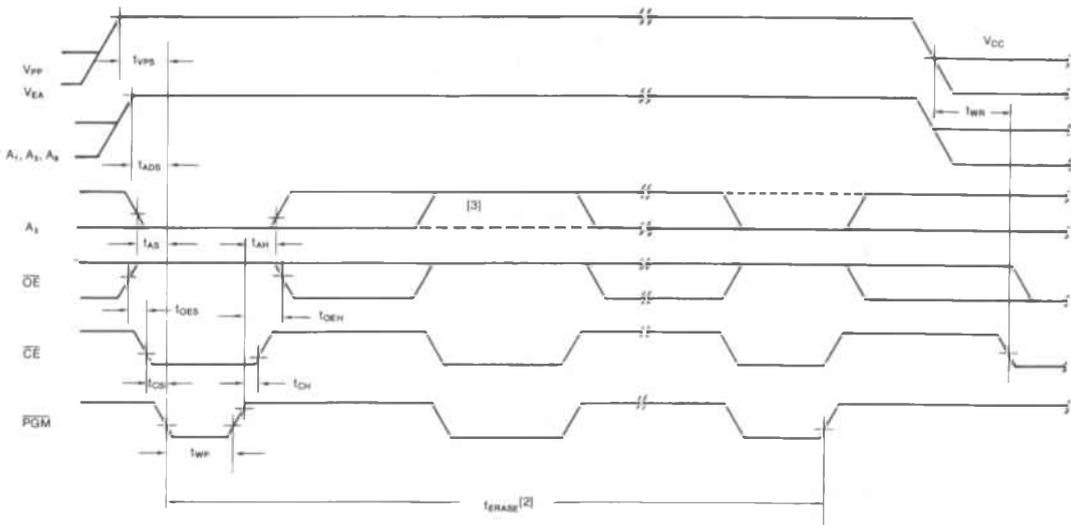
### ERASE TIMING OPTION 1



## AC Erase Characteristics — Option 2

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>ERASE</sub> (note 2)	Total PGM Low Time to Erase Memory	12	16	seconds
t <sub>ERH</sub>	Sum of PGM Pulse Widths with A <sub>3</sub> High	6	8	seconds
t <sub>ERL</sub>	Sum of PGM Pulse Widths with A <sub>3</sub> Low	6	8	seconds
t <sub>WP</sub>	PGM Pulse Width	90	3 x 10 <sup>8</sup>	μs
t <sub>CS</sub>	CE Setup Time	0		ns
t <sub>CH</sub>	CE Hold Time	0		ns
t <sub>OES</sub>	OE Setup Time	0		ns
t <sub>OEH</sub>	OE Hold Time	0		ns
t <sub>ADS</sub>	A <sub>1</sub> , A <sub>2</sub> , A <sub>6</sub> Setup Time	2		μs
t <sub>AS</sub>	A <sub>3</sub> Setup Time	0		ns
t <sub>AH</sub>	A <sub>3</sub> Hold Time	0		ns
t <sub>WR</sub>	Write Recovery Time		2	μs
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	2		μs

ERASE TIMING OPTION 2

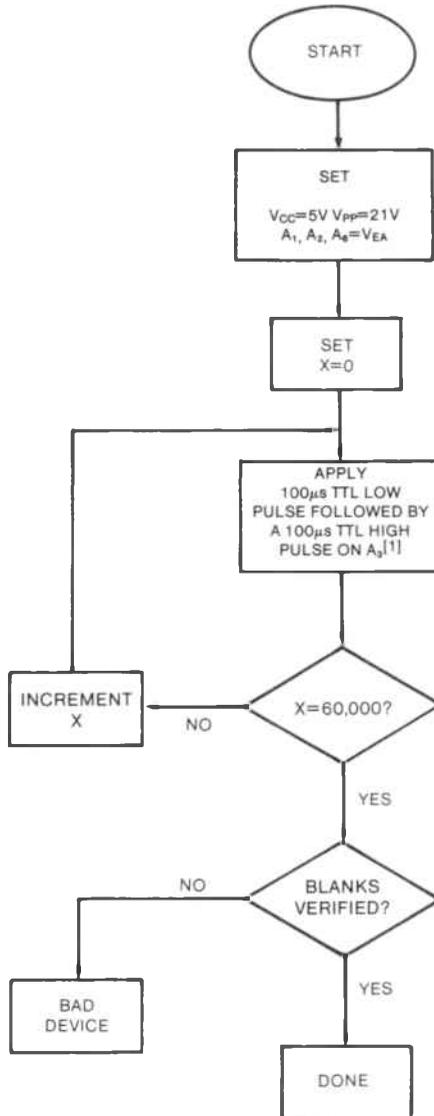


**NOTES:**

1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub>, A<sub>1</sub>, A<sub>2</sub>, and A<sub>6</sub> and removed after V<sub>PP</sub>, A<sub>1</sub>, A<sub>2</sub>, and A<sub>6</sub>.
2. The 48128 is erased when the cumulative time that PGM is low with CE low equals t<sub>ERH</sub> and t<sub>ERL</sub>.
3. A<sub>3</sub> may alternate between high and low or remain low for half the PGM cycles and high for half.
4. Addresses A<sub>4</sub>, A<sub>5</sub> and A<sub>7</sub> - A<sub>13</sub> are don't care during erase.
5. I/O<sub>0-7</sub> = V<sub>IH</sub> during erase.

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## Chip Erase Algorithm



[1] OPTIONALLY,  $\overline{PGM}$  MAY BE PULSED LOW OR MAINTAINED LOW. IF  $\overline{PGM}$  IS PULSED, IT SHOULD BE ON FOR 100µs.  $A_3$  MAY THEN BE LONGER THAN 100µs.

# 48128 FLASH™ EEPROM

## Ordering Information

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME
D - CERAMIC DIP	Q - 0°C to +70°C	18K x 8 FLASH™ EEPROM	170 - 170 ns
P - PLASTIC DIP			200 - 200 ns
N - PLCC			250 - 250 ns
			300 - 300 ns

N	Q	48128	-	170
P	Q	48128	-	170
D	Q	48128	-	170

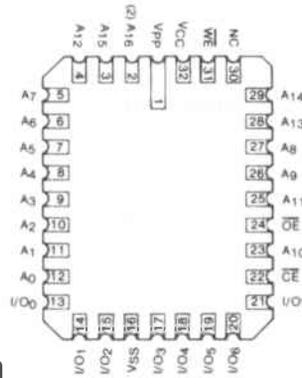


## Features

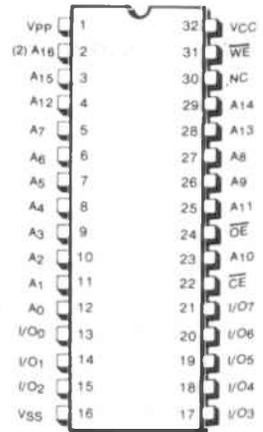
- 64K/128K Byte Writable Non-Volatile Memory
- Low Power CMOS Process
- Electrical Chip and Block Erase
  - 7.5 Second Maximum Erase Time
- Electrical Byte Write
  - 1 ms. Maximum, 500  $\mu$ s typical
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- Flash™ EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
  - Minimum 100 Cycle Endurance
  - Optional 1000 Cycle Endurance Screening
  - Minimum 10 Year Data Retention
- 5V  $\pm$  10% V<sub>CC</sub>,  
0°C to +70°C Temperature Range
- Silicon Signature™ and DiTrace™
- Jedec Standard Byte Wide Pinout
  - 32 Pin D.I.P.
  - 32 Pin J-Bend Plastic Leaded Chip Carrier

## Pin Configuration

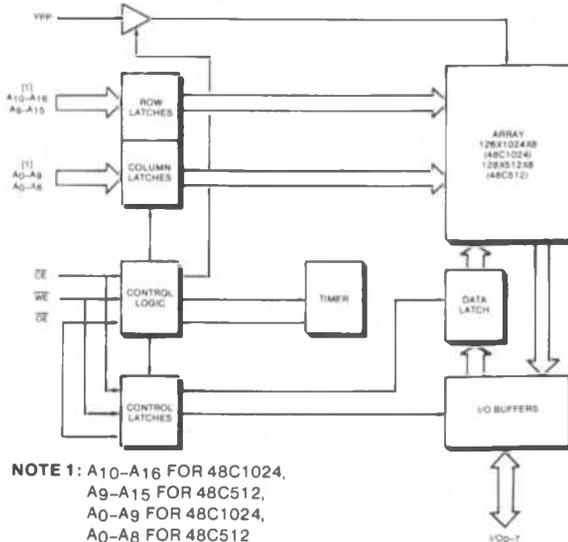
TOP VIEW  
PLASTIC LEADED CHIP CARRIER



DUAL-IN-LINE  
TOP VIEW



## Block Diagram



**NOTE 1:** A<sub>10</sub>-A<sub>16</sub> FOR 48C1024,  
A<sub>9</sub>-A<sub>15</sub> FOR 48C512,  
A<sub>0</sub>-A<sub>9</sub> FOR 48C1024,  
A<sub>0</sub>-A<sub>8</sub> FOR 48C512

**NOTE 2:** PIN 2 IS N.C. ON THE 48C512

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## Pin Names

A <sub>0</sub> -A <sub>8</sub>	COLUMN ADDRESS INPUT (48C512)
A <sub>0</sub> -A <sub>9</sub>	COLUMN ADDRESS INPUT (48C1024)
A <sub>9</sub> -A <sub>15</sub>	ROW ADDRESS INPUT (48C512)
A <sub>10</sub> -A <sub>16</sub>	ROW ADDRESS INPUT (48C1024)
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V <sub>PP</sub>	WRITE/ERASE INPUT VOLTAGE

## Description

The 48C512 and 48C1024 are 512 Kbit and 1024 Kbit CMOS Flash EEPROMS organized as 64K x 8 and 128K x 8 bits. Built using Seeq's proprietary Flash EEPROM single transistor memory cell, they feature input latches on address and data inputs for both erasing and writing, chip erase and block erase capability and a fast byte write. Endurance, the number of times a byte can be written, is specified as 100 with an optional screen to 1000 cycles.

## Read

Reading is accomplished by presenting a valid address with chip enable and output enable at  $V_{IL}$ , write enable at  $V_{IH}$ , and  $V_{PP}$  at any level. See timing waveforms for A.C. parameters.

## Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

## Block Erase

Block erase erases all bits in a block of the array to a logical one. It requires that the  $V_{PP}$  pin be brought to a high voltage and a write cycle performed. The block to be erased is defined by address inputs  $A_9$  through  $A_{15}$  for the 48C512 and  $A_{10}$  through  $A_{16}$  for the 48C1024. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time  $T_{abort}$  to allow aborting the erase by writing again. This permits recovering from an unintentional block erase if, for example, in loading a block of data a byte of 'FF' was written. After the  $T_{abort}$  delay the block erase will begin. The erase is accomplished by following the erase algorithm in figure 2.  $V_{PP}$  can

be brought to any TTL level or left at high voltage after the erase.

## Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm.  $V_{PP}$  can be brought to any TTL level or left at high voltage after the erase.

## Block and Chip Erase Algorithm

To reduce the block and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the block erase and chip erase flow charts.

## Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either block erase or chip erase.

Data are organized in these Flash EEPROMs in a group of bytes called a block. There are 128 blocks in both the 48C512 and the 48C1024. A block, which is 512 bytes in the 48C512 and 1024 bytes in the 48C1024, is conceptually like a sector on a disk drive. Individual bytes must be written as part of a block write algorithm which is detailed in figure 1. This algorithm is designed to minimize the total time to write a block of data.

Blocks are written by applying a high voltage to the  $V_{PP}$  pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of  $t_{WC}$  ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. Following each loop, a read-verification is done. If any bytes do not verify, another write loop is performed. When all bytes read correctly, additional loops are performed to insure adequate bit cell margin. The total number of loops will vary by device and depends on temperature; low temperature reduces

# 48C512/48C1024

ADVANCE DATA SHEET

EEPROMS

the number of loops required. For example, a typical (room temperature) loop count is 4. Blocks need not be written separately; the entire device or any combination of blocks can be written using the write algorithm.

Because bytes can only be written as part of a block write, if data is to be added to a partially written block or one or more bytes in a block must be changed, the contents of the block must first be read into system RAM; the bytes can then be added to the block of data in RAM and the block written using the block write algorithm.

## Power Up/Down Protection

These two devices contain a  $V_{CC}$  sense circuit which disables internal erase and write operations when  $V_{CC}$  is below 3.5 volts. In addition, erases and writes are prevented when any control input (CE, OE, WE) is in the wrong state for writing or erasing (see mode table).

## High Voltage Input Protection

The  $V_{PP}$  pin is at a high voltage for writing and erasing. There is an absolute maximum specifica-

tion which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1  $\mu$ f decoupling capacitor with good high frequency response connected from  $V_{PP}$  to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize  $V_{PP}$  voltage sag when a device goes from standby to a write or erase cycle.

## Silicon Signature™

A row of fixed ROM is present in the 48C512 and 48C1024 which contains the device's Silicon Signature™. Silicon Signature™ contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature™ is read by raising address  $A_9$  to  $12 \pm 0.5$  V. and bringing all other address inputs plus chip enable and output enable to  $V_{IL}$  with  $V_{CC}$  at 5 V. The two Silicon Signature™ bytes are selected by address input  $A_0$ . Silicon Signature™ is functional at room temperature only (25 C.)

## Silicon Signature™ Bytes

	$A_0$	Data (Hex)
Seeq Code	$V_{IL}$	94
Product code (48C512)	$V_{IH}$	1A
Product code (48C1024)	$V_{IH}$	1C

## Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$V_{PP}$	$A_9-15$ $A_{10-16}$	$A_0-8$ $A_0-9$	$D_0-7$
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	Address	Address	$D_{OUT}$
Standby	$V_{IH}$	X	X	X	X	X	Hi-Z
Byte write	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	Address	Address	$D_{IN}$
Chip erase select	$V_{IL}$	$V_{IH}$	$V_{IL}$	TTL	X	X	X
Chip erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	X	X	'FF'
Block erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	Address	X	'FF'

**DC Operating Characteristics**Over the  $V_{CC}$  and temperature range

Symbol	Parameter	Limits			Test Condition
		Min.	Max.	Unit	
$I_{IH}$	Input leakage high		1	$\mu A$	$V_{IN} = V_{CC}$
$I_{IL}$	Input leakage low		-1	$\mu A$	$V_{IN} = 0.1V$
$I_{OL}$	Output leakage		10	$\mu A$	$V_{IN} = V_{CC}$
$V_P$	Program/erase voltage	11.5	12.5	V	
$V_{PR}$	$V_{PP}$ voltage during read	0	$V_P$	V	
$I_{PP}$	$V_P$ current				
	Standby mode		200	$\mu A$	$\overline{CE} = V_{IH}, V_{PP} = V_P$
	Read mode		200	$\mu A$	$\overline{CE} = V_{IL}, V_{PP} = V_P$
	Byte write		40	mA	$V_{PP} = V_P$
	Erase		60	mA	$V_{PP} = V_P$
$I_{CC1}$	Standby $V_{CC}$ current		100	$\mu A$	$\overline{CE} = V_{CC} - .3$
$I_{CC2}$	Standby $V_{CC}$ current		5	mA	$\overline{CE} = V_{IH} \text{ min.}$
$I_{CC3}$	Active $V_{CC}$ current		60	mA	$\overline{CE} = V_{IL}$
$V_{IL}$	Input low voltage	-0.3	0.8	V	
$V_{IH}$	Input high voltage	2.0	$V_{CC} + .3$	V	
$V_{OL}$	Output low voltage		0.45	V	$I_{OL} = 2.1 \text{ ma}$
$V_{OH1}$	Output level (TTL)	2.4		V	$I_{OH} = -400 \mu A$
$V_{OH2}$	Output level (CMOS)	$V_{CC} - .4$		V	$I_{OH} = -100 \mu A$

**AC Test Conditions**Output load: 1 TTL gate and  $C(\text{load}) = 100 \text{ pf}$ .Input rise and fall times:  $< 20 \text{ ns}$ .

Input pulse levels: 0.45 V to 2.4 V

Timing measurement reference level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

**NOTE:**

In AC characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a **minimum** time; the user must provide a valid state on that input or wait for the stated minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a **maximum** time, the device will perform the operation within the stated time.

**Advance Data Sheets** contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

# 48C512/48C1024

ADVANCE DATA SHEET

EEPROMS

## Absolute Maximum Stress Ratings

Temperature:  
 Storage..... -65°C to +150°C  
 Under bias..... -10°C to +85°C  
 All Inputs except  $V_{PP}$  and  
 outputs with respect to  $V_{SS}$ ... +6 V to -0.3 V  
 $V_{PP}$  pin with respect to  $V_{SS}$ ... 14 V

## Recommended Operating Conditions

	48C512/ 48C1024
$V_{CC}$ supply voltage	5V ± 10%
Temperature range	0°C to 70°C (ambient temp.)

## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
VZAP	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note: Characterization data — not tested.

## Capacitance<sup>(1)</sup> $T_A=25^\circ\text{C}$ , $f=1\text{ MHz}$

Symbol	Parameter	Value	Test Conditions
$C_{IN}$	Input capacitance	6 pf.	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Output capacitance	12 pf.	$V_{I/O} = 0\text{ V}$

Note 1: This parameter is only sampled and not 100% tested.

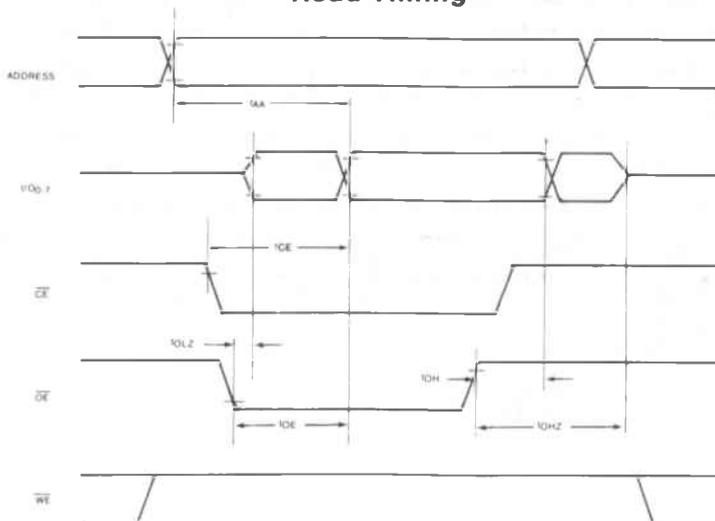
## AC Characteristics

(over the  $V_{CC}$  and temperature range)

## READ

Symbol	Parameter	48CXXX -200		48CXXX -250		48CXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read cycle time	200		250		300		ns
$t_{AA}$	Address to data		200		250		300	ns
$t_{CE}$	$\overline{CE}$ to data		200		250		300	ns
$t_{OE}$	$\overline{OE}$ to data		75		100		150	ns
$t_{DF}$	$\overline{OE}/\overline{CE}$ to data float		50		60		100	ns
$t_{OH}$	Output hold time	0		0		0		ns

## Read Timing



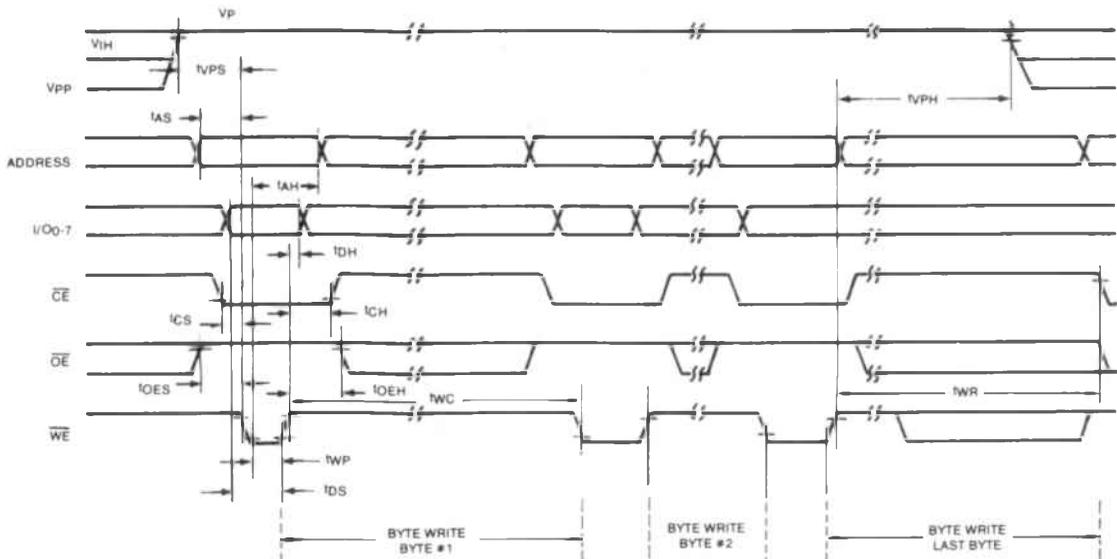
## AC Characteristics

(Over the  $V_{CC}$  and temperature range)

## BYTE WRITE

Symbol	Parameter	48CXXX -200		48CXXX -250		48CXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		2		$\mu s$
$t_{VPH}$	$V_{PP}$ hold time	250		250		250		$\mu s$
$t_{CS}$	$\overline{CE}$ setup time	0		0		0		ns
$t_{CH}$	$\overline{CE}$ hold time	0		0		0		ns
$t_{OES}$	$\overline{OE}$ setup time	10		10		10		ns
$t_{OEH}$	$\overline{OE}$ hold time	10		10		10		ns
$t_{AS}$	Address setup time	20		20		20		ns
$t_{AH}$	Address hold time	100		100		100		ns
$t_{DS}$	Data setup time	50		50		50		ns
$t_{DH}$	Data hold time	0		0		0		ns
$t_{WP}$	$\overline{WE}$ pulse width	100		100		100		ns
$t_{WC}$	Write cycle time	100	150	100	150	100	150	$\mu s$
$t_{WR}$	Write recovery time		1.5		1.5		1.5	ms

## Byte Write Timing



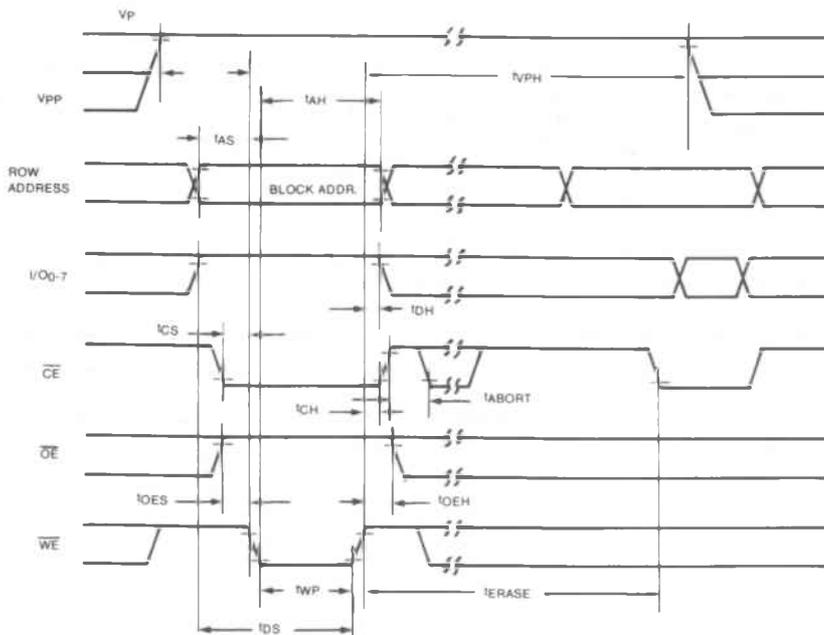
## AC Characteristics

(Over the  $V_{CC}$  and temperature range)

## BLOCK ERASE

Symbol	Parameter	48CXXXX -250		48CXXXX -300		48XXXX -350		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		2		$\mu$ S
$t_{VPH}$	$V_{PP}$ hold time	500		500		500		ms
$t_{CS}$	$\overline{CE}$ setup time	0		0		0		ns
$t_{OES}$	$\overline{OE}$ setup time	0		0		0		ns
$t_{AS}$	Address setup time	20		20		20		ns
$t_{AH}$	Address hold time	100		100		100		ns
$t_{DS}$	Data setup time	50		50		50		ns
$t_{DH}$	Data hold time	0		0		0		ns
$t_{WP}$	$\overline{WE}$ pulse width	100		100		100		ns
$t_{CH}$	$\overline{CE}$ hold time	0		0		0		ns
$t_{OEH}$	$\overline{OE}$ hold time	0		0		0		ns
$t_{ERASE}$	Block erase time		500		500		500	ms
$t_{ABORT}$	Block erase delay		250		250		250	$\mu$ S

### Block Erase Timing



## AC Characteristics

(Over the  $V_{CC}$  and temperature range)

## CHIP ERASE

Symbol	Parameter	48CXXXX -200		48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		2		$\mu$ S
$t_{VPH}$	$V_{PP}$ hold time	500		500		500		ms
$t_{CS}$	$\overline{CE}$ setup time	0		0		0		ns
$t_{OES}$	$\overline{OE}$ setup time	0		0		0		ns
$t_{DS}$	Data setup time	50		50		50		ns
$t_{DH}$	Data hold time	0		0		0		ns
$t_{WP}$	$\overline{WE}$ pulse width	100		100		100		ns
$t_{CH}$	$\overline{CE}$ hold time	0		0		0		ns
$t_{OEH}$	$\overline{OE}$ hold time	0		0		0		ns
$t_{ERASE}$	Chip erase time		500		500		500	ms

### Chip Erase Timing

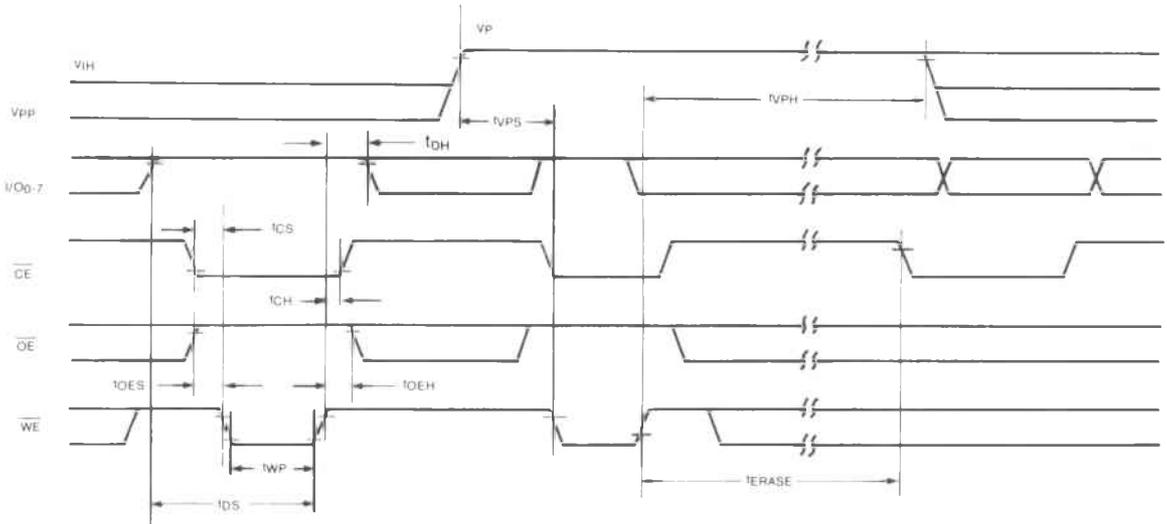


FIGURE 1  
48C512/1024 WRITE ALGORITHM

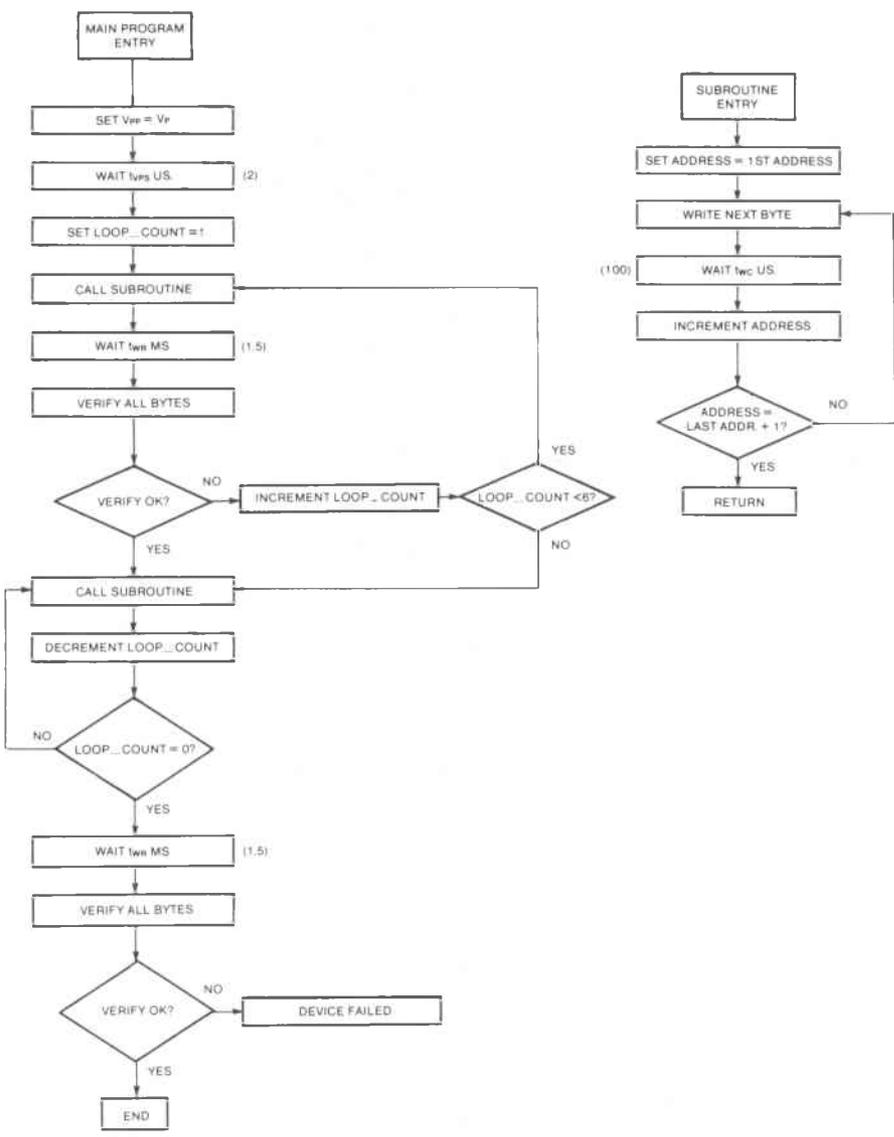


FIGURE 2  
48C512/1024  
BLOCK ERASE ALGORITHM

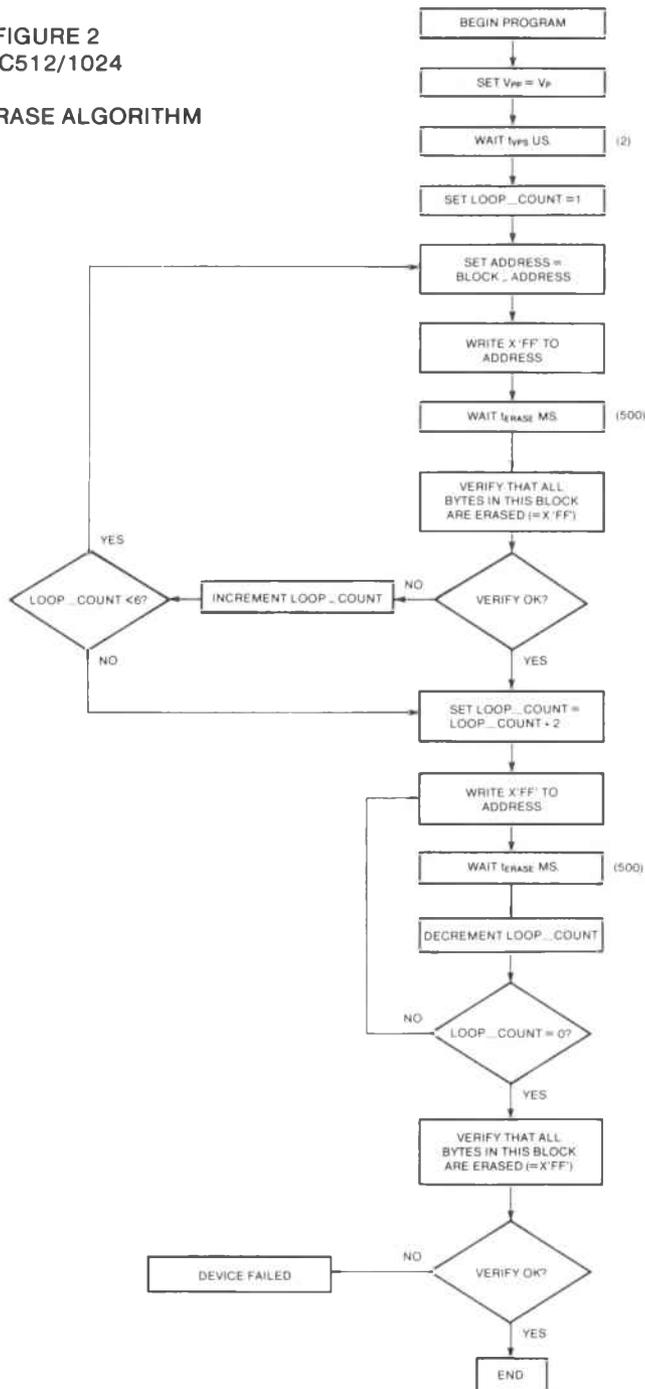
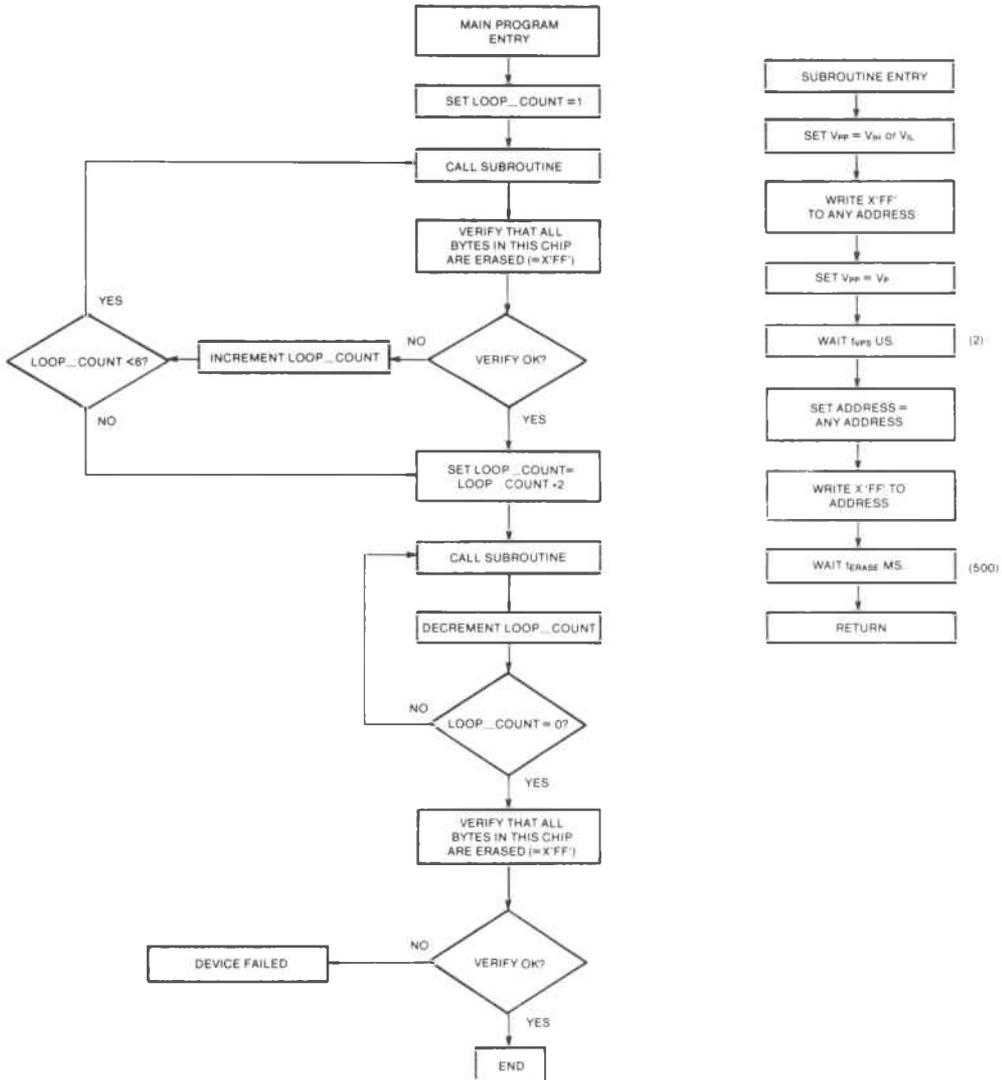


FIGURE 3  
48C512/1024

## CHIP ERASE ALGORITHM





# 2

## ***EPROMS***

(Erasable Programmable Read Only Memories)



## Features

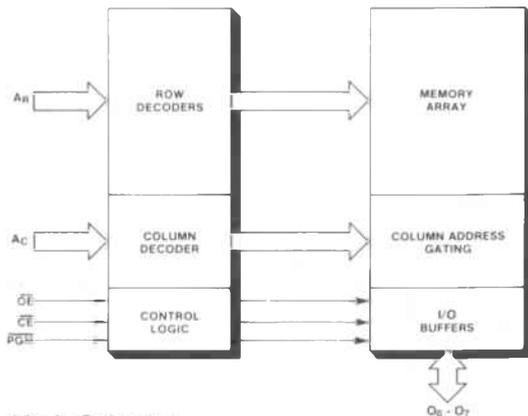
- **Fast Access Times at 0° to 70°C**
  - 2764 - 160 ns
  - 27128 - 200 ns
- **Programmed Using Intelligent Algorithm**
  - 21 V  $V_{PP}$
  - 2 Minutes for 27128
  - 1 Minute for 2764
- **JEDEC Approved Byte-wide Pin Configuration**
  - 2764 8K x 8 Organization
  - 27128 16K x 8 Organization
- **Low Power Dissipation**
  - 100 mA Active Current
  - 30 mA Standby Current
- **Military And Extended Temperature Range Available**
- **Silicon Signature™**

## Description

SEEQ's 2764 and 27128 are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are pin for pin compatible to JEDEC approved 64K and 128K EPROMs in all operational/programming modes. The devices have access times as fast as 160 ns over the 0° to 70°C temperature and  $V_{CC}$  tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 100 mA and 30 mA respectively. The fast access times allow higher system efficiency by eliminating the need for wait states in today's 8- or 16-bit microprocessors.

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to  $V_{PP}$  and a TTL "0" to pin 27 (program pin). The 2764 and 27128 may be programmed with an intelligent algorithm that is now

## Block Diagram



## Mode Selection

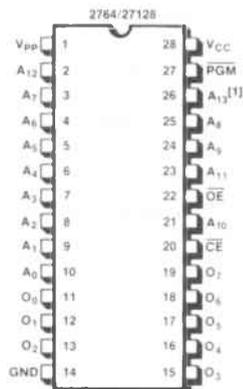
MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	PCM (27)	$V_{PP}$ (1)	$V_{CC}$ (28)	Outputs (11-13, 15-19)
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	$D_{OUT}$
Output Disable	X	$V_{IH}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	High Z
Standby	$V_{IH}$	X	X	$V_{CC}$	$V_{CC}$	High Z
Program	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{PP}$	$V_{CC}$	$D_{IN}$
Program Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	$D_{OUT}$
Program Inhibit	$V_{IH}$	X	X	$V_{PP}$	$V_{CC}$	High Z
Silicon Signature™*	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	Encoded Data

X can be either  $V_{IL}$  or  $V_{IH}$

\* For Silicon Signature™:  $A_0$  is toggled,  $A_9 = 12V$ , and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

## Pin Configuration



NOTE 1: PIN 26 IS A NO CONNECT ON THE 2764.

## Pin Names

$A_C$	ADDRESSES — COLUMN (LSB)
$A_R$	ADDRESSES — ROW
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS
PGM	PROGRAM

available on commercial programmers. The programming time is typically 5 ms/byte or 2 minutes for all 16K bytes of the 27128. The 2764 requires only half of this time, about a minute for 8K bytes. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, both EPROMs may be programmed using the

conventional 50 ms programming specification of older generation EPROMs.

Incorporated on SEEQ's EPROMs is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, the product's fab location, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

**Absolute Maximum Ratings**

Temperature

- Storage ..... -65°C to +150°C
- Under Bias ..... -10°C to +80°C

All Inputs or Outputs with

- Respect to Ground ..... +6V to -0.3V

V<sub>PP</sub> During Programming with

- Respect to Ground ..... +22V to -0.3V

Voltage on A<sub>9</sub> with

- Respect to Ground ..... +15.5V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	<b>2764</b> <b>27128</b>
V <sub>CC</sub> Supply Voltage <sup>[2]</sup>	5 V ± 10%
Temperature Range (Read Mode)	(Ambient) 0°C to 70°C
V <sub>PP</sub> During Programming	21 ± 0.5 V

**DC Operating Characteristics During Read or Programming**

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I <sub>IN</sub>	Input Leakage Current		10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>O</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
I <sub>PP</sub> <sup>[1]</sup>	V <sub>PP</sub> Current	Read Mode	5	mA	V <sub>PP</sub> = V <sub>CC</sub> Max.
		Prog. Mode	30	mA	V <sub>PP</sub> = 21.5V
I <sub>CC1</sub> <sup>[1]</sup>	V <sub>CC</sub> Standby Current		30	mA	$\overline{CE} = V_{IH}$
I <sub>CC2</sub> <sup>[1]</sup>	V <sub>CC</sub> Active Current		100	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA

**NOTES:**

1. V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

### AC Operating Characteristics During Read

Symbol	Parameter	Limits										Test Conditions
		2764-16		27XX-20		27XX-25		27XX-30		27XX-45		
		Min.	Max.									
$t_{AA}$	Address Access Time		160		200		250		300		450	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid		160		200		250		300		450	$\overline{OE} = V_{IL}$
$t_{OE}$	Output Enable to Data Valid		75		75		100		120		150	$\overline{CE} = V_{IL}$
$t_{DF}$	Output Enable to Output Float	0	60	0	60	0	60	0	105	0	130	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

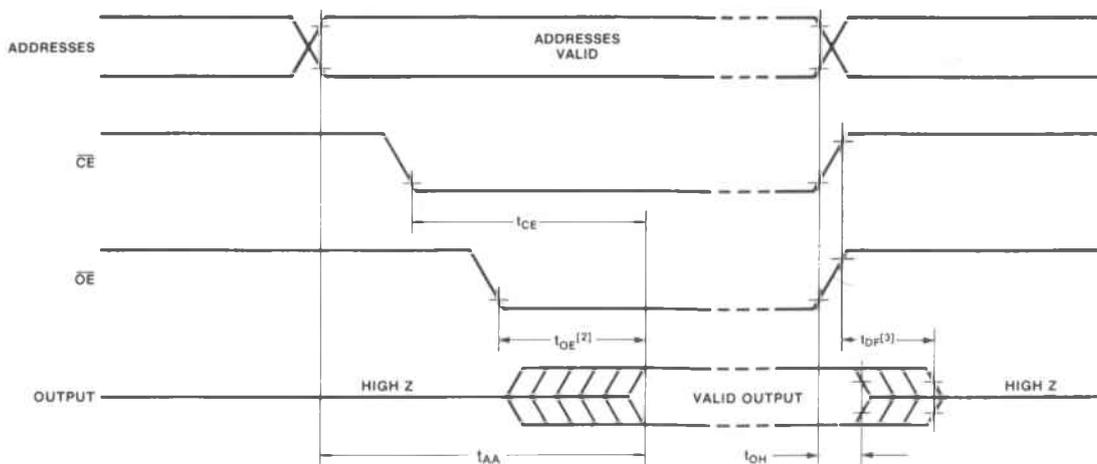
### Capacitance<sup>[1]</sup>

Symbol	Parameter	Typ.	Max.	Unit	Conditions
$C_{IN}$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

### A.C. Test Conditions

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times:  $\leq 20$ ns  
 Input Pulse Levels: 0.45V to 2.4V  
 Timing Measurement Reference Level:  
 Inputs 1V and 2V  
 Outputs 0.8V and 2V

### A.C. Waveforms



**NOTES:**

1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2.  $\overline{OE}$  MAY BE DELAYED TO  $t_{AA} - t_{OE}$  AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON  $t_{AA}$ .
3.  $t_{DF}$  IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$  WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER

**Erasure Characteristics**

The 64K and 128K EPROMs are erased using ultra-violet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm<sup>2</sup>. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

**Table 1. Typical EPROM Erasure Time**

Light Intensity (Micro-Watts/cm <sup>2</sup> )	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

**Silicon Signature™**

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer can proceed programming.

Silicon Signature is activated by raising address A<sub>9</sub> to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V<sub>CC</sub> at 5V, and having all addresses except A<sub>0</sub> at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL)

the column address A<sub>0</sub>. There are 2 bytes of data available (see Table 2). The data appears on outputs O<sub>0</sub> to O<sub>6</sub>, with O<sub>7</sub> used as an odd parity bit. This mode is functional at 25 ± 5° C ambient temperature.

**Table 2. Silicon Signature Bytes**

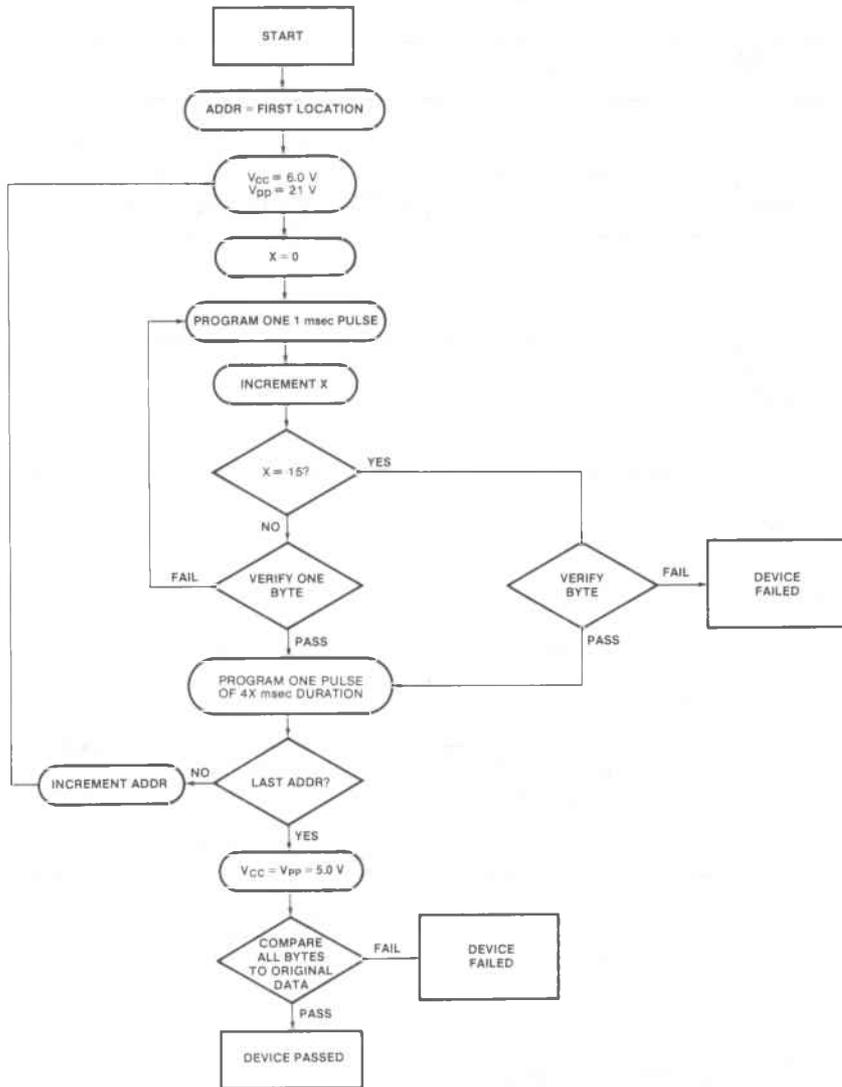
	A <sub>0</sub>	Hex Data
SEQ Code (Byte 0)	V <sub>IL</sub>	94
Product Code (Byte 1)	V <sub>IH</sub>	40
	V <sub>IH</sub>	C1

**Programming**

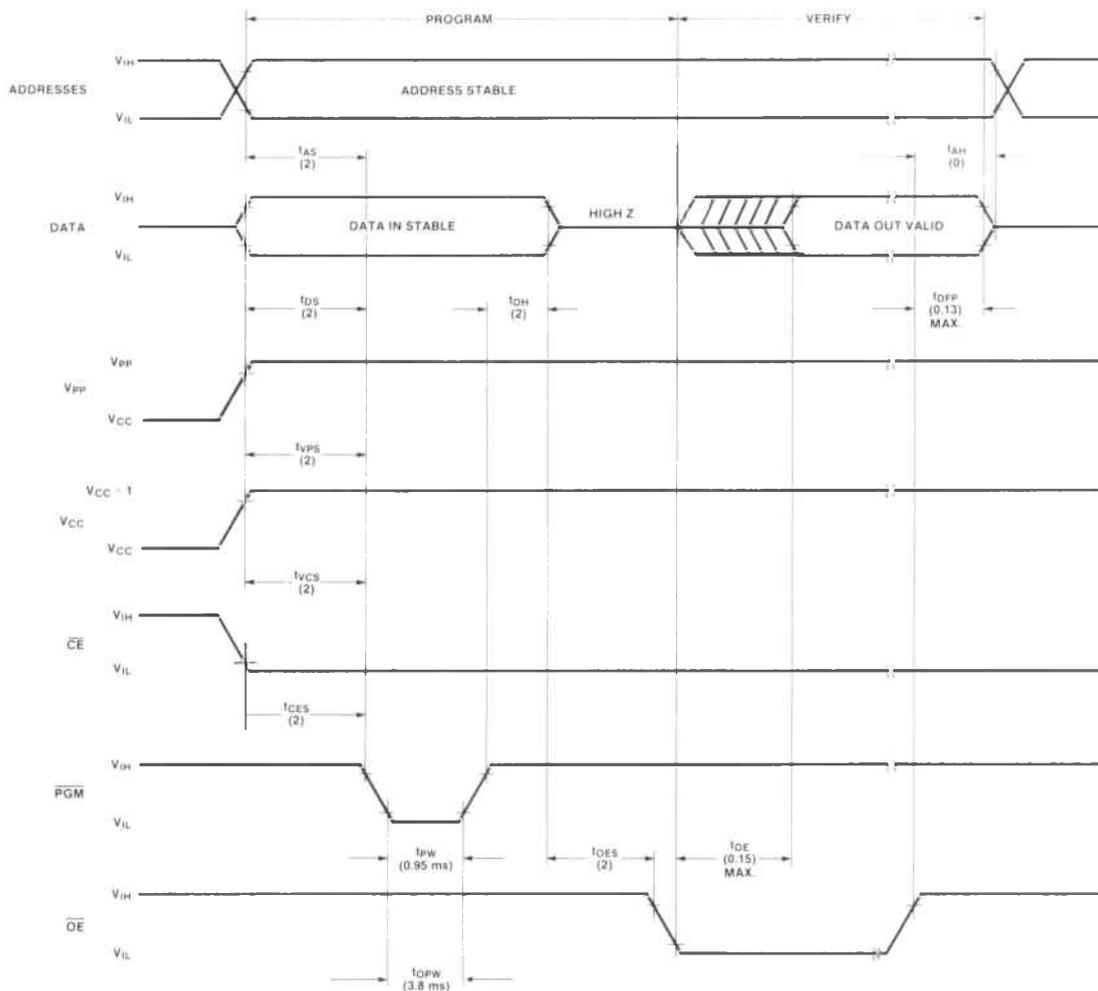
Both EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm. It typically requires only 1 and 2 minute programming time for all 64K and 128K bits respectively.

The intelligent algorithm requires V<sub>CC</sub> = 6V and V<sub>PP</sub> = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at V<sub>CC</sub> = V<sub>PP</sub> = 5V.

Intelligent Algorithm Flowchart



Intelligent Algorithm



NOTES:

- 1 ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN  $\mu$ SEC UNLESS OTHERWISE SPECIFIED.
- 2 THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A  $V_{IL}$  AND 2V FOR A  $V_{IH}$ .
- 3  $t_{OE}$  AND  $t_{DPP}$  ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

**Intelligent Algorithm**

**AC Programming Characteristics**<sup>1,4</sup>  $T_A = 25^\circ \pm 5^\circ\text{C}$ ,  $V_{CC}^{(1)} = 6.0\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 21\text{ V} \pm 0.5\text{ V}$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAS	Address Setup Time	2			$\mu\text{s}$
tOES	OE Setup Time	2			$\mu\text{s}$
tDS	Data Setup Time	2			$\mu\text{s}$
tAH	Address Hold Time	0			$\mu\text{s}$
tDH	Data Hold Time	2			$\mu\text{s}$
tDFP	Output Enable to Output Float Delay	0		130	ns
tVPS	VPP Setup Time	2			$\mu\text{s}$
tVCS	VCC Setup Time	2			$\mu\text{s}$
tpw <sup>2</sup>	PGM Initial Program Pulse Width	0.95	1.0	1.05	ms
topw <sup>3</sup>	PGM Overprogram Pulse Width	3.8		63	ms
tCES	CE Setup Time	2			$\mu\text{s}$
tOE	Data Valid from OE			150	ns

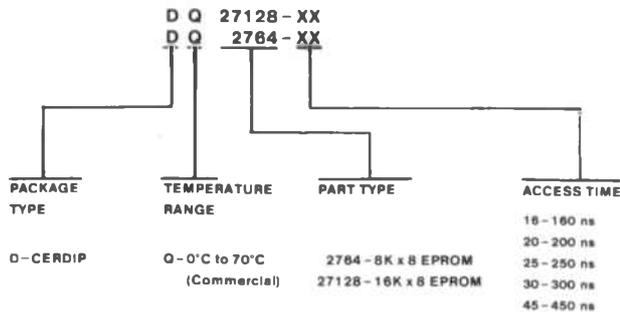
**NOTES:**

1. VCC must be applied simultaneously or before VPP and removed simultaneously or after VPP.
2. Initial Program Pulse width tolerance is 1 msec  $\pm$  5%.
3. The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
4. For 50 ms programming, VCC = 5 V  $\pm$  5%, TPW = 50 ms  $\pm$  10%, and Topw is not applicable.

**AC Test Conditions**

Input Rise and Fall Times (10% to 90%) ..... 20 ns  
 Input Pulse Levels ..... 0.45V to 2.4V  
 Input Timing Reference Level ..... 0.8V and 2.0V  
 Output Timing Reference Level ..... 0.8V and 2.0V

**Ordering Information**





## Features

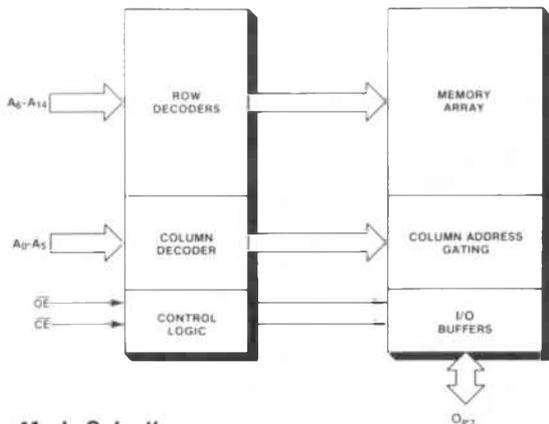
- **256K (32K x 8) CMOS EPROM**
- **Ultra Low Power**
  - 100  $\mu$ A Max.  $V_{CC}$  Standby Current
  - 40 mA Max. Active Current
- **Programmed Using Intelligent Algorithm**
  - 12.5 V  $V_{pp}$
- **200 ns Access Times**
  - 5 V  $\pm$  10%  $V_{CC}$
  - 0° to 70°C Temperature Range
- **Minimum 10 Year Data Retention**
- **JEDEC Approved Byte-wide Pin Configuration**
- **Silicon Signature™**
- **Military And Extended Temperature Range Available.**

## Description

SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its 40 mA active current is less than one half the active power of n-channel EPROMs. In addition the 100  $\mu$ A  $V_{CC}$  standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

The 27C256 is specified over the 0° to 70°C temperature range and at 5 V  $\pm$  10%  $V_{CC}$ . The access time is specified at 200 ns, making the 27C256 compatible with most of today's microprocessors. Its inputs and outputs are completely TTL compatible.

## Block Diagram



## Pin Configuration



## Mode Selection

MODE	PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$V_{PP}$ (1)	$V_{CC}$ (28)	Outputs (11-13, 15-19)
Read		$V_{IL}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	$D_{OUT}$
Output Disable		X	$V_{IH}$	$V_{CC}$	$V_{CC}$	High Z
Standby		$V_{IH}$	X	$V_{CC}$	$V_{CC}$	High Z
Program		$V_{IL}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	$D_{IN}$
Program Verify		$V_{IH}$	$V_{IL}$	$V_{PP}$	$V_{CC}$	$D_{OUT}$
Program Inhibit		$V_{IH}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	High Z
Silicon Signature™*		$V_{IL}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	Encoded Data

X can be either  $V_{IL}$  or  $V_{IH}$ .

\* For Silicon Signature™  $A_0$  is toggled,  $A_9 = 12$  V, and all other addresses are at a TTL low.

Silicon Signature™ is a registered trademark of SEEQ Technology.

## Pin Names

$A_0 - A_5$	ADDRESSES — COLUMN (LSB)
$A_6 - A_{14}$	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5 V  $V_{PP}$  and an initial chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

## Absolute Maximum Ratings

### Temperature

Storage .....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Under Bias .....  $-10^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$

### All Inputs or Outputs with

Respect to Ground .....  $+6\text{ V}$  to  $-0.3\text{ V}$

$V_{PP}$  with Respect to Ground .....  $+14.0\text{ V}$  to  $-0.3\text{ V}$   
Voltage on  $A_9$  with

Respect to Ground .....  $+14.0\text{ V}$  to  $-0.3\text{ V}$

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

27C256-20, 27C256-25, 27C256-30, 27C256-45.	
$V_{CC}$ Supply Voltage <sup>[1]</sup>	5 V $\pm$ 10%
Temperature Range (Read Mode)	(Ambient) $0^{\circ}\text{C}$ to $70^{\circ}\text{C}$
$V_{PP}$ During Read <sup>[2]</sup>	$V_{CC}$
$V_{PP}$ During Programming <sup>[3]</sup>	$12.5 \pm 0.3\text{ V}$

## DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
$I_{IN}$ <sup>[4]</sup>	Input leakage		1	$\mu\text{A}$	$V_{IN}=V_{CC}$ Max.
$I_O$ <sup>[5]</sup>	Output leakage		10	$\mu\text{A}$	$V_{OUT}=V_{CC}$ Max.
$I_{PP}$	$V_{PP}$ current: Standby mode Read Mode Programming mode		150 1 30	$\mu\text{A}$ mA mA	$\overline{CE}=V_{CC}-1\text{ v. min.}$ $F=5\text{ MHz}$ , $\overline{CE}=V_{IL}$ $V_{PP}=12.5\text{ v.}$
$I_{CC1}$	$V_{CC}$ standby current		100	$\mu\text{A}$	$\overline{CE}>=V_{CC}-1\text{ v.}$
$I_{CC2}$	$V_{CC}$ standby current		1.5	mA	$\overline{CE}=V_{IH}$
$I_{CC3}$	$V_{CC}$ active current		40	mA	$\overline{CE}=\overline{OE}=V_{IL}$ , $O_0-\gamma=0$ , $F=5\text{ MHz}$ .
$V_{IL}$	Input low voltage	-0.1	0.8	V	
$V_{IH}$	Input high voltage	2.0	$V_{CC} + 1$	V	
$V_{OL}$	Output low voltage		0.45	V	$I_{OL}=2.1\text{ ma.}$
$V_{OH}$	Output high voltage	2.4		V	$I_{OH}=-400\text{ }\mu\text{A.}$

### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- $V_{PP}$  cannot be left floating and should be connected to  $V_{CC}$  during read.
- 0.1  $\mu\text{F}$  ceramic capacitor on  $V_{PP}$  is required during programming only, to suppress voltage transients.
- Inputs only. Does not include I/O.
- For I/O only.

**AC Characteristics Read Operation** (Over Operating Temperature And  $V_{CC}$  Range, Unless Otherwise Specified)

Symbol	Parameter	Limits								Units	Test Conditions
		27C256-20		27C256-25		27C256-30		27C256-45			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
$t_{AA}$	Address Access Time		200		250		300		450	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$t_{CE}$	Chip Enable Access Time		200		250		300		450	ns	$\overline{OE}=V_{IL}$
$t_{OE}$	Output Enable Access Time		75		100		120		150	ns	$\overline{CE}=V_{IL}$
$t_{DF}$	Output or Chip Enable off To Output Float <sup>3)</sup>		60		60		105		130	ns	$\overline{CE}=V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		0		ns	$\overline{CE}=\overline{OE}=V_{IL}$

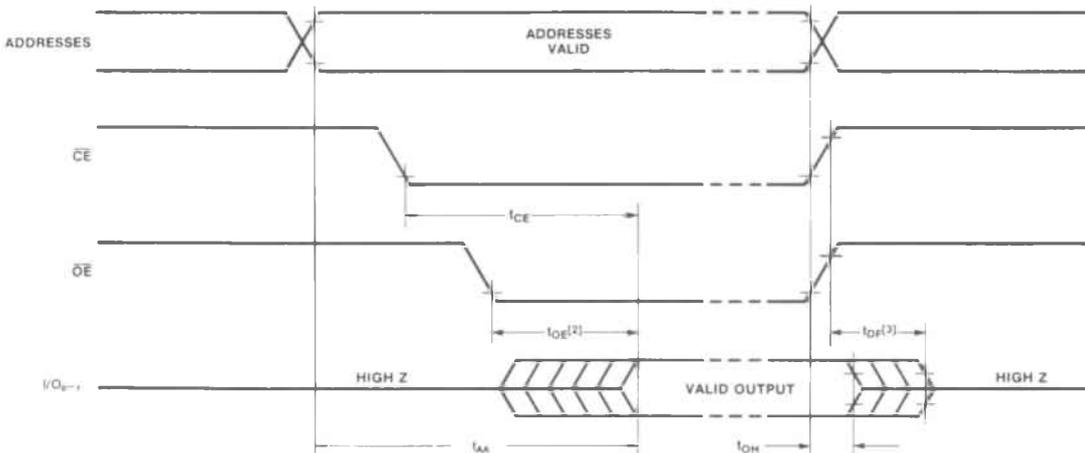
**Capacitance**

Symbol	Parameter	Typ.	Max.	Unit	Conditions
$C_{IN}$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

**A.C. Test Conditions**

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times:  $\leq 20$ ns  
 Input Pulse Levels: 0.45V to 2.4V  
 Timing Measurement Reference Level:  
 Inputs 1V and 2V  
 Outputs 0.8V and 2V

**A.C. Waveforms**



**NOTES:**

1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED
2.  $\overline{OE}$  MAY BE DELAYED TO  $t_{AA} - t_{OE}$  AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON  $t_{AA}$ .
3.  $t_{DF}$  IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$ , WHICHEVER OCCURS FIRST.

### Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity  $\times$  exposure time, for erasure is a minimum of 15 watt-second/cm<sup>2</sup>. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm <sup>2</sup> )	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

### Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A<sub>9</sub> to

12V  $\pm$  0.5V, bringing chip enable and output enable to a TTL low, having V<sub>CC</sub> at 5V, and having all addresses except A<sub>0</sub> at a TTL low. The Silicon Signature data is then accessed by toggling A<sub>0</sub>. The data appears on outputs O<sub>0</sub> to O<sub>6</sub>, with O<sub>7</sub> used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

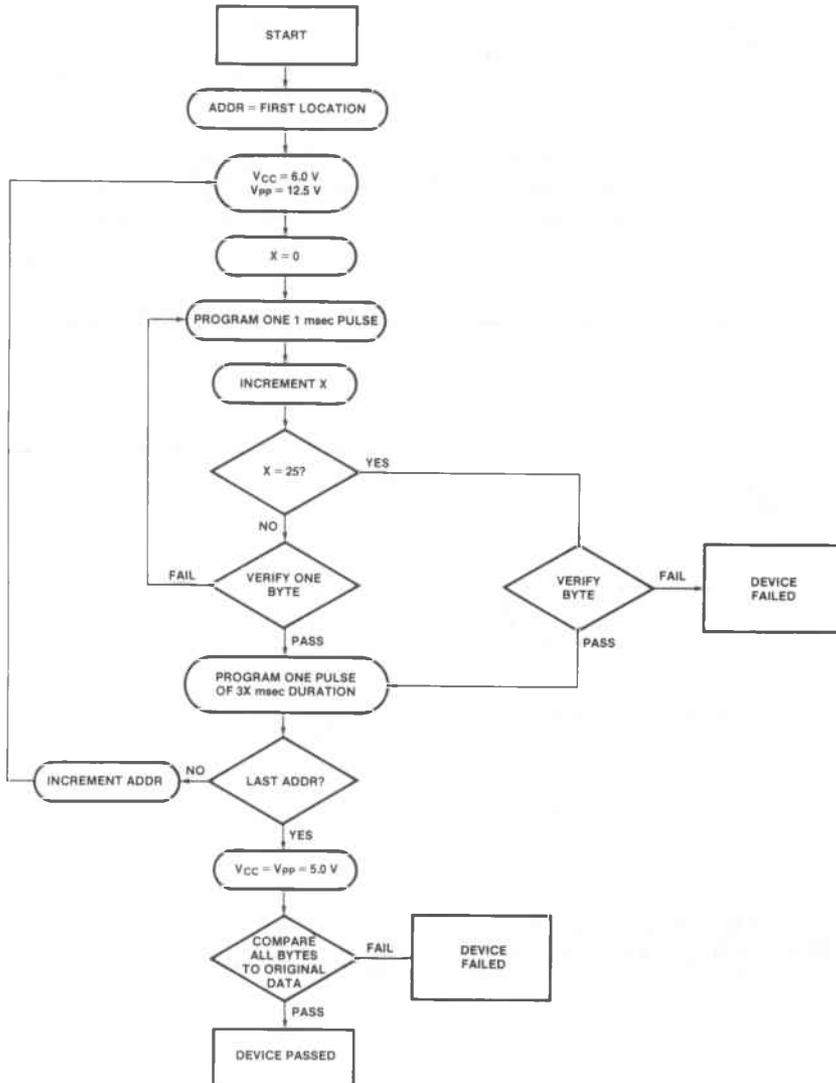
	A <sub>0</sub>	Data (Hex)
SEEQ Code (Byte 0)	V <sub>IL</sub>	94
Product Code (Byte 1)	V <sub>IH</sub>	C2

### Programming

The 27C256 is programmed using the industry standard intelligent algorithm.

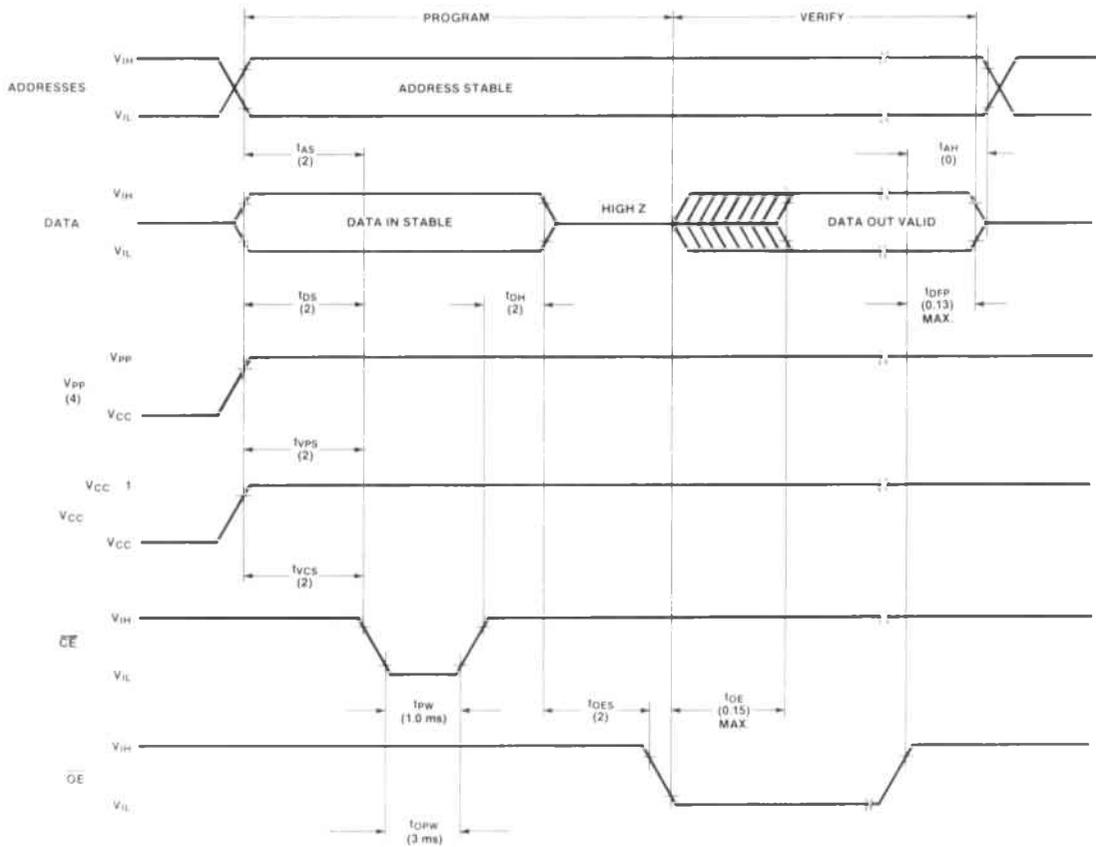
The intelligent algorithm requires V<sub>CC</sub> = 6 V and V<sub>PP</sub> = 12.5 V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X overpulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at V<sub>CC</sub> = V<sub>PP</sub> = 5 V.

Intelligent Algorithm Flowchart



EPROMS

**Intelligent Algorithm**



**NOTES:**

1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN  $\mu$ SEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A V<sub>IL</sub> AND 2 V FOR A V<sub>IH</sub>.
3. t<sub>OE</sub> AND t<sub>ODP</sub> ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
4. 0.1  $\mu$ F CERAMIC CAPACITOR ON V<sub>pp</sub> IS REQUIRED DURING PROGRAMMING ONLY, TO SUPPRESS VOLTAGE TRANSIENTS.

**Intelligent Algorithm**

**AC Programming Characteristics**  $T_A = 25^\circ \pm 5^\circ\text{C}$ ,  $V_{CC}^{[1]} = 6.0\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 12.5\text{V}$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tAS	Address Setup Time	2			$\mu\text{S}$
tOES	$\overline{\text{OE}}$ Setup Time	2			$\mu\text{S}$
tDS	Data Setup Time	2			$\mu\text{S}$
tAH	Address Hold Time	0			$\mu\text{S}$
tDH	Data Hold Time	2			$\mu\text{S}$
tDFP	Output Enable to Output Float Delay	0		130	ns
tVPS	$V_{PP}$ Setup Time	2			$\mu\text{S}$
tVCS	$V_{CC}$ Setup Time	2			$\mu\text{S}$
tpw	$\overline{\text{CE}}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
tOPW <sup>[2]</sup>	$\overline{\text{CE}}$ Overprogram Pulse Width	2.85		78.75	ms
tOE	Data Valid from $\overline{\text{OE}}$			150	ns

EPROMS

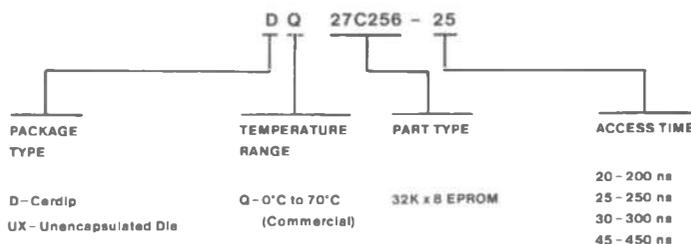
**AC Conditions of Test**

Input Rise and Fall Times (10% to 90%) . . . . . 20 ns  
 Input Pulse Levels . . . . . 0.45 V to 2.4 V  
 Input Timing Reference Level . . . . . 0.8 V and 2.0 V  
 Output Timing Reference Level . . . . . 0.8 V and 2.0 V

**NOTES:**

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

**Ordering Information**





# 3

## ***MICRO/DATA COM***

(Microcomputers/Data Communications)



## Features

- On Chip 5V EEPROM Program Memory: 2K x 8
- Write to EEPROM Instruction allows processor to load and alter its own program memory
- EEPROM programmable externally as well as under processor control
- EEPROM programming instruction can program external EEPROM
- On Chip Static Ram: 256 x 8
- Silicon Security™ lock to prevent external access to user code and data
- Silicon Signature™ and DiTrace™
- TMS 7000 Microlanguage Processor Architecture
- High Speed Clock Rates:
  - 10 MHz for 72720-10
  - 16 MHz for 72720-16

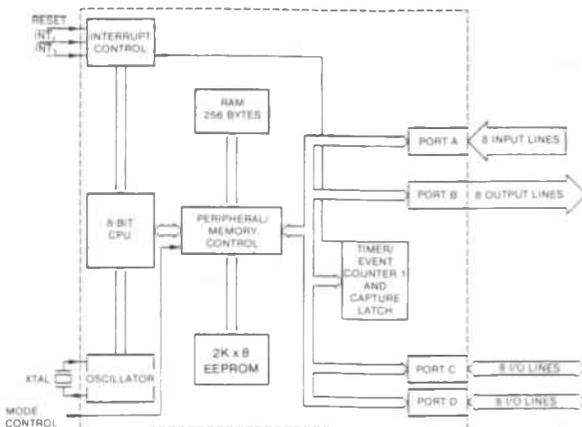
## Description

The Seeq 72720 is a full function single chip microcomputer fabricated in N channel silicon gate technology which contains a non-volatile electrically erasable EEPROM program memory. This program memory can be erased and programmed via the processor itself during normal program execution or can be programmed under external control as if it were a standard 5V EEPROM memory component. The EEPROM can easily be expanded off chip using the processor's Full Expansion Mode. External EEPROM can be programmed with the same instruction used to alter on chip EEPROM.

A Silicon Security™ lock mechanism is implemented in EEPROM which allows the user's program to inhibit external access to its proprietary program code. Once activated this lock can be reset only by a EEPROM Block Clear operation which erases the entire program memory contents.

As with other EEPROM devices which SEEQ manufactures, the 72720 has Silicon Signature™ and DiTrace™ features to facilitate production testing and tracking. Each device is encoded with detailed processing and testing results which are stored in a special EEPROM memory as it passes through the manufacturing cycle. Also stored is an unalterable identification code which contains such information as mask revision and EEPROM programming parameters.

## Functional Block Diagram



## EEPROM Microcomputer Applications Summary

The availability of a single chip microcomputer with non-volatile program memory which can be altered under processor control makes possible the design of a variety of low cost products with many new features including:

- SELF ADAPTIVE CODE for machines that learn as they perform their tasks.
- IN-CIRCUIT REPROGRAMMABILITY to eliminate product disassembly for firmware updates and diagnostics.
- REMOTE REPROGRAMMABILITY to eliminate service calls for firmware modifications.

MICRO/  
DATA COM

- DATA LOGGING of factory test results, product configuration, revision level, service records, product usage, and product errors.
- STORED INITIALIZATION PARAMETERS to eliminate front panel switches and automatically configure product for one or many users.
- CODE AND DATA SECURITY to protect proprietary programs and confidential data.

### Silicon Security™

The combination of EEPROM Program Memory with a single chip microcomputer provides unique possibilities for the design of highly secure yet

adaptable computer and control systems. When all program code exists on chip, instructions do not appear on the I/O pins of the processor (as they do on any system where CPU and Program Memory are separate) making the code externally invisible. Also when instruction fetches occur only from on chip memory, instructions cannot be forced on the processor externally causing it to dump the contents of internal registers or memory. The 72720 provides for security by allowing the processor to lock itself in the Single Chip mode preventing external access but allowing the processor complete read/write access to all memory including EEPROM.

### Pin Descriptions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
A <sub>0</sub> (LSB)	6	I	Data input
A <sub>1</sub>	7	I	Data input
A <sub>2</sub>	8	I	Data input
A <sub>3</sub>	9	I	Data input
A <sub>4</sub>	10	I	Data input
A <sub>5</sub>	16	I	Data input
A <sub>6</sub>	15	I	Data input
A <sub>7</sub>	11	I	Data input
B <sub>0</sub>	3	O	Data output
B <sub>1</sub>	4	O	Data output
B <sub>2</sub>	5	O	Data output
B <sub>3</sub>	37	O	Data output
B <sub>4</sub> /ALATCH	38	O	Data output/Memory interface address latch strobe
B <sub>5</sub> /R/W	1	O	Data output/Memory interface Read/Write signal
B <sub>6</sub> /ENABLE	39	O	Data output/Memory interface enable strobe
B <sub>7</sub> /CLKOUT	2	O	Data output/Memory interface clock
C <sub>0</sub>	28	I/O	Port C is bidirectional data port. In Peripheral Expansion, Full Expansion, and Microprocessor modes, Port C is a multiplexed low address and data bus.
C <sub>1</sub>	29	I/O	
C <sub>2</sub>	30	I/O	
C <sub>3</sub>	31	I/O	
C <sub>4</sub>	32	I/O	
C <sub>5</sub>	33	I/O	
C <sub>6</sub>	34	I/O	
C <sub>7</sub>	35	I/O	
D <sub>0</sub>	27	I/O	Port D is bidirectional data port. In Full Expansion and Microprocessor modes, Port D is the high address bus.
D <sub>1</sub>	26	I/O	
D <sub>2</sub>	24	I/O	
D <sub>3</sub>	23	I/O	
D <sub>4</sub>	22	I/O	
D <sub>5</sub>	21	I/O	
D <sub>6</sub>	20	I/O	
D <sub>7</sub>	19	I/O	
INT <sub>1</sub>	13	I	Highest priority maskable, software programmable interrupt
INT <sub>3</sub>	12	I	Lower priority maskable, software programmable interrupt
RESET	14	I	Device reset
MC	36	I	Mode control pin
XTAL <sub>2</sub> /CLKIN	17	I	Crystal input for control of internal oscillator
XTAL <sub>1</sub>	18	O	Crystal output for control of internal oscillator
V <sub>CC</sub>	25		Supply voltage
V <sub>SS</sub>	40		Ground reference

Security is also enhanced because program data is stored in the EEPROM in the form of electrical charges hidden under metal gates on the die which makes visual or electronic determination of bit patterns extremely difficult if not impossible. Finally, since program memory is non-volatile yet alterable, programs can be written which alter themselves in response to equipment tampering to confuse the would be product copier.

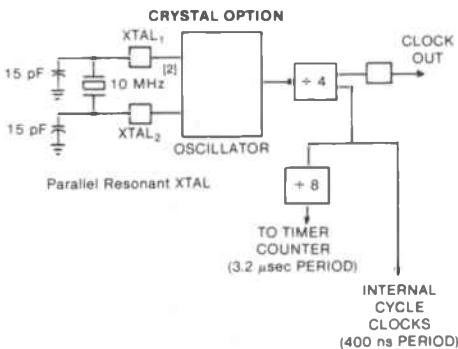
The oscillator frequency is divided by four on the 72720 to generate both an internal machine cycle clock and an external clock which is output on I/O Port line B<sub>7</sub> when the processor is placed in one of its expansion modes. All instructions execute in multiples of this machine cycle clock as described under INSTRUCTION SET. The internal cycle clock is further divided by eight to provide a clock input to the on chip timer prescaler.

## Functional Description

### Oscillator and Clocks

The 72720 operates synchronously to internal clocks which can be generated either by the on chip oscillator or an externally supplied square wave. To operate using the on chip oscillator, a parallel resonant crystal is connected to the XTAL<sub>1</sub> and XTAL<sub>2</sub> input pins.

Each of these inputs must have a small high frequency filter capacitor to ground to guarantee reliable oscillator startup. To operate using an externally supplied clock, the XTAL<sub>1</sub> pin is left open and XTAL<sub>2</sub> is driven by a TTL level square wave. Required high and low time and allowable frequency range for this input are specified under AC CHARACTERISTICS.

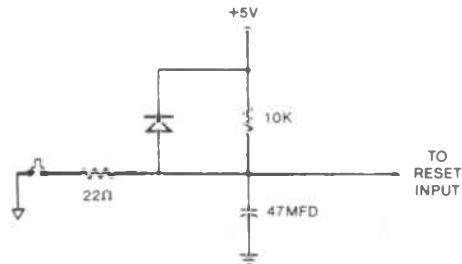


OSCILLATOR AND CLOCK CIRCUITS  
FIGURE 1

NOTE:  
1. 2-16MHz for 72720-16  
2. 18MHz for 72720-16

### Reset

Reset is a hardware initialization input which can be treated as a non-maskable highest priority interrupt. The RESET input pin must be active low at power on and must be held low until a minimum of 100 microseconds after the power supply is within specified operating range to guarantee proper initialization. Reset can be applied asynchronously to the processor clock and is recognized immediately on assertion. It is recommended that the timing and sequence specified in the RESET TIMING diagram be followed to eliminate program disturb.



RECOMMENDED RESET CIRCUIT  
FIGURE 2

The application of Reset causes the following to occur immediately:

1. Ports C and D are placed in the high impedance input mode.
2. All bits of Port B are set to one.

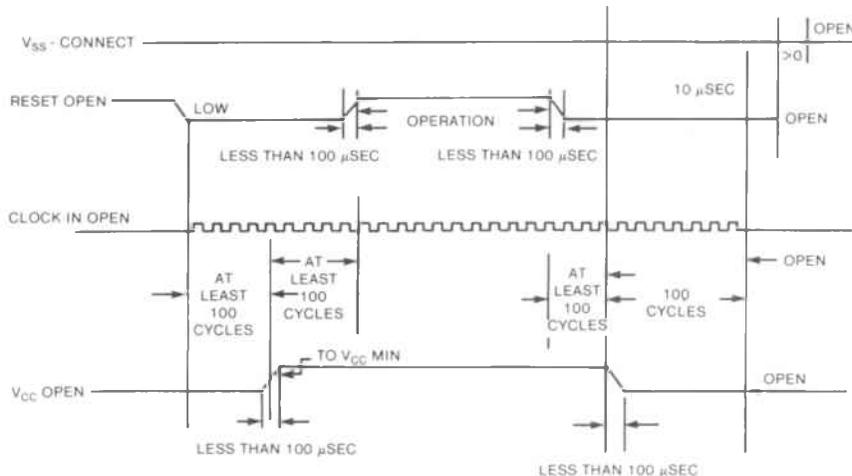
After Reset is removed and before execution of the first instruction the following occurs:

1. The I/O Control and Status Registers are cleared to zero. (Single Chip mode—Interrupts disabled)
2. The Program Counter is saved in the A and B Registers.
3. The Stack Pointer is initialized to 01.

4. The Reset Vector is fetched from Program Memory locations FFFE/FFFF and placed in the Program Counter.

The Interrupt Flags of the I/O Control Register have indeterminate values after Reset. It is recommended that they be cleared before interrupts are enabled.

**72720**  
**RECOMMENDED POWER UP/DOWN SEQUENCE**



**FIGURE 3**

**Interrupts**

The 72720 has four hardware interrupt sources and levels as follows:

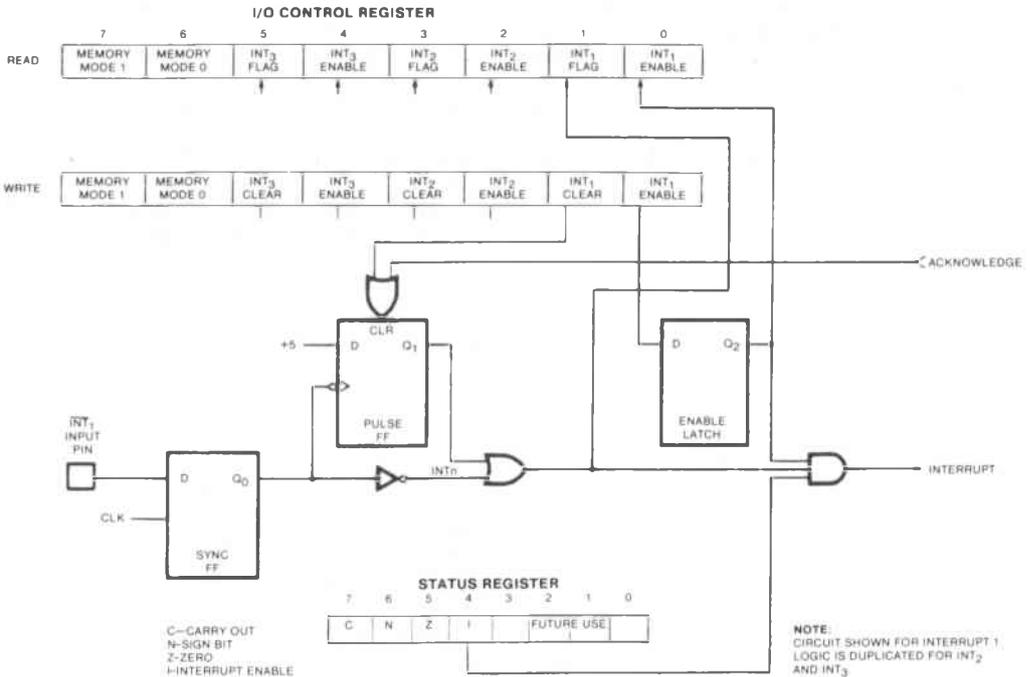
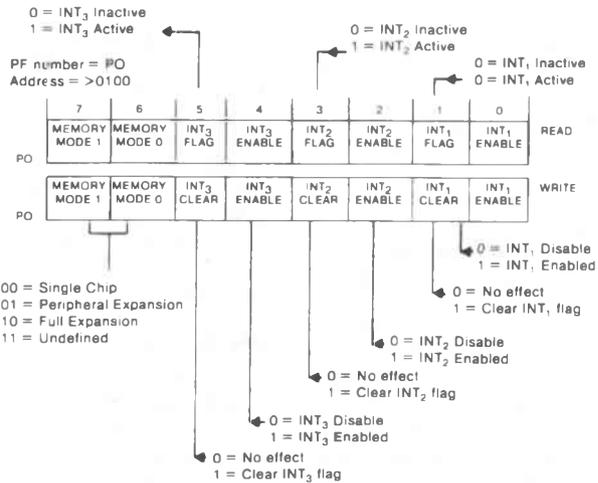
Level	Source	Priority
0	Reset	Highest
1	External 1	
2	Timer	
3	External 2	Lowest

The external interrupts consist of three input lines:  $\overline{RESET}$ ,  $\overline{INT}_1$ , and  $\overline{INT}_3$ . These interrupts are activated by a low level or pulse on the corresponding pin and require no external synchronization. External interrupt inputs must be held low for five oscillator (1.25 machine) cycles to be detected. Interrupt level 2 is asserted internally upon rollover of the on chip Timer/Counter.

Each interrupt source (except Reset) can be individually enabled and disabled via Interrupt

Enable bits in the I/O Control Register in the Peripheral File (see figure 4). Writing a '1' to an Interrupt Enable bit enables the Interrupt, while '0' disables it. All interrupts with the exception of Reset, can be globally disabled via an Interrupt Enable bit (bit 4) in the CPU's Status Register.

The status of each interrupt request can be tested even if the interrupt is disabled by reading the appropriate Interrupt Flag bit in the I/O Control Register. These flag bits will indicate the presence of a previously latched and unserviced interrupt pulse input or the presence of a current interrupt level input. Writing a '1' to the Interrupt Clear bit clears the corresponding Interrupt flag, while a '0' has no effect on the bit. The active low level inputs allow for collector ORing of several interrupts at one input pin.



INTERRUPT LOGIC DIAGRAM

FIGURE 4

Normal interrupt processing occurs as follows:

1. Interrupt input is applied.
2. Input is sampled, latched, and the appropriate Interrupt Flag is set.
3. If the global and specific Interrupt Enable bits are set the interrupt request is passed to the interrupt priority logic.
4. The priority logic continuously compares the priority level of the request to others pending and applies a vector associated with the highest currently pending to the CPU along with an interrupt request signal.
5. The CPU completes its currently executing instruction and then executes a modified sub-routine call to the appropriate interrupt service routine. The CPU then responds with an interrupt acknowledge signal which is directed via the priority logic to reset the appropriate interrupt input pulse latch.

The vector which is supplied by the priority logic is used to select the appropriate two byte sub-routine pointer stored in the upper 48 bytes of system memory. Nineteen (19) machine cycles occur between the completion of the currently executing instruction and the beginning of the first instruction of the interrupt service routine. This time is reduced to 17 cycles if the CPU is executing an IDLE (wait for interrupt) instruction at the time the interrupt occurs.

As a part of the call to the interrupt service routine the CPU pushes the current Program Counter on the Stack and also pushes the Status Register then zeroes its contents (including the global Interrupt Enable bit). Interrupts are thus disabled for the duration of the service routine and are re-enabled by the Return from Interrupt instruction RETI. If interrupts are to be allowed during the execution of an interrupt service routine, the user's program must set the Interrupt Enable bit in the Status Register after the routine has been entered.

### Mode Control

The 72720 can be placed in several different modes consisting of both normal operating modes alterable during program execution and non-alterable modes entered only at Reset.

The normal operating modes consisting of Single Chip, Peripheral Expansion, and Full Expansion are enabled by holding the MC (Memory Mode Control) pin at  $V_{IL}$  during Reset. For normal operation the MC pin can be permanently tied to GND. The modes are latched at the rising edge of Reset.  $MC=V_{IL}$  at Reset initializes the processor in the Single Chip mode. Once in this mode, either the Peripheral Expansion or Full Expansion modes can be entered under program control by writing to the Memory mode bits of the I/O Control Register in the Peripheral File (address 0100H).

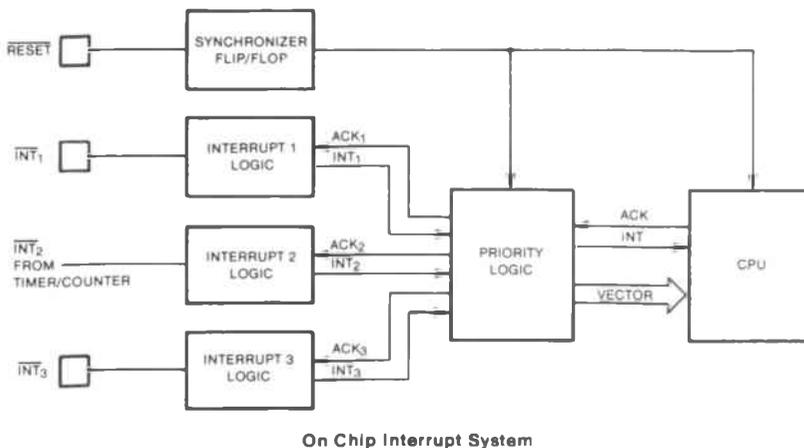


FIGURE 5

## I/O Control Register

	Bit 7	Bit 6
Single Chip Mode	0	0
Peripheral Expansion	0	1
Full Expansion Mode	1	0

The Microprocessor mode is an operating mode which is entered at Reset with the MC pin at  $V_H$  and three I/O pins held as indicated in the figure 6. This initialization can be inconvenient to perform in-circuit but can be done once out of circuit then permanently locked using the Silicon Security™ lock feature of the 72720.

The external EEPROM Programming mode is entered at Reset with the MC,  $A_4$  and  $A_7$  pins held at  $V_{IH}$ . Once this mode is entered, pin  $A_7$  acts as programming pulse control line and  $A_4$  becomes a Read/Write control line.

**MODE LOCK-** The MODE LOCK feature allows the three normal operating modes and the microprocessor mode to be permanently locked. Once the desired mode has been entered, MODE LOCK is achieved by writing a one (via a PRG instruction) to bit 0 and bit 7 of the Security Lock Register in the Peripheral File (all other bits = 0). Other bits in this EEPROM register should normally be written with zeroes as they are reserved for other functions. MODE LOCK can be removed by entering the BLOCK CLEAR MODE.

**BLOCK CLEAR-** The Block Clear mode erases all EEPROM memory including the Security Lock Register. The Mode is entered at Reset with MC at  $V_H$  and three I/O pins  $B_2$ ,  $A_4$ ,  $A_7$  at  $V_{IH}$  as shown. Block Clear mode should be maintained for at least 100 milliseconds and can be operated indefinitely. Block Clear is terminated by Resetting into another mode. A second BLOCK CLEAR is required to clear the Security Register if the SECURITY LOCK has been set. See Block Clear Mode Timing for details.

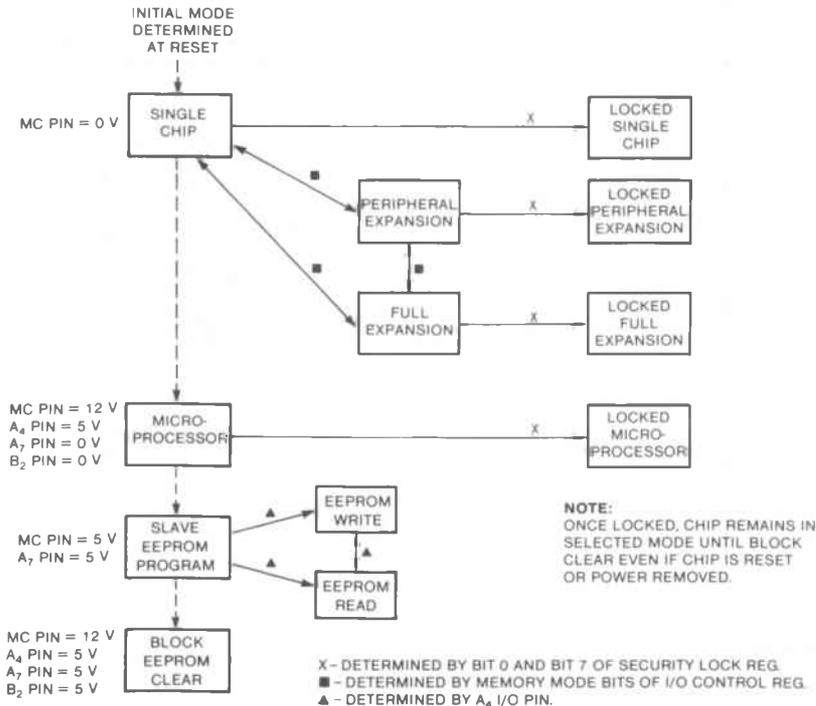


FIGURE 6

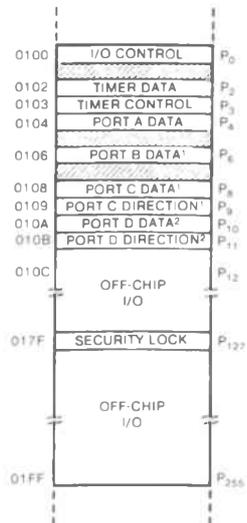
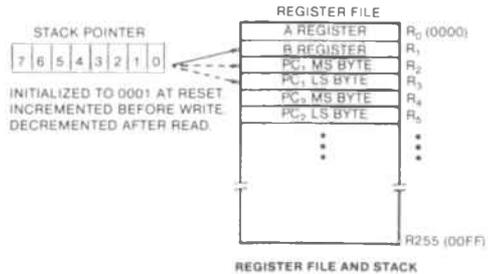
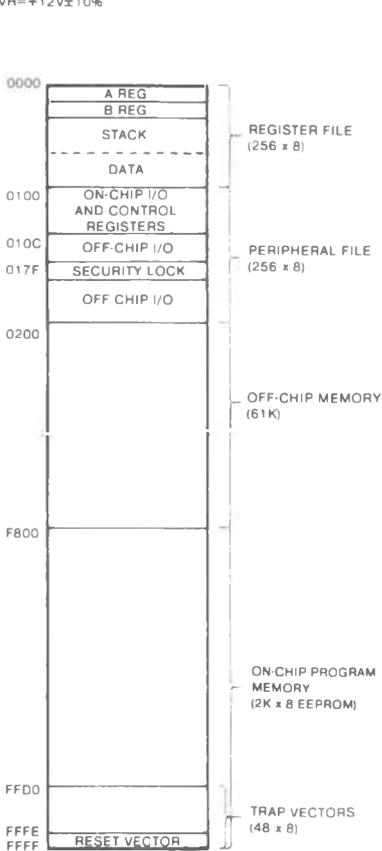
Mode	Pin Voltages at Reset				I/O Control Register	
	MC	B2*	A4	A7	BIT 7	BIT 6
Single Chip	V <sub>IL</sub>				0	0
Peripheral Expansion	V <sub>IL</sub>				0	1
Full Expansion	V <sub>IL</sub>				1	0
Microprocessor	V <sub>H</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>		
Slave Prog/Verify EEPROM	V <sub>IH</sub>		V <sub>IH</sub>	V <sub>IH</sub>		
Slave Verify EEPROM	V <sub>IH</sub>		V <sub>IL</sub>	V <sub>IH</sub>		
Block Clear EEPROM	V <sub>H</sub>	V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>		

\*NOTE: Pin B<sub>2</sub> should be driven thru a 5K resistor  
 NO ENTRY INDICATES DON'T CARE  
 V<sub>H</sub> = +12V ± 10%

## Memory Address Space

The 72720 has a single 64K byte address space divided into three basic areas: a Register File, a Peripheral File, and Memory.

**REGISTER FILE-** The Register File resides in the lower 256 bytes of system memory. The Register File contains the A Register (Accumulator), the B Register (a secondary accumulator and index register) and 254 general purpose registers. The Stack resides in the Register File and is accessed via a separate 8 bit Stack Pointer Register. The Register File resides entirely on chip.



- NOTES:
- UPPER HALF OF P<sub>6</sub>, P<sub>8</sub>, and P<sub>9</sub> BECOME PART OF OFF-CHIP I/O EXPANSION SPACE IN PERIPHERAL AND FULL EXPANSION MODES.
  - P<sub>10</sub> and P<sub>11</sub> ALSO BECOME PART OF I/O EXPANSION SPACE IN FULL EXPANSION MODE

**PERIPHERAL FILE**—The Peripheral File occupies the next 256 locations above the Register File and contains all on-chip I/O ports within the first 11 locations. The remaining 245 locations can be used to access off-chip I/O ports and peripherals in the Peripheral Expansion mode.

For details of the various registers in the Peripheral File see the following sections:

I/O Control—see **INTERRUPTS** and **MODE CONTROL**

Timer Data/Timer Control—see **TIMER COUNTER**

Port Data/Port Direction—see **INPUT/OUTPUT**

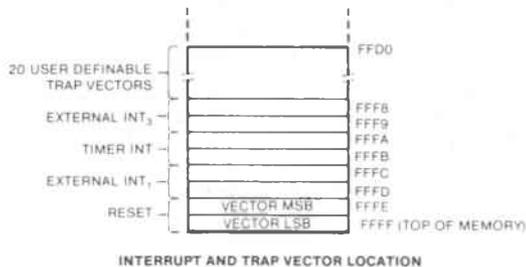
Security Lock—see **SILICON SECURITY LOCK**

**MEMORY**—The remainder of the 64K address space is general purpose memory for storage of both programs and data. In the 72720 the upper 2K bytes exist on chip as EEPROM which serves to store programs, constants, and for non-volatile storage of infrequently varying data. The remainder of the address space is available in the Full Expansion mode for any type of memory or I/O.

The upper 48 bytes (FFD0-FFFF) of the memory address space can be used to store up to 24 two byte address vectors which are used by 24 special TRAP instructions (TRAP0-TRAP23). A TRAP instruction is a subroutine call instruction which substitutes a vector fetched from the TRAP vector table at the top of memory for the two byte direct address of a CALL instruction. The TRAP instruction is therefore a more code efficient form of the CALL for frequently used subroutines.

**MACHINE REGISTERS**—There are three user visible registers in the 72720 which are not a part of the 64K memory address space;

1. A 16 bit Program Counter
2. An 8 bit Stack Pointer
3. An 8 bit Status Register



## Instruction Set

The 72720 shares the standard instruction set of the TMS7000 MicroLanguage Processor family which consists of 61 different instructions to which has been added the PRG EEPROM programming instruction. The instruction set includes: direct support for BCD arithmetic with Decimal Add and Decimal Subtract on packed BCD bytes, single instruction I/O operations on bit fields from one to eight bits via the Peripheral File logical instructions, masked bit test and jump instructions that function on both I/O and memory, and an 8 x 8 multiply of any two registers in the Register File. Several double byte operations are provided including load immediate to register pair and move register pair to register pair.

72720 addressing modes include three byte direct addressing allowing direct register to register operations bypassing the Accumulator, 16 bit indirect addressing to the entire 64K address space using any register pair in the Register File, and 16 bit direct addressing indexed with the B Register.

For full details and examples of the use of the 72720 instruction set see the Texas Instruments TMS7000 Assembly Language Programmer's Guide.

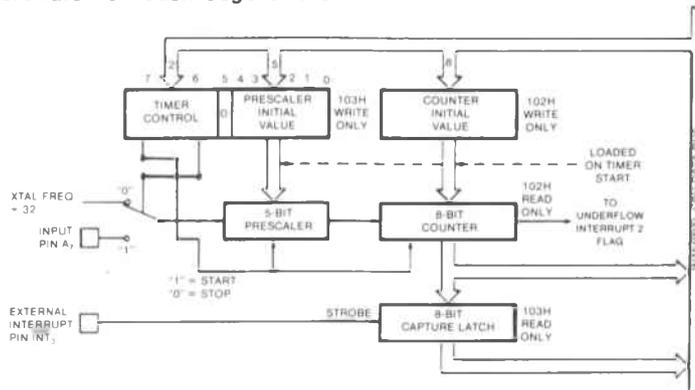
## Timer/Counter

The programmable Timer/Counter on board the 72720 consists of a modulo-eight binary down counter and a 5 bit clock prescaler counter both of which are programmable. The Timer Counter can be started and stopped via bit 7 of the Timer Control Register in the Peripheral File ("1" = start, "0" = stop). Each time a one is written to this start bit (whether the bit was previously a one or not) the Contents of a Prescaler Initial Value Register and a Counter Initial Value Register are loaded into the prescaler and counter; then decrementing begins. Counter underflow generates an interrupt level 2 pulse and sets the associated flag in the I/O Control Register. Underflow also automatically initiates reload of the counter from the Counter Initial Value Register (but allows the prescaler to continue running in order to maintain accuracy over long periods of time) to provide unattended generation of periodic events. The counter clock source is controlled by bit 6 in a Timer Control Register. A "1" specifies an internal clock which is

the oscillator frequency divided by 32 (resulting in a 3.2 microsecond period at 10MHz) and a "0" selects an external source which the user applies to I/O pin A<sub>7</sub>. A zero to one transition on A<sub>7</sub> decrements the prescaler. The maximum clock frequency which can be applied to A<sub>7</sub> is the oscillator frequency divided by 32 and the minimum high or low pulse width must be at least 1.25 machine cycles. The Counter also has associated with it an 8 bit Capture Latch which can be used to instantaneously save the counter value in response to an external level 3 interrupt input. This feature facilitates the measurement of input pulse width and also provides a means of measuring and compensating for variable interrupt response times. Pulse width measurement is accomplished by loading the capture latch on each edge of the

pulse and comparing the difference. Interrupt response time (latency) can be determined by an interrupt service routine, if the interrupt loads the capture latch, by subtracting the content of the Capture Latch from the current counter value.

There are only two Peripheral File locations associated with the Timer/Counter—Timer Data (location 0102H) and Timer Control (location 0103H). A write to Timer Data loads the Counter Initial Value and read fetches the Current Counter Value. Likewise a write to Timer Control loads the Prescaler Initial Value bits 0-4, the Start bit 7 and the clock Source bit 6 (bit 5 is not used and should be loaded with "0"). A read of Timer Control returns the contents of the Capture Latch.



**PROGRAMMABLE TIMER/EVENT COUNTER**  
**FIGURE 7**

**Input/Output**

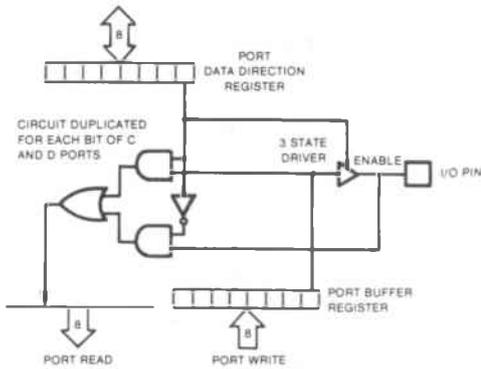
In the Single Chip mode the 72720 provides 32 I/O lines configured as four 8 bit ports A, B, C, and D. A Port is input only, B Port is output only, and both C and D Ports are fully bidirectional (programmable as inputs or outputs on a bit by bit basis). Ports C and D are configured by writing to Data Direction Registers in the Peripheral File.

**A PORT** – All eight lines of A Port are high impedance TTL level compatible input lines with internal pullup resistors to V<sub>CC</sub> of approximately 30K ohms. The most significant bit of A Port A<sub>7</sub> can also serve as a clock input to the on chip Timer/Counter. Inputs are not latched and a read

of the port returns the state of the A Port pins. Input data is sampled approximately two machine cycles before the end of an I/O instruction.

**B PORT** – All eight lines of B Port are latched TTL level compatible push/pull outputs capable of driving two standard TTL loads. A read of the B Port returns the state of the B Port pins which should reflect the contents of the port's output latch.

**C and D PORT** – Ports C and D are identical 8 bit input/output ports. Each port has associated with it a Data Direction Register which determines whether each bit in the port is in input or output mode and a Buffer Register which holds data to be output.



**Bidirectional I/O Port Control**

**FIGURE 8**

All four registers are addressable as part of the Peripheral File. A "1" bit in a Data Direction Register causes the corresponding I/O pin to be an output while a "0" makes it a high impedance non-latched input. At reset all pins of the C and D ports are set to input mode but the Buffer Registers are not initialized so they should be loaded before defining any pins as outputs. Reading Ports C or D provides the input pin values for inputs and the output latch values for outputs. The output values in the Buffer Registers are not affected by switching I/O pins from output to input or vice versa.

### Silicon Security™ Lock

Location 017FH in the Peripheral File is a special control register implemented as EEPROM memory which serves to disable external access to on board program memory. The highest level of security in the 72720 is achieved by locking the processor in the Single Chip mode via two EEPROM bits. This is achieved by writing a "1" to bit 0 and bit 7 of the control register via the PRG EEPROM programming instruction (writing '81H' to 017FH location) while the 72720 is in the Single Chip mode. When this bit is written the current mode is permanently locked preventing anyone from reading program memory by placing the chip in the EEPROM Program/Verify mode. The security lock register should be written only once on power-up/reset to achieve security lock. Subsequent power-up/reset operations should not execute any writes to the register after first write to lock. The security lock can be reset only by entering the Block Clear mode at Reset TWICE, which also erases all of program memory. The 72720 is designed to guarantee that in Block

Clear all of EEPROM memory will be completely erased before the lock bit is erased.

### Expansion Modes

In addition to the stand alone Single Chip mode the 72720 has three expansion modes which provide for the addition of external I/O peripheral devices and memory to supplement on chip functions.

**PERIPHERAL EXPANSION MODE** – This mode is intended to provide for the addition of external I/O ports and specialized I/O peripheral devices which are accessed as part of the 256 byte Peripheral File. The mode uses Port C as a bidirectional multiplexed 8 bit data/address bus and one half of Port B for address latch, and read/write control lines. This is the most efficient expansion mode in that it leaves 20 lines available on chip for general purpose I/O. Devices placed on this expansion bus are accessed the same as if they existed in the on chip Peripheral File sharing the same instructions and timing. This includes the logical instructions ANDP, ORP, and XORP which perform read/modify/write cycles on external Peripheral File locations to provide bit set, reset, and test capability.

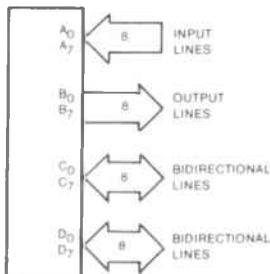
References to Port B while in this mode are handled in a special manner. When a write is performed to Port B, pins B<sub>0</sub>-B<sub>3</sub> output their new value and an external memory cycle writing the full 8 bit port value to address 0106H is performed as well. When Port B is read the least significant nibble is provided by I/O pins B<sub>0</sub>-B<sub>3</sub> and the most significant nibble by external Peripheral address 0106H.

**FULL EXPANSION MODE** – This mode allows for the addition of up to 61.5K bytes of external program and/or data memory to the 72720 using standard memory devices. This mode also includes the functions of Peripheral Expansion mode and uses the same I/O lines with the addition of Port D to provide the additional address lines required to access the full 64K address space. In this mode read and/or write sequence(s) to ports C and D reference external Peripheral File addresses 0108H and 010AH.

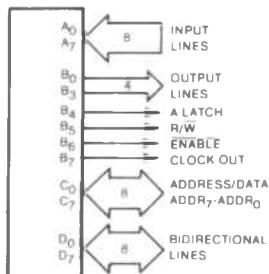
**MICROPROCESSOR MODE** – This mode operates the same as the Full Expansion mode except that any on chip program memory is disabled. All accesses to addresses not a part of the Register or Peripheral Files result in external memory access cycles. Unlike the Full Expansion mode the Microprocessor mode cannot be entered

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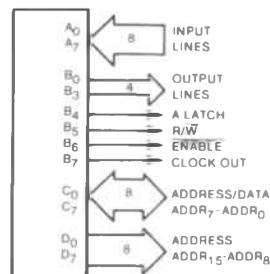
## Single Chip Mode



## Peripheral Expansion Mode



## Full Expansion Mode



under processor control from the Single Chip mode but must be initiated at Reset with  $V_H$  on the MC pin (see MODE CONTROL for a complete description). Once activated however, the Micro-processor mode can be permanently locked via the Security Lock Register in the same manner as can the Single Chip, Peripheral, and Full Expansion modes.

### Programming the EEPROM Memory

The 72720 provides two modes in which the on board program memory can be programmed:

**PROGRAM INSTRUCTION (PRG)** – In all normal operating modes the 72720's EEPROM memory can be programmed a byte at a time by executing a special instruction called Program (PRG). The PRG instruction can use any 16 bit register pair in the Register File as a pointer to the location to be programmed. The 8 bits of data to be programmed is placed in the A register prior to executing PRG. This addressing mode allows EEPROM memory to exist anywhere in the memory address space of the processor either on or off chip. The PRG instruction is a byte write operation approximately 13 milliseconds long (with a 10MHz XTAL) which can write any "1" bit to a "0". Any byte not erased i.e. not all "1"s must be initialized via an extra PRG instruction with data of all "1"s. The external read/write control logic of the 72720 operates in a special manner for PRG instructions to external memory to allow direct interface to both latched and non latched EEPROM memory components. Therefore EEPROM memory can be added off chip with no impact on system software or timing.

**SLAVE MODE PROGRAMMING** – This mode provides for programming the EEPROM memory under external control. Programming of the

72720 requires that the CPU be running since programming is performed under microcode control.

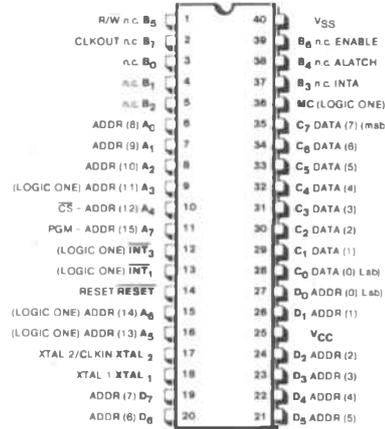
CPU operation requires the application of  $V_{CC}$ ,  $V_{SS}$ , and an external 2 to 10MHz clock input to the XTAL 2 pin, or a 2 to 10 MHz crystal between the XTAL 1 and XTAL 2 pins. Both crystal input pins must have a small high frequency capacitor (15 pf) to ground to guarantee reliable oscillator startup.

Before programming cycles can begin, the 72720 must first be placed in the Slave Program mode by releasing Reset while the MC, A<sub>4</sub> and A<sub>7</sub> pins are held at a logic one level ( $V_{IH}$ ). In the Slave Program mode full 16 bit address is used. Memory starts at F800 Hex and ends at FFFF Hex (72720 has 2K of EEPROM). Once the Slave Program mode has been entered, eleven bit addresses which select the byte to be programmed are applied to the Port D and Port A pins. The low order address A<sub>7</sub>-A<sub>0</sub> is applied to Port D (7-0) input/output pins and the high order address A<sub>10</sub>-A<sub>8</sub> to the lower half of Port A (2-0) pins. Data is written and read via the 8 bits of Port C (see figure 9 for Slave Program/Verify mode pin out). The Slave Program mode has both program and verify features. Once this mode has been entered, the A<sub>7</sub> pin acts as a programming pulse and pin A<sub>4</sub> becomes a Write/Read (Program/Verify) control line. Prior to programming data, the 72720's memory must be erased (all "1"s) either by a Block Clear of the entire memory or by writing all "1"s to the locations to be programmed using either the PRG Program Instruction or the Slave Program mode. A data byte is programmed into the addressed memory location when PGM (A<sub>7</sub>) is pulsed high while keeping CS (A<sub>4</sub>) high. This is

followed by keeping PGM (A<sub>7</sub>) low and pulsing  $\overline{CS}$  (A<sub>4</sub>) low at which time the 72720 outputs the programmed data byte on its Port C (7-0) bits, making verification of the programmed data byte possible. See SLAVE MODE PROGRAMMING TIMING for details.

**SLAVE VERIFY EEPROM MODE** – The programmed data bytes can be verified or read in this mode. This mode is entered by releasing Reset while holding A<sub>4</sub> pin at V<sub>IL</sub>, MC and A<sub>7</sub> pins at V<sub>IH</sub> respectively. To read or verify data at an addressed location, PGM (A<sub>7</sub>) has to be pulsed high while holding  $\overline{CS}$  (A<sub>4</sub>) high. This is followed by keeping PGM (A<sub>7</sub>) low and pulsing  $\overline{CS}$  (A<sub>4</sub>) low, at which time the 72720 outputs the data byte at the addressed location on its Port C (7-0) for verification. See SLAVE VERIFY EEPROM MODE TIMING for details.

### SLAVE PROGRAMMING PIN CONFIGURATION



ADDRESS ON PORT A (2-0): PINS (9-6)  
ON PORT D (7-0): PINS (19-24, 26, 27)  
DATA ON PORT C (7-0): PINS (35-28)

FIGURE 9

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## Electrical Specifications

### Absolute Maximum Ratings:

Ambient Temperature Under Bias... -10°C to +80°C  
Storage Temperature ..... -65°C to +150°C  
All Input or Output Voltages  
with Respect to Ground ..... +6V to -0.3V  
(+14V to -0.3V on mode control input pins)  
Package Maximum Power Dissipation ... 1.5 Watts

### DC Operating Characteristics

T<sub>A</sub>=0°C to 70°C, V<sub>CC</sub>=4.5 V to 5.5 V

### Operating Conditions:

Ambient Temperature Range ..... 0°C to 70°C  
V<sub>CC</sub> Power Supply ..... 4.5V to 5.5V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Limits			Units	Condition
		Min.	Typ.	Max		
I <sub>I1</sub>	Input Current A Port and Interrupts		100	200	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>I2</sub>	Input Current C and D Port		10	100	μA	V <sub>IN</sub> = 0.4V to V <sub>CC</sub>
I <sub>I3</sub>	Input Current Reset			10	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
I <sub>I4</sub>	Input Current MC			10	μA	V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>
C <sub>I</sub> <sup>(1)</sup>	Input Capacitance			10	pF	
V <sub>OH</sub>	High Level Output Voltage	2.4	2.8		V	I <sub>OH</sub> = -400 μA
V <sub>OL</sub>	Low Level Output Voltage		0.2	0.4	V	I <sub>OL</sub> = 3.2 mA
V <sub>IH</sub>	HI Level Input Voltage	Clk in	2.6		V	
		All Others	2.0			
V <sub>IL</sub>	LO Level Input Voltage	Clk in		0.6	V	
		All Others		0.8		
I <sub>CC</sub>	Power Supply Current		80	150	mA	All Outputs Open
P <sub>D (AV)</sub>	Average Power Dissipation		400	825	mW	All Outputs Open

#### Notes:

1. Characterized. Not tested.

**seeq** Technology, Incorporated

MD400005/-

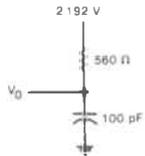
**AC Characteristics**

CLOCK IN/CRYSTAL Input specifications

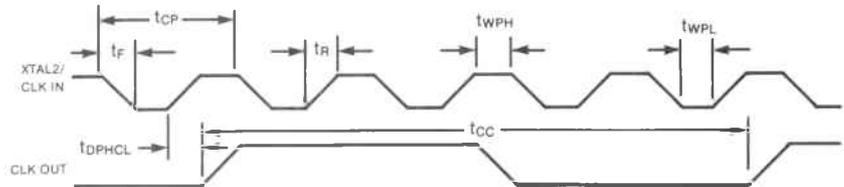
$T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ,  $V_{CC}=4.5\text{ V}$  to  $5.5\text{ V}$

Symbol	Parameter	72720-10			72720-16			Units	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.		
$t_{CP}$	Clockin Cycle Time	100		500	62.5		500	nS	
$t_{WPH}$	Clockin High Time	45			25			nS	
$t_{WPL}$	Clockin Low Time	45			25			nS	
$t_R$	Clockin Rise Time			30			30	nS	(1)
$t_F$	Clockin Fall Time			30			30	nS	(1)
$t_{DPHCL}$	Clockin to Clockout Rise		125	200		70	150	nS	

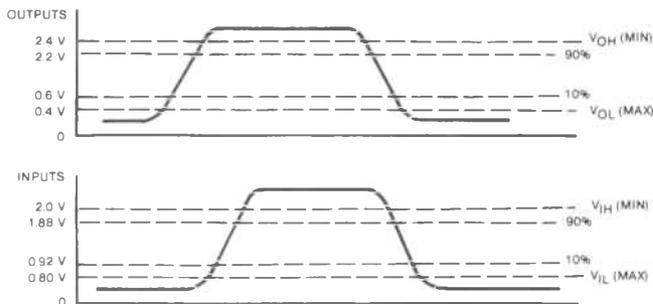
**Note 1** - Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points. (See figure 12).  
Measured outputs have 100-pF loads to  $V_{SS}$  (See figure 10).



**Figure 10**  
Output Loading Circuit for Test



**Figure 11**  
Clock Timing



**Figure 12**  
Measurement Points For  
Switching Characteristics

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## Bus Cycle Parameters

T<sub>A</sub>=0°C to 70°C, V<sub>CC</sub>=4.5 V to 5.5 V

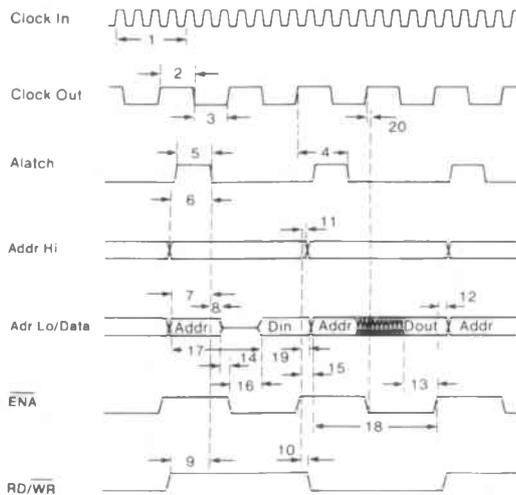
	Symbol	Parameter	72720-10 <sup>[2]</sup>			72720-16 <sup>[3]</sup>			Units	Condition
			Min.	Typ.	Max.	Min.	Typ.	Max.		
1	t <sub>CC</sub>	Clockout Cycle Time	400		2000	250		2000	nS	
2	t <sub>WCH</sub>	Clockout High Pulse Width	130	170	200	100			nS	
3	t <sub>WCL</sub>	Clockout Low Pulse Width	150	190	240	100			nS	
4	t <sub>DCHJL</sub>	Clockout to Alatch	260	300	340	180			nS	
5	t <sub>WJH</sub>	Alatch High Width	150	190	230	100			nS	
6	t <sub>DAHJL</sub>	HI Address Valid to Alatch	50	170	220	75			nS	
7	t <sub>DALJL</sub>	LO Address Valid to Alatch	50	150	220	75			nS	
8	t <sub>HJLAL</sub>	LO Addr Hold after Alatch	20	45	80	20			nS	
9	t <sub>DRWJL</sub>	RD/WR Valid to Alatch	50	140	200	50			nS	
10	t <sub>HEHRW</sub>	RD/WR Hold After Enable	40	100		40			nS	
11	t <sub>HEHAH</sub>	HI Addr Hold After Enable	30	40		30			nS	
12	t <sub>HEHO</sub>	Data Out Hold After Enable	65	80		50			nS	
13	t <sub>DOEH</sub>	Data Out Valid to Enable	230	290		150			nS	
14	t <sub>DAFEL</sub>	Enable to LO Addr High-Z	0	30	120	0			nS	
15	t <sub>DEHAF</sub>	Enable to Next Address	60	85		50			nS	
16	t <sub>DELD</sub>	Data in After Enable	155	190		140			nS	
17	t <sub>DAD</sub>	Valid Address to Data in	400	470		265			nS	
18	t <sub>DAEH</sub>	Enable HI After Valid Addr	580		730	390			nS	
19	t <sub>MEHD</sub>	Data in Hold After Enable	0			0			nS	
20	t <sub>OCHEL</sub>	Clockout to Enable	-10	15	50	-10			nS	
	t <sub>RO</sub>	Output Rise Time		9	50		9	50	nS	100 pF Load to V <sub>SS</sub> <sup>[1]</sup>
	t <sub>FO</sub>	Output Fall Time		10	60		10	60	nS	100 pF Load to V <sub>SS</sub> <sup>[1]</sup>

**Note 1** - Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points. See figure 10 and 12.

**Note 2** - All parameters specified at clockin/crystal frequency of 10 MHz.

**Note 3** - All parameters specified at clockin/crystal frequency of 16 MHz.

## 72720 Timing Diagram



### Memory and Peripheral Interface timing

These equations are given to allow memory and peripheral interface timings for the 72720 to be calculated at different frequencies using the propagation delay values which are constant with varying frequency. See 72720 Read/Write timing diagram for details (figure 14).

Propagation delay values:

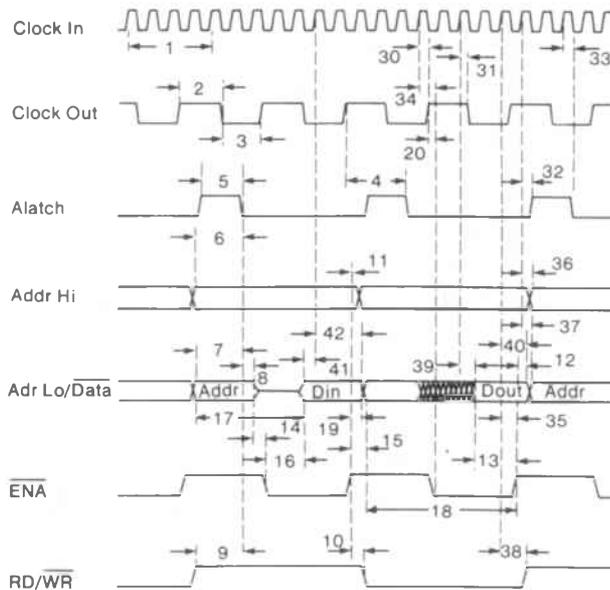
Values listed are typical values at 70°C @ 10 MHz XTAL frequency.

Ref. No.	Parameter	Typ.	Units	Comments
30	Clock in to Clock out HI	85	nS	
31	Clock in to Clock out LO	85	nS	
32	Clock in to AL Rise	95	nS	
33	Clock in to AL Fall	90	nS	
34	Clock in to Enable Fall	90	nS	
35	Clock in to Enable Rise	100	nS	
36	Clock in to HI Address Valid	120	nS	
37	Clock in to LO Address Valid	130	nS	
38	Clock in to Read/Write	140	nS	
39	Clock in to Data Out	120	nS	
40	Clock in to Data Out Hold	120	nS	
41	Data in Set Up to Clock in	40	nS	
42	Data in Hold After Clock in	35	nS	

### Memory Interface Timing Equations

	Symbol	Parameter	Equation	Computed Value	Units
2	t <sub>WCH</sub>	Clockout High Pulse Width	t <sub>CC/2</sub> + Clk in to Clk Out Fall - Clk in to Clk out Rise		nS
3	t <sub>WCL</sub>	Clockout Low Pulse Width	t <sub>CC/2</sub> + Clk in to Clk Out Rise - Clk in to Clk out Fall		nS
4	t <sub>DCHJL</sub>	Clockout to Alatch	3/4 * t <sub>CC</sub> + Clk in to AL Fall - Clk in to Clk out Rise		nS
5	t <sub>WJH</sub>	Alatch High Width	t <sub>CC/2</sub> + Clk in to AL Fall - Clk in to AL Rise		nS
6	t <sub>DAHJL</sub>	HI Address Valid to Alatch	t <sub>CC/2</sub> + Clk in to AL Fall - Clk in to High Addrs Valid		nS
7	t <sub>DALJL</sub>	LO Address Valid to Alatch	t <sub>CC/2</sub> + Clk in to AL Fall - Clk in Low Addrs Valid		
8	t <sub>HJLAL</sub>	LO Address Hold After Alatch		20	nS
9	t <sub>DRWJL</sub>	Read/Write Valid to Alatch	t <sub>CC/2</sub> + Clk in to AL Fall - Clk in to Read/Write		nS
10	t <sub>HEHRW</sub>	Read/Write Hold After Enable	t <sub>CC/4</sub> + Clk in to R/W - Clk in to Enable Rise		nS
11	t <sub>HEHAH</sub>	HI Address Hold After Enable	t <sub>CC/4</sub> + Clk in to HI Addr Valid - Clk in to Enable Rise		nS
12	t <sub>HEHO</sub>	Data Out Hold After Enable	t <sub>CC/4</sub> + Clk in to Data out Hold - Clk in to Enable Rise		nS
13	t <sub>DQEH</sub>	Data Out Valid to Enable	3/4 * t <sub>CC</sub> + Clk in to Enable Rise - Clk in to Data Out		nS
14	t <sub>DAFEL</sub>	Enable to LO Address High-Z	t <sub>CC/4</sub> + Clk in to Enable Fall - Clk in to Low Address Tristate		nS
15	t <sub>DEHAF</sub>	Enable to Next Address	t <sub>CC/4</sub> + Clk in to Low Address - Clk in to Enable Rise		nS
16	t <sub>DELd</sub>	Data in After Enable	3/4 * t <sub>CC</sub> + Data in Set Up to Clk in - Clk in to Enable Fall		nS
17	t <sub>DAD</sub>	Valid Address to Data in	3/2 * t <sub>CC</sub> + Data in Set Up to Clk in - Clk in to Low Address		nS
18	t <sub>DAEH</sub>	Enable HI after Valid Address	7/4 * t <sub>CC</sub> + Clk in Enable Rise - Clk in Low Addr		nS
19	t <sub>HEHD</sub>	Data in Hold After Enable	t <sub>CC/4</sub> + Clk in Enable Rise - Data in Hold After Clk in		nS
20	t <sub>DCHEL</sub>	Clockout to Enable	Clk in to Enable Fall - Clk in to Clk out high		nS

**Figure 14**  
**72720 Timing Diagram**



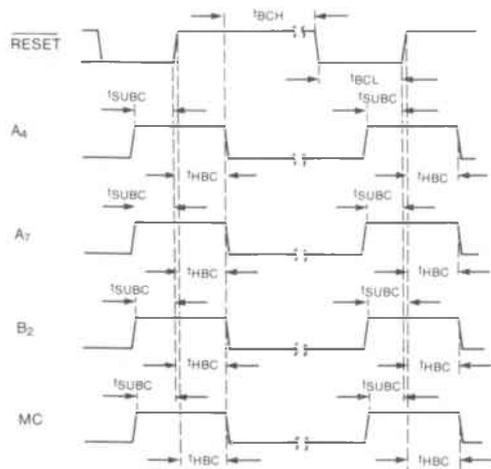
**Block Clear Specifications**

BLOCK CLEAR:  $V_{CC} = +6V \pm 10\%$   
SECURITY ENDURANCE: 50 CYCLES MAXIMUM

**BLOCK CLEAR TIMING**

Symbol	Parameter	Min.	Typ.	Max	Units	Comments
$t_{SUBC}$	Set Up Time to Reset	1			$\mu S$	
$t_{HBC}$	Hold Time After Reset	1			$\mu S$	
$t_{BCH}$	Block Clear Time HI	100			mS	
$t_{BCL}$	Block Clear Time LO	10			$\mu S$	

**Block Clear Timing**



**Figure 15**

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**External PRG Instruction Timing**

Symbol	Parameter	72720-10			72720-16			Units	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.		
t <sub>DQEL</sub>	Data Valid to Enable LO	200			100			nS	
t <sub>DALEL</sub>	Address Valid to Enable LO	13261			8287			uS	
t <sub>WEL</sub>	Width of Enable Low	13.26			8.287			mS	
t <sub>HEHAQ</sub>	Addr/Data Hold After Enable	65			50			nS	
t <sub>DQEH</sub>	Data Valid to Enable Rise	13261			8287			uS	

Note: All other PRG instruction timings are the same as for a normal external write operation.

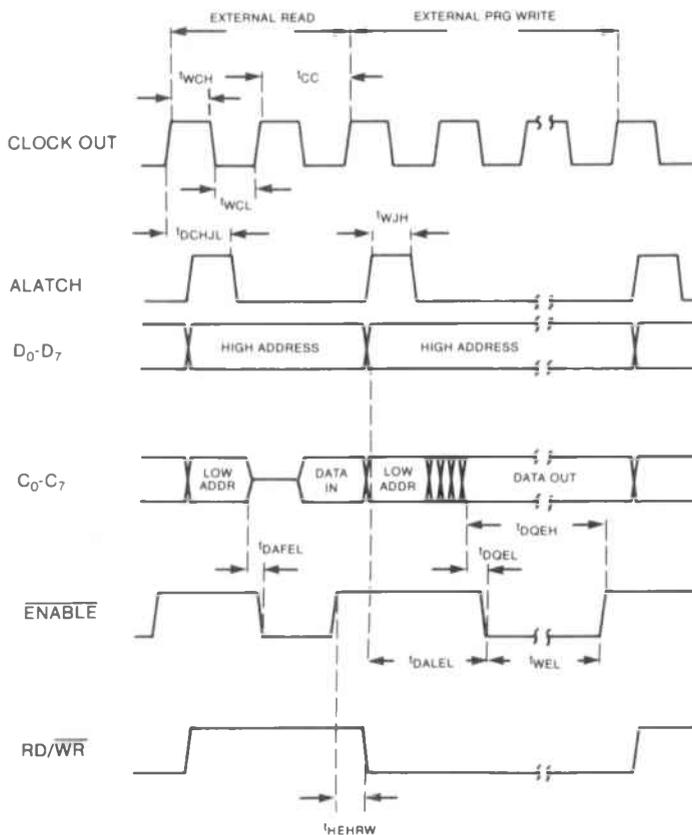


Figure 16

**Endurance and Data Retention**

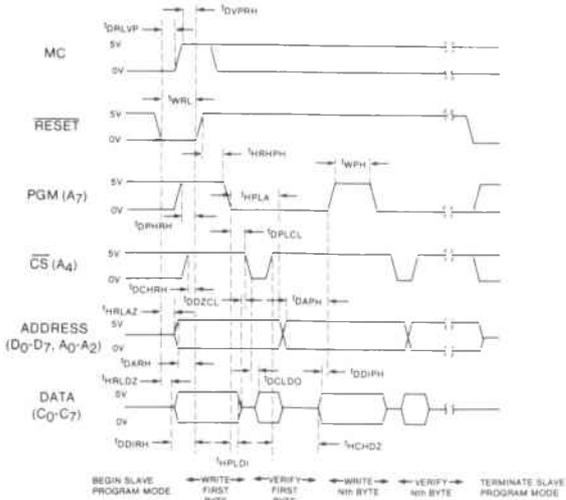
Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**Slave Programming Mode Timing at 10 MHz**

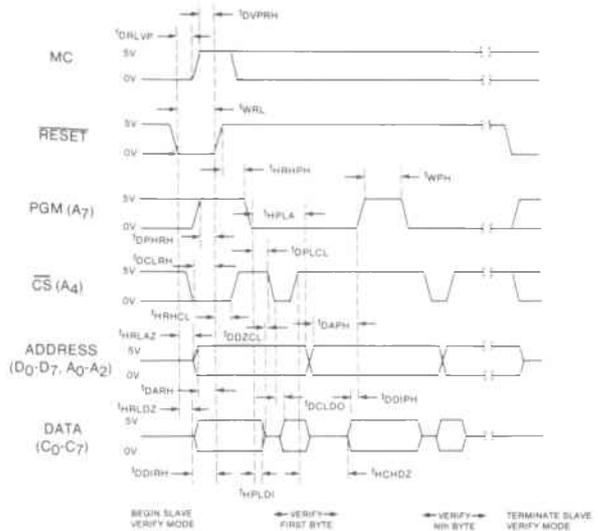
Symbol	Parameter	Limits			Units	Conditions
		Min.	Typ.	Max		
t <sub>DRLVP</sub>	Reset to V <sub>PP</sub>	2			uS	
t <sub>HRLAZ</sub>	Address Hold HI Z	400			nS	
t <sub>HRLDZ</sub>	Data Hold HI Z	400			nS	
t <sub>WRL</sub>	Reset Width	2			uS	
t <sub>DVPRH</sub>	V <sub>PP</sub> to Reset	1			uS	
t <sub>DPHRH</sub>	PGM to Reset	1			uS	
t <sub>DCHRH</sub>	CS HI to Reset	0				
t <sub>DCLR</sub>	CS LO to Reset	1			uS	
t <sub>DARH</sub>	Address to Reset	0				
t <sub>DDIRH</sub>	Data to Reset	0				
t <sub>HPLA</sub>	Address Hold PGM	0				
t <sub>HPLDI</sub>	Data Hold PGM	0				
t <sub>HRHPH</sub>	PGM Hold		10		mS	
t <sub>HRHCL</sub>	CS Hold	1			uS	
t <sub>DPLCL</sub>	PGM to CS	4			uS	
t <sub>DDZCL</sub>	Data HI Z to CS	0				
t <sub>DCLDO</sub>	CS to Data Out			400	nS	
t <sub>WPH</sub>	PGM High Width		10		mS	
t <sub>DAPH</sub>	Address to PGM	0				
t <sub>DDIPH</sub>	Data to PGM	0				
t <sub>HCHDZ</sub>	Data HI Z Hold	400			nS	

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**Figure 17**  
**72720 SLAVE PROGRAM MODE TIMING**



**Figure 18**  
**72720 SLAVE VERIFICATION TIMING**



## Instruction Set Summary

DATA MOVE INSTRUCTIONS					
MEMORNIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
MOV Rn,A	Move Register File to A	12	2	8	ZNC
MOV %n,A	Move Immediate to A	22	2	7	ZNC
MOV Rn,B	Move Register File to B	32	2	8	ZNC
MOV Rn,Rn	Move Register File to Register File	42	3	10	ZNC
MOV %n,B	Move Immediate to B	52	2	7	ZNC
MOV B,A	Move B to A Register	62	1	5	ZNC
MOV %n,Rn	Move Immediate to Register File	72	3	9	ZNC
MOV A,B	Move A to B Register	C0	1	6	ZNC
MOV A,Rn	Move A to Register File	D0	2	8	ZNC
MOV B,Rn	Move B to Register File	D1	2	7	ZNC
MOV A,Pn	Move A to Peripheral	82	2	10	ZNC
MOV B,Pn	Move B to Peripheral	92	2	9	ZNC
MOV %n,Pn	Move Immediate to Peripheral	A2	3	11	ZNC
MOV Pn,A	Move Peripheral to A	80	2	9	ZNC
MOV Pn,B	Move Peripheral to B	91	2	8	ZNC
MOV %n,Rn	Move Double Byte Immediate to Register File	88	4	15	ZNC
MOVD Rn,Rn	Move Double Byte Register File to Register File	98	3	14	ZNC
MOVD %n(B),Rn	Move Immediate Double Byte + B Register to Register File	AB	4	17	ZNC
LDA @n	Load A Direct (16 Bit Address)	8A	3	11	ZNC
LDA *Rn	Load A Indirect (via Register Pair)	9A	2	10	ZNC
LDA @n(B)	Load A Direct indexed	AA	3	13	ZNC
STA *Rn	Store A Direct	8B	3	11	ZNC
STA @n	Store A Indirect	9B	2	10	ZNC
STA @n(B)	Store A Direct Indexed	AB	3	13	ZNC
PRG *Rn	Program EEPROM Indirect	04	2	33165	ZNC
XCHB A	Exchange A with B Register	B6	1	6	ZNC
XCHB B	Exchange B with B Register	C6	1	6	ZNC
XCHB Rn	Exchange Register File with B Register	D6	2	8	ZNC
SWAP A	Swap Nibbles of A Register	B7	1	8	ZNC
SWAP B	Swap Nibbles of B Register	C7	1	8	ZNC
SWAP Rn	Swap Nibbles of Register File	D7	2	10	ZNC
PUSH A	Push A Register on Stack	B8	1	6	ZNC
PUSH B	Push B Register on Stack	CB	1	6	ZNC
PUSH Rn	Push Register File on Stack	D8	2	8	ZNC
POP A	Pop A Register from Stack	B9	1	6	ZNC
POP B	Pop B Register from Stack	C9	1	6	ZNC
POP Rn	Pop Register File from Stack	D9	2	8	ZNC

ARITHMETIC INSTRUCTIONS					
MMEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
ADD Rn,A	Add Register File to A Register	18	2	8	Z NC
ADD %n,A	Add Immediate to A Register	28	2	7	Z NC
ADD Rn,B	Add Register File to B Register	38	2	8	Z NC
ADD Rn,Rn	Add Register to Register	48	3	10	Z NC
ADD %n,B	Add Immediate to B Register	58	2	7	Z NC
ADD B,A	Add B to A Register	68	1	5	Z NC
ADD %n,Rn	Add Immediate to Register File	78	3	9	Z NC
ADC Rn,A	Add w Carry Register File to A Reg.	19	2	8	Z NC
ADC %n,A	Add w Carry Immediate to A Reg.	29	2	7	Z NC
ADC Rn,B	Add w Carry Register File to B Reg.	39	2	8	Z NC
ADC Rn,Rn	Add w Carry Reg. File to Reg. File	49	3	10	Z NC
ADC %n,B	Add w Carry Immediate to B Reg.	59	2	7	Z NC
ADC B,A	Add w Carry B to A Register	69	1	5	Z NC
ADC %n,Rn	Add w Carry Immediate to Reg. File	79	3	9	Z NC
SUB Rn,A	Subtract Register File from A	1A	2	8	Z NC
SUB %n,A	Subtract Immediate from A	2A	2	7	Z NC
SUB Rn,B	Subtract Register File from B	3A	2	8	Z NC
SUB Rn,Rn	Subtract Reg. File from Reg. File	4A	3	10	Z NC
SUB %n,B	Subtract Immediate from B	5A	2	7	Z NC
SUB B,A	Subtract B from A Register	6A	1	5	Z NC
SUB %n,Rn	Subtract Immediate from Reg. File	7A	3	9	Z NC
SBB Rn,A	Subtract w Borrow Reg. File from A	1B	2	8	Z NC
SBB %n,A	Subtract w Borrow Immediate from A	2B	2	7	Z NC
SBB Rn,B	Subtract w Borrow Reg. File from B	3B	2	8	Z NC
SBB Rn,Rn	Subtract w Borrow Reg. File from Register File	4B	3	10	Z NC
SBB %n,B	Subtract w Borrow Immediate from B	5B	2	7	Z NC
SBB B,A	Subtract w Borrow B from A Reg.	6B	1	5	Z NC
SBB %n,Rn	Subtract w Borrow Immediate from Register File	7B	3	9	Z NC
CMP Rn,A	Compare Register File to A	1D	2	8	Z NC
CMP %n,A	Compare Immediate to A	2D	2	7	Z NC
CMP Rn,B	Compare Register File to B	3D	2	8	Z NC
CMP Rn,Rn	Compare Register File to Reg. File	4D	3	10	Z NC
CMP %n,B	Compare Immediate to B	5D	2	7	Z NC
CMP B,A	Compare B to A Register	6D	1	5	Z NC
CMP %n,Rn	Compare Immediate to Register File	7D	3	9	Z NC
CPMA @ n	Compare Direct to A	8D	3	12	Z NC
CPMA *Rn	Compare Indirect to A	9D	2	11	Z NC
CPMA @ n(B)	Compare Direct Indexed to A	AD	3	14	Z NC

ARITHMETIC INSTRUCTIONS					
MMEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
DAC Rn,A	Decimal Add w Carry Reg. File to A	1E	2	10	Z NC
DAC %n,A	Decimal Add w Carry Immed. to A	2E	2	9	Z NC
DAC Rn,B	Decimal Add w Carry Reg. File to B	3E	2	10	Z NC
DAC Rn,Rn	Decimal Add w Carry Register File to Register File	4E	3	12	Z NC
DAC %n,B	Decimal Add w Carry Immed. to B	5E	2	9	Z NC
DAC B,A	Decimal Add w Carry B to A Reg.	6E	1	7	Z NC
DAC %n,Rn	Decimal Add w Carry Immediate to Register File	7E	3	11	Z NC
DSB Rn,A	Decimal Subtract w Borrow Register File from A Register	1F	2	10	Z NC
DSB %n,A	Decimal Subtract w Borrow Immediate from A Register	2F	2	9	Z NC
DSB Rn,B	Decimal Subtract w Borrow Register File from B Register	3F	2	10	Z NC
DSB Rn,Rn	Decimal Subtract w Borrow Register File from Register File	4F	3	12	Z NC
DSB %n,B	Decimal Subtract w Borrow Immediate from B Register	5F	2	9	Z NC
DSB B,A	Decimal Subtract w Borrow B from A Register	6F	1	7	Z NC
DSB %n,Rn	Decimal Subtract w Borrow Immediate from Register File	7F	3	11	Z NC
MPY Rn,A	Multiply A by Register File	1C	2	47	Z NC
MPY %n,A	Multiply A Immediate	2C	2	46	Z NC
MPY Rn,B	Multiply B by Register File	3C	2	47	Z NC
MPY Rn,Rn	Multiply Register File by Reg. File	4C	3	49	Z NC
MPY %n,B	Multiply B Immediate	5C	2	46	Z NC
MPY B,A	Multiply A by B Register	6C	1	44	Z NC
MPY %n,Rn	Multiply Register File Immediate	7C	3	48	Z NC
INC A	Increment A Register	B3	1	5	Z NC
INC B	Increment B Register	C3	1	5	Z NC
INC Rn	Increment Register File	D3	2	7	Z NC
DEC A	Decrement A Register	B2	1	5	Z NC
DEC B	Decrement B Register	C2	1	5	Z NC
DEC Rn	Decrement Register File	D2	2	7	Z NC
DECD A	Decrement Double A Register	BB	1	9	Z NC
DECD B	Decrement Double B Register	CB	1	9	Z NC
DECD Rn	Decrement Double Register File	DB	2	11	Z NC

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LOGICAL INSTRUCTIONS					
MEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
AND Rn,A	AND Register File to A	13	2	8	Z N C
AND %n,A	AND Immediate to A	23	2	7	Z N C
AND Rn, B	AND Register File to B	33	2	8	Z N C
AND Rn, Rn	AND Reg. File to Reg. File	43	3	10	Z N C
AND %n,B	AND Immediate to B	53	2	7	Z N C
AND B,A	AND B to A Register	63	1	5	Z N C
AND %n,Rn	AND Immediate to Reg. File	73	3	9	Z N C
OR Rn,A	OR Register File to A	14	2	8	Z N C
OR %n,A	OR Immediate to A	24	2	7	Z N C
OR Rn,B	OR Register File to B	34	2	8	Z N C
OR Rn, Rn	OR Register File to Reg. File	44	3	10	Z N C
OR %n,B	OR Immediate to B	54	2	7	Z N C
OR B,A	OR B to A Register	64	1	5	Z N C
OR %n,Rn	OR Immediate to Reg. File	74	3	9	Z N C
XOR Rn,A	Exclusive OR Reg. File to A	15	2	8	Z N C
XOR %n,A	Exclusive OR Immediate to A	25	2	7	Z N C
XOR Rn,B	Exclusive OR Reg. File to B	35	2	8	Z N C
XOR Rn, Rn	Exclusive OR Register File to Register File	45	3	10	Z N C
XOR %n,B	Exclusive OR Immediate to B	55	2	7	Z N C
XOR B,A	Exclusive OR B to A Register	65	1	5	Z N C
XOR %n,Rn	Exclusive OR Immediate to Register File	75	3	9	Z N C
ANDP A,Pn	AND A Register to Peripheral File	83	2	10	Z N C
ANDP B,Pn	AND B Register to Peripheral File	93	2	9	Z N C
ANDP %n,Pn	AND Immediate to Peripheral File	A3	3	11	Z N C
ORP A,Pn	OR A Register to Peripheral File	84	2	10	Z N C
ORP B,Pn	OR B Register to Peripheral File	94	2	9	Z N C
ORP %n,Pn	OR Immediate to Peripheral File	A4	3	11	Z N C
XORP A,Pn	Exclusive OR A Register to Peripheral File	85	2	10	Z N C
XORP B,Pn	Exclusive OR B Register to Peripheral File	95	2	9	Z N C
XORP %n,Pn	Exclusive OR Immediate to Peripheral File	A5	3	11	Z N C
RR A	Rotate Right A Register	BC	1	5	Z N C
RR B	Rotate Right B Register	CC	1	5	Z N C
RR Rn	Rotate Right Register File	DC	2	7	Z N C
RRC A	Rotate Right w Carry A Register	BD	1	5	Z N C
RRC B	Rotate Right w Carry B Reg	CD	1	5	Z N C
RRC Rn	Rotate Right w Carry Register File	DD	2	7	Z N C
RL A	Rotate Left A Register	BE	1	5	Z N C
RL B	Rotate Left B Register	CE	1	5	Z N C
RL Rn	Rotate Left Register File	DE	2	7	Z N C
RLC A	Rotate Left w Carry A Reg.	BF	1	5	Z N C
RLC B	Rotate Left w Carry B Reg.	CF	1	5	Z N C
RLC Rn	Rotate Left w Carry Register File	DF	2	7	Z N C
INV A	Invert A Register	B4	1	5	Z N C
INV B	Invert B Register	C4	1	5	Z N C
INV Rn	Invert Register File	D4	2	7	Z N C
CLR A	Clear A Register	B5	1	5	Z N C
CLR B	Clear B Register	C5	1	5	Z N C
CLR Rn	Clear Register File	D5	2	7	Z N C

JUMP INSTRUCTIONS					
MEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
BR @n	Branch Direct	8C	3	10	
BR *Rn	Branch Indirect	9C	2	9	
BR @n (B)	Branch Direct Indexed	AC	3	12	
JMP	Jump Relative	E0	2	7	
JN	Jump if Negative	E1	2	5/7	
JZ	Jump if Zero	E2	2	5/7	
JC	Jump if Carry	E3	2	5/7	
JP	Jump if Positive	E4	2	5/7	
JPZ	Jump if Positive or Zero	E5	2	5/7	
JNZ	Jump if Non Zero	E6	2	5/7	
JNC	Jump if No Carry	E7	2	5/7	
BTJO Rn,A	Bit Test Jump if One A Reg. (Bit Mask in Register File)	16	3	10	Z N C
BTJO %n,A	Bit Test Jump if One A Reg. (Bit Mask is Immediate)	26	3	9	Z N C
BTJO Rn,B	Bit Test Jump if One B Reg. (Bit Mask in Register File)	36	3	10	Z N C
BTJO Rn, Rn	Bit Test Jump if One Reg. File (Bit Mask in Register File)	46	4	12	Z N C
BTJO %n,B	Bit Test Jump if One B Reg. (Bit Mask is Immediate)	56	3	9	Z N C
BTJO B,A	Bit Test Jump if One A Reg. (Bit Mask in B Register)	66	2	7	Z N C
BTJO %n,Rn	Bit Test Jump if One Reg. File (Bit Mask is Immediate)	76	4	11	Z N C
BTJZ Rn,A	Bit Test Jump if Zero A Reg. (Bit Mask in Register File)	17	3	10	Z N C
BTJZ %n,A	Bit Test Jump if Zero A Reg. (Bit Mask is Immediate)	27	3	9	Z N C
BTJZ Rn,B	Bit Test Jump if Zero B Reg. (Bit Mask in Register File)	37	3	10	Z N C
BTJZ Rn, Rn	Bit Test Jump if Zero Reg. File (Bit Mask in Register File)	47	4	12	Z N C
BTJZ %n,B	Bit Test Jump if Zero B Reg. (Bit Mask is Immediate)	57	3	9	Z N C
BTJZ B,A	Bit Test Jump if Zero A Reg. (Bit Mask in B Register)	67	2	7	Z N C
BTJZ %n,Rn	Bit Test Jump if Zero Reg. File (Bit Mask is Immediate)	77	4	11	Z N C
BTJOP A,Pn	Bit Test Jump if One Periph. File (Bit Mask in A Register)	86	3	11	Z N C
BTJOP B,Pn	Bit Test Jump if One Periph. File (Bit Mask in B Register)	96	3	10	Z N C
BTJOP %n,Pn	Bit Test Jump if One Periph. File (Bit Mask is Immediate)	A6	4	12	Z N C
BTJZP A,Pn	Bit Test Jump if Zero Periph. File (Bit Mask in A Register)	87	3	11	Z N C
BTJZP B,Pn	Bit Test Jump if Zero Periph. File (Bit Mask in B Register)	97	3	10	Z N C
BTJZP %n,Pn	Bit Test Jump if Zero Periph. File (Bit Mask is Immediate)	A7	4	12	Z N C
DJNZ A	Decrement Jump if Non Zero A Reg.	BA	2	7/9	Z N C
DJNZ B	Decrement Jump if Non Zero B Reg.	CA	2	7/9	
DJNZ Rn	Decrement Jump if Non Zero Register File	DA	3	9/11	

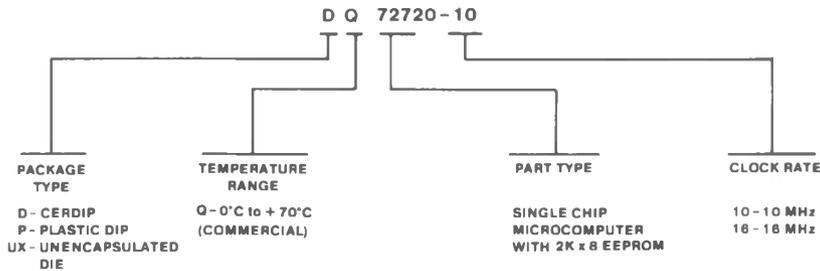
SUBROUTINE INSTRUCTIONS					
MNEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
CALL @n	Call Subroutine Direct	8E	3	14	
CALL *Rn	Call Subroutine Indirect	9E	2	13	
CALL @n(B)	Call Subroutine Direct Indexed	AE	3	16	
TRAP 23	Trap to Vector 23	E8	1	14	
TRAP 22	22	E9	1	14	
TRAP 21	21	EA	1	14	
TRAP 20	20	EB	1	14	
TRAP 19	19	EC	1	14	
TRAP 18	18	ED	1	14	
TRAP 17	17	EE	1	14	
TRAP 16	16	FF	1	14	
TRAP 15	15	F0	1	14	
TRAP 14	14	F1	1	14	
TRAP 13	13	F2	1	14	
TRAP 12	12	F3	1	14	
TRAP 11	11	F4	1	14	
TRAP 10	10	F5	1	14	
TRAP 9	9	F6	1	14	
TRAP 8	8	F7	1	14	
TRAP 7	7	F8	1	14	
TRAP 6	6	F9	1	14	
TRAP 5	5	FA	1	14	
TRAP 4	4	FB	1	14	
TRAP 3	3	FC	1	14	
TRAP 2	2	FD	1	14	
TRAP 1	1	FE	1	14	
TRAP 0	0	FF	1	14	
RETS	Return from Subroutine	0A	1	7	
RET1	Return from interrupt Routine	0B	1	9	I Z N C

CONTROL INSTRUCTIONS					
MNEMONIC	DESCRIPTION	CODE	BYTES	CYCLES	FLAGS
NOP	No. Operation	00	1	4	
IDLE	Wait for Interrupt	01	1	6+	
EINT	Enable Interrupts	05	1	5	I Z N C
DINT	Disable Interrupts	06	1	5	I Z N C
LDSP	Load Stack Pointer to B Register	0D	1	5	
STSP	Store Stack Pointer to B Register	09	1	6	
POP ST	Pop Status from Stack	0B	1	6	I Z N C
PUSH ST	Push Status on Stack	0E	1	6	I Z N C
TSTA	Test A/Set Flags on Contents	80	1	6	Z N C
TSTB	Test B/Set Flags on Contents	C1	1	5	Z N C
SETC	Set Carry Flag	07	1	5	Z N C
CLRC	Clear Carry Flag (and Test A Register)	80	1	6	Z N C

- NOTES**
1. Rn denotes a register or register pair in Register File where n= 0 to 255. When a Register pair is called for, pair consists of Rn and Rn-1 where Rn is least significant byte.
  2. Pn denotes a location in the Peripheral File where n= 0 to 255
  3. %n denotes one or two byte immediate data.
  4. @n denotes a Direct 16 bit Address
  5. (B) indicates contents of B Register is added as index to direct address
  6. \*Rn denotes a 16 bit Indirect address located in registers Rn and Rn-1 (Least significant byte in Rn)
  7. Each Cycle= 400ns with 10MHz Crystal, 250ns with 16MHz Crystal
  8. Conditional Jumps require two cycles more to execute if jump is taken than if jump is not taken
  9. Flag definitions:

I - Interrupt Enable  
 Z - Zero  
 N - Negative  
 C - Carry

## Ordering Information



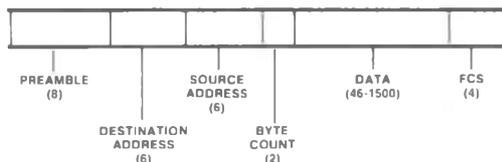




## Functional Description

### Frame Format

On an Ethernet communication network, information is transmitted and received in packets or frames. An Ethernet frame consists of a preamble, two address fields, a byte-count field, a data field, and a frame check sequence (FCS). Each field has a specific format which is described in detail below. An Ethernet frame has a minimum length of 64 bytes and a maximum length of 1518 bytes exclusive of the preamble. The Ethernet frame format is shown below.



#### NOTE:

Field length in bytes in parentheses.

**Preamble:** The preamble is a 64-bit field consisting of 62 alternating "1"s and "0"s followed by a "11" End-of-Preamble indicator.

**Destination Address:** The Destination Address is a 6-byte field containing either a specific Station Address, a Broadcast Address, or a Multicast Address to which this frame is directed.

**Source Address:** The Source Address is a 6-byte field containing the specific Station Address from which this frame originated.

**Byte-Count Field:** The Byte-Count Field consists of two bytes providing the number of valid data bytes in the Data Field, 46 to 1500. This field is uninterpreted at the Data Link Layer, and is passed through the EDLC chip to be handled at the Client Layer.

**Data Field:** The Data Field consists of 46 to 1500 bytes of information which are fully transparent in the sense that any arbitrary sequence of bytes may occur.

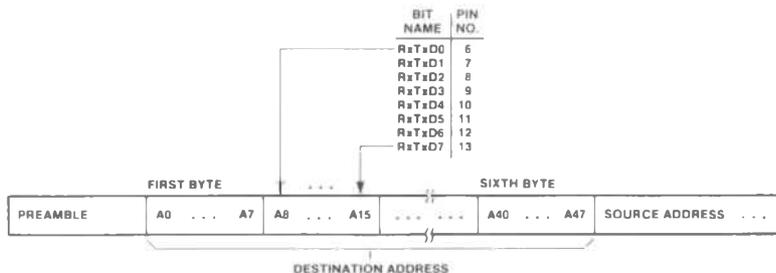
**Frame Check Sequence:** The Frame Check Sequence (FCS) field is a 32-bit cyclic redundancy check (CRC) value computed as a function of the Destination Address Field, Source Address Field, Type Field, and Data Field. The FCS is appended to each transmitted frame, and used at reception to determine if the received frame is valid.

### Transmitting

The transmit data stream consists of the Preamble, four information fields, and the FCS which is computed in real time by the EDLC chip and automatically appended to the frame at the end of the serial data. The Preamble is also generated by the EDLC chip and transmitted immediately prior to the Destination Address. Destination Address, Source Address, Type Field and Data Field are prepared in the buffer memory prior to initiating transmission. The EDLC chip encapsulates these fields into an Ethernet frame by inserting a preamble prior to these information fields and appending a CRC after the information fields.

### Transmission Initiation/Deferral

The Ethernet node initiates a transmission by storing the entire information content of the frame to be transmitted in an external buffer memory, and then transferring initial frame bytes to the EDLC Transmit FIFO. "Transmit-buffer to FIFO" transfers are coordinated via the  $\overline{\text{TxWR}}$  and TxRDY handshake interface, i.e., bytes are written to the FIFO via  $\overline{\text{TxWR}}$  only when TxRDY is HIGH. Actual transmission of the data onto the network will only occur if the network has not been busy for the minimum defer time (9.6  $\mu\text{s}$ ) and any Backoff time requirements have been satisfied. When transmission begins, the EDLC chip activates the transmit enable (TxEN) line concurrently with the transmission of the first bit of the Preamble and keeps it active for the duration of the transmission.



BITS WITHIN A BYTE ARE TRANSMITTED/RECEIVED BIT NO. "0" FIRST THROUGH BIT NO. "7" LAST.

Figure 1. Bit Serialization/Deserialization



bits (8 bytes) long. The Preamble consists of a sequence of 62 alternating "1"s and "0"s followed by "11", with the frame information fields immediately following. In order for the decoder phase-lock to occur, the EDLC chip waits 16 bit times before looking for the "11" end of preamble indicator. If the EDLC chip receives a "00" before receiving the "11" in the Preamble, an error condition has occurred. The frame is not received, and the EDLC chip begins monitoring the network for a carrier again.

#### Address Matching

Ethernet addresses consist of two 6-byte fields. The first bit of the address signifies whether it is a Station Address or a Multicast/Broadcast Address.

First Bit	Address
0	Station Address (Physical)
1	Multicast/Broadcast Address (logical)

Address matching occurs as follows:

**Station Address:** All destination address bytes must match the corresponding bytes found in the Station Address Register.

**Multicast Address:** If the first bit of the incoming address is a 1 and the EDLC chip is programmed to accept Multicast Addresses, the frame is received.

**Broadcast Address:** The six incoming destination address bytes must all be FF hex. If the EDLC chip is programmed to accept Broadcast or Multicast Addresses the frame will be received.

If the incoming frame is addressed to the EDLC chip specifically (Destination Address matches the contents of the Station Address Register), or is of general or group interest (Broadcast or Multicast Address), the EDLC chip will pass the frame exclusive of Preamble and FCS to the CPU buffer and indicate any error conditions at the end of the frame. If, however, the address does not match, as soon as the mismatch is recognized the EDLC chip will terminate reception and issue an RxDC.

The EDLC chip may be programmed via the Match Mode bits of the Receive Command Register to ignore all frames (Disable Receiver), accept all frames (Promiscuous mode), accept frames with the proper Station Address or the Broadcast Address (Station/Broadcast), or accept all frames with the proper Station Address, the Broadcast Address, or all Multicast Addresses (Station/Broadcast/Multicast).

#### Terminating Reception

Reception is terminated when either of the following conditions occur:

**Carrier Sense Inactive:** Indicates that traffic is no longer present on the Ethernet cable.

**Overflow:** The host node for some reason is not able to empty the Receive FIFO as rapidly as it is filled, and an error occurs as frame data is lost. On average the Receive FIFO must be serviced every 800 ns to avoid this conditions.

#### Frame Reception Conditions

Upon terminating reception, the EDLC chip will determine the status of the received frame and conditionally load it into the Receive Status Register. An interrupt will be issued if the appropriate conditions as specified in the Receive Command Register are present. The EDLC chip may report the following conditions at the end of frame reception:

**Overflow:** The EDLC internal Receive FIFO overflows.

**Dribble Error:** Carrier Sense did not go inactive on a receive data byte boundary.

**CRC Error:** The 32-bit CRC transmitted with the frame does not match that calculated upon reception.

**Short Frame:** A frame containing less than 64 bytes of information was received (including FCS).

**Good Frame:** A frame is received that does not have a CRC error, Shortframe, or Overflow condition.

#### System Interface

The EDLC chip system interface consists of two independent busses and respective control signals. Data is read and written over the Receive/Transmit Data Bus RxTx<sub>D</sub> (0-7). These transfers are controlled by the TxRDY and TxWR signals for transmitted data, and RxRDY and RxRD signals for received data. All Commands and Station Addresses are written, and all status read over a separate Command/Status Bus CdSt (0-7). These transfers are controlled by the CS, RD, WR, and A0-A2 signals. The EDLC chip's command and status registers may be accessed at any time. However, it is recommended that writing to the command register be done only during interframe gaps.

With the exception of the two Match Mode bits in the Receive Command Register, all bits in both command registers are interrupt enable bits. Changing the interrupt enable bits during frame transmission does not affect the frame integrity. Asynchronous error events, however, e.g., overflow, underflow, etc., may cause chip operation to vary, if their corresponding enable bits are being altered at the same time.

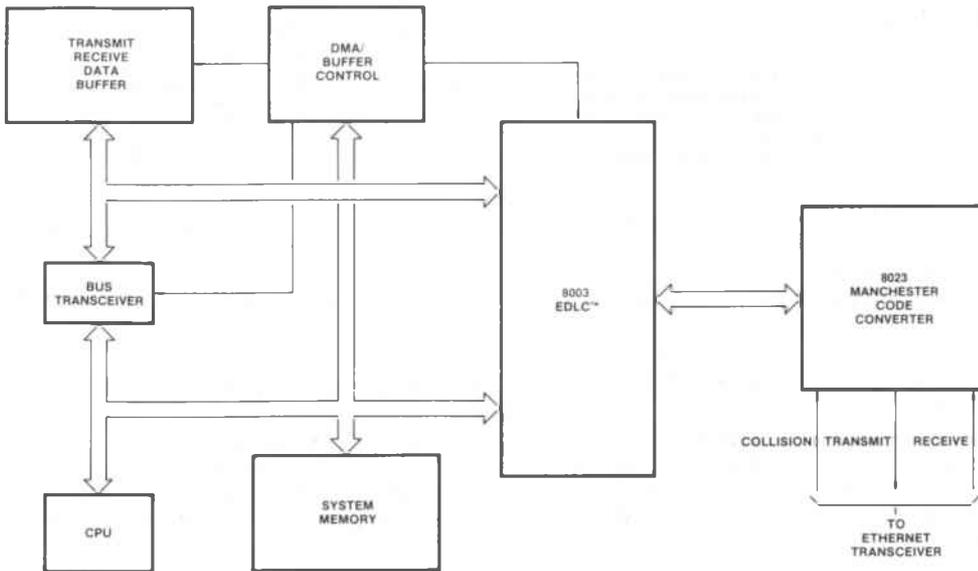


Figure 3. Typical Ethernet Node Configuration

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Reading the status registers may also occur at any time during transmission or reception.

**Internal Register Addressing**

	Register Address			Register Description	
	A2	A1	A0	Read	Write
0	0	0	0	—	Station Addr 0
1	0	0	1	—	Station Addr 1
2	0	1	0	—	Station Addr 2
3	0	1	1	—	Station Addr 3
4	1	0	0	—	Station Addr 4
5	1	0	1	—	Station Addr 5
6	1	1	0	Rx Status	Rx Command
7	1	1	1	Tx Status	Tx Command

Status registers are read only registers. Command and Station Address registers are write only registers. Access to these registers is via the CPU interface: Control signals CS, RD, WR, and the Command/Status Data Bus CdSt (0-7).

**Station Address Register**

The Station Address Register is 6 bytes in length. The contents may be written in any order, with bit "0" of byte "0" corresponding to the first bit received in the

data stream, and indicating whether the address is physical or logical. Bit 7 of station address byte 5 is compared to the last bit of the received destination address. The Station Address should be programmed prior to enabling the receiver.

**Transmit Command Register**

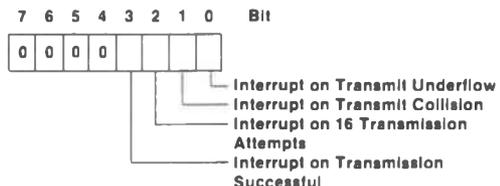
The Transmit Command Register is an interrupt mask register, which provides for control of the conditions allowed to generate transmit interrupts. Each of the four least significant bits of the register may be individually set or cleared. When set, the occurrence of the associated condition will cause an interrupt to be generated. The four specific conditions for which interrupts may be generated are:

- Underflow
- Collision
- 16 Collisions
- Transmission Successful

The interrupt signal INT will be set when one or more of the specified transmission termination conditions occurs and the associated command bit has been set. The interrupt signal INT will be cleared when the Transmit Status Register is read.

All bits of the Transmit Command Register are cleared upon chip reset.

**Transmit Command Register Format**



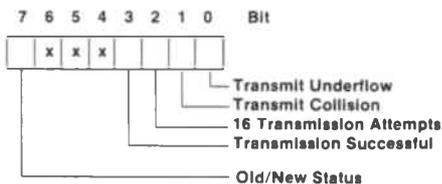
Transmission Successful is set only on the successful transmission or retransmission of a frame.

**Transmit Status Register**

The Transmit Status Register is loaded at the conclusion of each frame transmission or retransmission attempt. It provides for the reporting of both the normal and error termination conditions of each transmission.

The OLD/NEW status bit is set each time the Transmit Status Register is read, and reset each time new status is loaded into the Transmit Status Register. The OLD/NEW status bit is SET, and all other bits CLEARED upon chip reset.

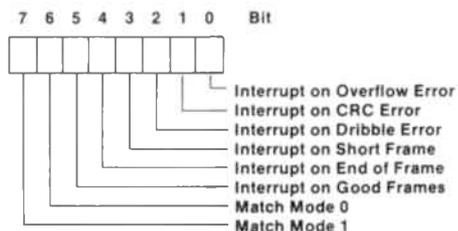
**Transmit Status Register Format**



**Receive Command Register**

The Receive Command Register has two primary functions, it specifies the Address Match Mode, and it specifies Frames-of-Interest. i.e. frames whose arrival must be communicated to the CPU via interrupts and status register updates. Frames-of-Interest are frames whose status must be saved for inspection, even at the expense of losing subsequent frames.

**Receive Command Register Format**



Bits 0-5 specify Interrupt and Frame-of-Interest when set. Bit 4, End of Frame, specifies any type of frame except overflow.

**Match Mode Definition**

	Match Mode 1	Match Mode 0	Function
0	0	0	Receiver Disable
1	0	1	Receive All Frames
2	1	0	Receive Station or Broadcast Frames
3	1	1	Receive Station, Broadcast/Multicast Frames

Changing the receive Match Mode bits during frame reception may change chip operation and give unpredictable results.

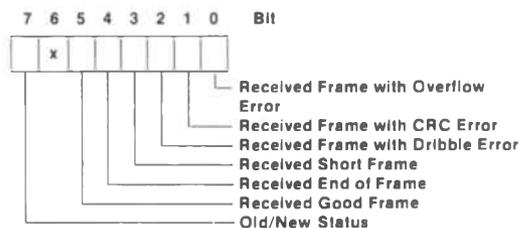
**Interrupt Enable and Frames-of-Interest**

Bits 0-5 when set specify interrupt generation on occurrence of the corresponding frame reception condition. They also specify the corresponding types of frames to be Frames-of-Interest for use by the Receive Status Register to control status loading.

**Receive Status Register**

The Receive Status Register is normally loaded with the status of each received frame when the frame has been received or frame reception has been terminated due to an error condition. In addition, this register contains the Old/New Status bit which is set when the Receive Status Register is read or the chip is reset, and cleared only when new status is loaded for a Frame-of-Interest (as defined by bits 0-5 of the Receive Command Register). All other bits are cleared upon chip reset.

**Receive Status Register Format**



The Old/New Status bit write-protects the Receive Status Register while it contains unread status for a Frame-of-Interest. When this bit is zero, the register is write-protected. The Old/New Status bit is cleared whenever the status of a new Frame-of-Interest is loaded into the Receive Status Register and is set after that status is read. When zero, it indicates "new status for a Frame-of-Interest".

Thus the status of any frame received following the reception of a Frame-of-Interest will not be loaded into the Receive Status Register unless the previous status has been read. If any following frame is received before the status of the previous Frame-of-Interest has been read, the new status will not be loaded, the Receive Discard (RxDC) signal will be issued and the Receive FIFO will be cleared.

With this one exception caused by a write-protect condition, the status of each frame is always loaded into the Receive Status Register on completion of reception.

Any frame received will cause an interrupt to be generated if the corresponding Interrupt Enable bit is set. This interrupt is reset upon reading the Receive Status Register.

These conditions ensure that a maximum number of good frames are received and retained.

from the EDLC chip to the encoder. This clock runs continuously, and is asynchronous to RxC.

**TxD Transmit Data (Output):** Serial data output to the encoder. Active HIGH.

**TxEN Transmit Enable (Output):** This signal is used to activate the encoder. It becomes active when the first bit of the Preamble is transmitted and inactive when the last bit of the frame is transmitted. Active HIGH and cleared by Reset.

**RxC Receive Clock (Input):** 10 MHz, 50% duty cycle nominal. The receive clock is used to synchronize incoming data to the EDLC chip from the decoder. This clock runs continuously, and is asynchronous to  $\overline{\text{TxC}}$ .

**RxD Receive Data (Input):** Serial input data to the EDLC chip from the decoder. Active HIGH.

**CSN Carrier Sense (Input):** Indicates traffic on the coaxial cable to the EDLC chip. Becomes active with the first bit of the Preamble received, and inactive one bit time after the last bit of the frame is received. Active HIGH.

**COLL Collision (Input):** Indicates transmission contention on the Ethernet cable. The Collision input is latched internally. Sampled during transmission, Collision is set by an active high pulse on the COLL input and automatically reset at the end of transmission of the JAM sequence.

**Data Buffer Interface**

**RxTxD (0-7) Receive/Transmit Data Bus (I/O):** Carries Receive/Transmit data byte from/to the EDLC chip Receive/Transmit FIFOs.

**RxTxEOF Receive/Transmit End of Frame (I/O):** Indicates last byte of data on the Receive/Transmit Data Bus. Effectively a ninth bit in the FIFOs with identical timing to RxTxD (0-7). Active HIGH.

**RxRDY Receive Ready (Output):** Indicates that at least one byte of received data is available in the Receive FIFO. This signal will remain active high as long as one byte of data remains in the Receive FIFO. When this condition no longer exists, RxRDY will be deasserted with respect to the leading edge of the  $\overline{\text{RxRD}}$  strobe that removes the last byte of data from the Receive FIFO. RxRD should not be activated if RxRDY is low. Active HIGH and cleared by Reset.

**RxRD Receive Read Strobe (Input):** Enables transfer of received data from the EDLC Receive FIFO to the RxTxD Bus. Data is valid from the EDLC Receive FIFO at the RxTxD pins on the rising edge of this signal. This signal should not be activated unless RxRDY is high. Active LOW.

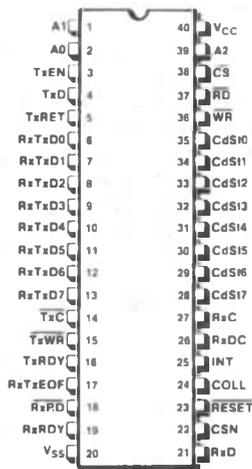


Figure 4. Pin Configuration

**Pin Description**

The EDLC chip has four groups of interface signals:

- Power Supply
- Encoder/Decoder
- Data Buffer
- Command/Status

**Power Supply**

V <sub>CC</sub> .....	+5V
V <sub>SS</sub> .....	Ground

**Encoder/Decoder Interface**

**TxC Transmit Clock (Input):** 10 MHz, 50% duty cycle transmit clock used to synchronize the transmit data

**RxDC Receive Discard (Output):** Asserted when one of the following conditions occurs, and the associated Interrupt Enable bit in the Receive Command Register is reset. (1) Receive FIFO overflow. (2) CRC Error. (3) Short Frame Error. (4) Receive frame address non-match or (5) current frame status lost because previous status was not read. RxDC does not activate on errors when the associated Interrupt Enable bit is set. In this case, EOF will be generated instead when the Receive FIFO is read out. This allows reception of frames with errors. RxDC acts internally to clear the Receive FIFO.

**TxRDY Transmit Ready (Output):** Indicates that the Transmit FIFO has space available for at least one data byte. This signal will remain active high as long as one byte of space exists for transmitted data to be written into. When this condition no longer exists, TxRDY will be deasserted with respect to the leading edge of the TxWR strobe that fills the Transmit FIFO. TxRDY is forced inactive during Reset, and when TxRET is active. Active HIGH. Goes high after Reset.

**TxWR Transmit Write (Input):** Synchronizes data transfer from the RxTxD Bus to the Transmit FIFO. Data is written to the FIFO on the rising edge of this signal. This signal should not be active unless TxRDY is high. Active LOW.

**TxRET Transmit Retransmit (Output):** Asserted whenever either transmit underflow or transmit collision conditions occur. It is nominally 800 ns in width. Active HIGH. Asserted by Reset.

TxRET clears the internal Transmit FIFO.

#### Command/Status Interface

**CdSt (0-7) Command/Status Data Bus (I/O):** These lines carry commands and status as well as station address initialization information between the EDLC chip and CPU. These lines are nominally high impedance until activated by CS and RD being simultaneously active.

**DC Characteristics**  $T_A = 0^\circ\text{C to }70^\circ\text{C}$ ,  $V_{CC} = 4.50\text{ V to }5.50\text{ V}$

Symbol	Parameter	Limits <sup>(1)</sup>			Units	Condition
		Min.	Typ.	Max.		
I <sub>IN</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = 0.45 V to 5.25 V
I <sub>O</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = 0.45 V to 5.25 V
I <sub>CC</sub>	V <sub>CC</sub> Current		150	200	mA	
V <sub>CH</sub>	Clock Input High Voltage	3.5		V <sub>CC</sub> + 1	V	
V <sub>CL</sub>	Clock Input Low Voltage			0.8	V	
V <sub>IL</sub>	Input Low Voltage			0.8	V	
V <sub>IH1</sub>	Input High Voltage	2.0		V <sub>CC</sub> + 1	V	Except TxWR and RxRD
V <sub>IH2</sub>	Input High Voltage	3.0		V <sub>CC</sub> + 1	V	TxWR and RxRD
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA

#### NOTE:

1. Typical values are for  $T_A = 25^\circ\text{C}$  and nominal supply voltages

**A0-A2 Address (0-2) (Input):** Address lines to select the proper EDLC internal registers for reading or writing.

**CS Chip Select (Input):** Chip Select input, must be active in conjunction with RD or WR to successfully access the EDLC internal registers. Active LOW.

**RD Read (Input):** Enables reading of the EDLC internal registers in conjunction with CS. Data from the internal registers is enabled via the falling edge of RD and is valid on the rising edge of the signal. Active LOW.

**WR Write (Input):** Enables writing of the EDLC internal registers in conjunction with CS. Write data on the CdSt (0-7) data lines must be set up relative to the rising edge of the signal. Active LOW.

**INT Interrupt (Output):** Enabled as outlined above by a variety of transmit and receive conditions. Remains active until the status register containing the reason for the interrupt is read. Active HIGH.

**RESET (Input):** Initializes control logic, clears command registers, clears the Transmit Status Register, clears bits 0-5 of the Receive Status Register, sets the Old/New Status bit (bit 7 of the Receive Status Register), asserts RxDC and TxRET and clears the Receive and Transmit FIFOs. In addition, TxRDY is forced low during a reset. TxRDY goes high when RESET goes high, indicating the EDLC chip is ready to transmit. RESET is active LOW.

#### Absolute Maximum Ratings

Ambient Temperature  
 Under Bias .....  $-10^\circ\text{C to }+80^\circ\text{C}$   
 Storage Temperature .....  $-65^\circ\text{C to }+150^\circ\text{C}$   
 All Input or Output Voltages  
 with Respect to Ground .....  $+6\text{ V to }-0.3\text{ V}$   
 Package Maximum Power Dissipation ..... 1.5 Watts

**Operating Conditions**

Ambient Temperature Range . . . . . 0°C to 70°C  
 V<sub>CC</sub> Power Supply . . . . . 4.50 V to 5.50 V

**AC Test Conditions**

Output Load: 1 Schottky TTL Gate + CL = 100 pF  
 (All pins except TxEN, TxD)  
 TxEN, TxD Load: 1 Schottky TTL Gate + CL = 35 pF  
 Input Pulse Level: 0.4 V to 2.4 V  
 Timing Reference Level: 1.5 V

**Capacitance**<sup>[6]</sup> T<sub>A</sub> = 25°C, F<sub>C</sub> = 1 MHz

Symbol	Parameter	Maximum	Condition
C <sub>IN</sub>	Input Capacitance	15 pF	V <sub>IN</sub> = 0 V
C <sub>I/O</sub>	I/O Capacitance	15 pF	V <sub>I/O</sub> = 0 V

**A.C. Characteristics** T<sub>A</sub> = 0°C to 70°C, V<sub>CC</sub> = 4.50 V to 5.50 V

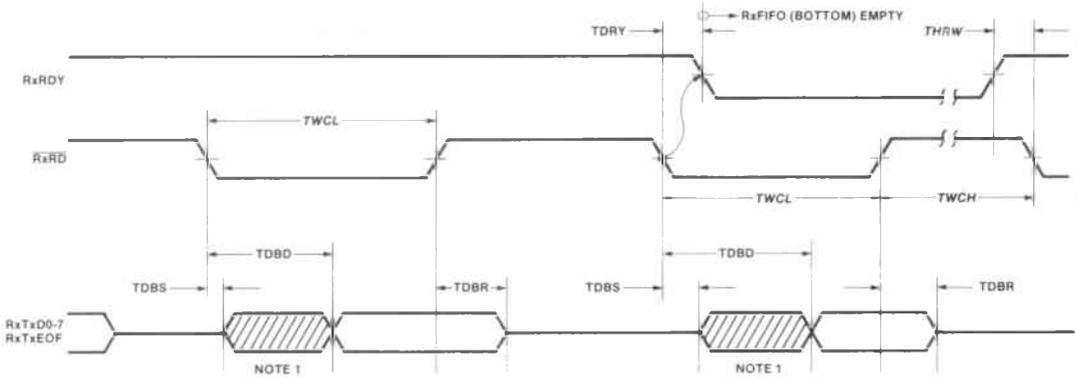
Symbol <sup>[5]</sup>	Parameter	Limits			Units (ns)	Condition
		Min.	Typ.	Max.		
<b>DATA AND COMMAND/STATUS INTERFACE TIMING</b>						
TDBD	RxTx/CdSt Bus Data Delay			150	ns	
TDBR	RxTx/CdSt Bus Release Delay	10			ns	
TDBS	RxTx/CdSt Bus Seizure Delay	10		150	ns	
TDRY	RxRDY/TxRDY Clear Delay			100	ns	
THAR	A <sub>0-2</sub> /CS Hold	10			ns	
THDA	RxTx/CdSt Bus Hold	0			ns	
THRW	RxRD/TxWR Hold	0			ns	
TSAR	A <sub>0-2</sub> /CS Setup	0			ns	
TSCS	CdSt Bus Setup	90			ns	
TSRT	RxTx Bus Setup	90			ns	
TWCH	RxRD/TxWR/RD//WR High Width	100			ns	
TWCL	RxRD/TxWR/RD//WR Low Width	200		10,000	ns	

<b>SERIAL TRANSMIT AND RECEIVE INTERFACE TIMING</b>						
TDDC	RxDC Set Delay	800			ns	Note 1
TDIC	INT Clear Delay			150	ns	
TDRE	TxRET Set Delay	2400		3400	ns	Note 3
TDRI	Receive INT Delay	1000			ns	Note 2
TDTD	TxD/TxEN Delay	20		60	ns	Cl = 35 pF
TDTI	Transmit INT Delay	1200			ns	Note 4
THRD	RxD Hold	20			ns	
TPCK	RxC/TxC Clock Period	95		1000	ns	
TSRD	RxD Setup	30			ns	
TWDC	RxDC High Width	600			ns	
TWRC	RxC High/Low Width	45			ns	
TWRE	TxRET High Width	600			ns	
TWRS	RESET Low Width	10,000			ns	
TWTC	TxC High/Low Width	45			ns	
TWCO	COLL Width	50			ns	

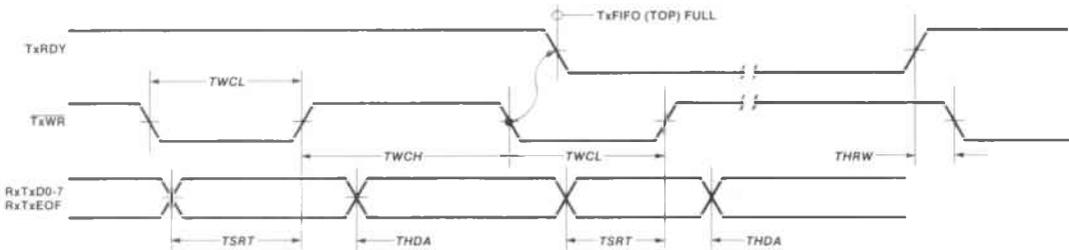
**NOTES:**

- For frame reception with Shortframe or CRC Error. If frame reception is terminated due to Overflow, RxDC will be issued within 1.2 μs of Overflow. If frame reception is terminated due to non-match of address, RxDC will be issued within 2.4 μs of the receipt of the last address bit.
- Normal frame reception without Overflow. If frame reception is terminated due to Overflow, INT will be issued within 1.2 μs of Overflow.
- For TxRET caused by Collision or 16 Collision condition. If transmission is terminated due to Underflow TxRET will be issued within 1.2 μs of the Underflow.
- For INT caused by Collision or 16 Collision condition. If caused by Underflow, INT will be issued within 1.2 μs. If caused by normal termination, INT will be issued within 200 ns of TxEN going LOW.
- Italics indicate input requirement, non-italics indicate output timing.
- Characterized, not tested.

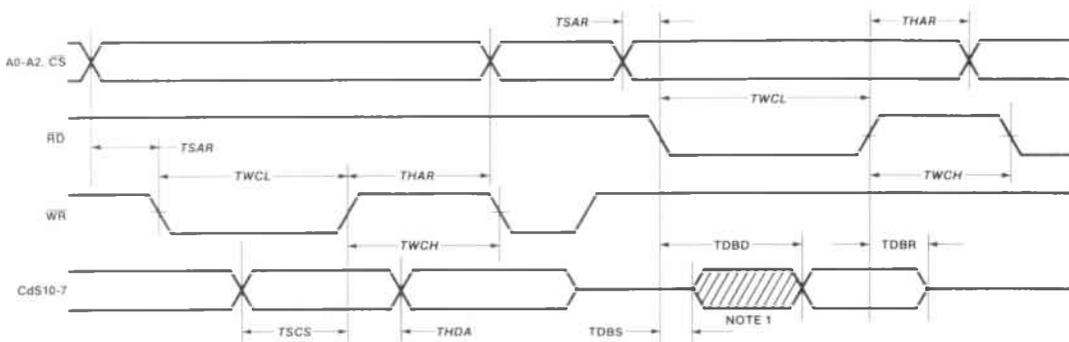
RECEIVE DATA INTERFACE TIMING



TRANSMIT DATA INTERFACE TIMING

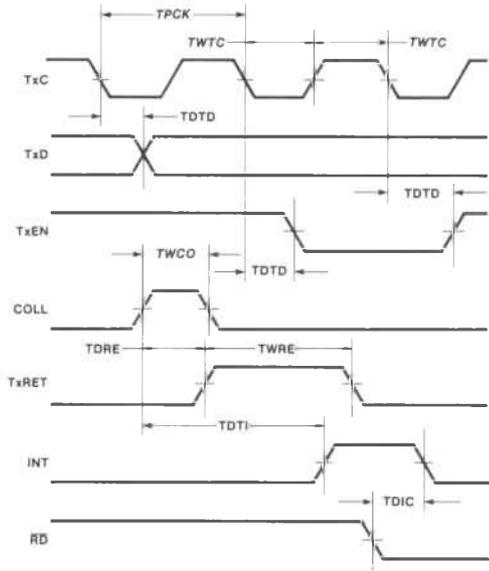


COMMAND/STATUS INTERFACE TIMING

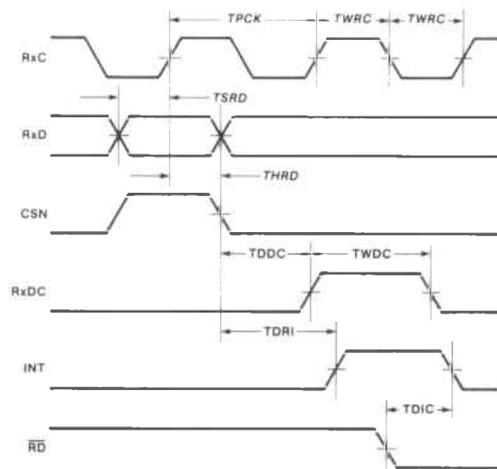


NOTE 1: BUS IS DRIVEN AT THIS TIME. HOWEVER, NO VALID INFORMATION PRESENT.

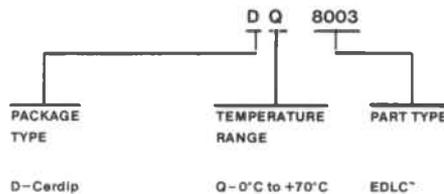
SERIAL TRANSMIT INTERFACE TIMING



SERIAL RECEIVE INTERFACE TIMING



Ordering Information



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### Features

- Compatible with IEEE 802.3 and Ethernet Rev. 1 Specification
- Compatible with the 8003 EDLC™, 8005 Advanced EDLC
- Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)
- Receiver and Collision Squelch Circuit and Noise Rejection Filter
- Differential TRANSMIT Cable Driver
- Loopback Capability for Diagnostics and Isolation
- Fail-Safe Watchdog Timer Circuit to Prevent Continuous Transmission
- 20 MHz Crystal Oscillator
- Transceiver Interface High Voltage (16 V) and Low Voltage Short Circuit Protection
- Low Power CMOS Technology with Single 5V Supply
- 20 pin DIP & PLCC Packages

### Description

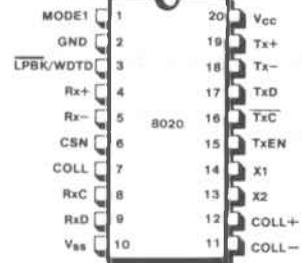
The SEEQ 8020 Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 and 8005 Controllers and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The SEEQ 8020 MCC™ is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8020 includes a watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

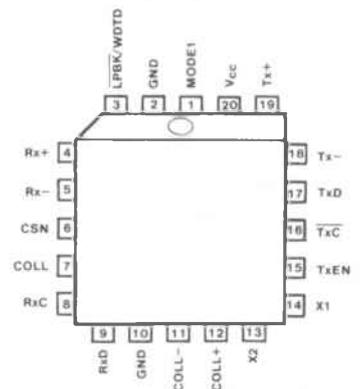
Together with the 8003 or 8005 and a transceiver, the 8020 Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

### Pin Configuration

DUAL-IN LINE  
TOP VIEW



PLASTIC LEADED CHIP CARRIER  
TOP VIEW



### Functional Block Diagram

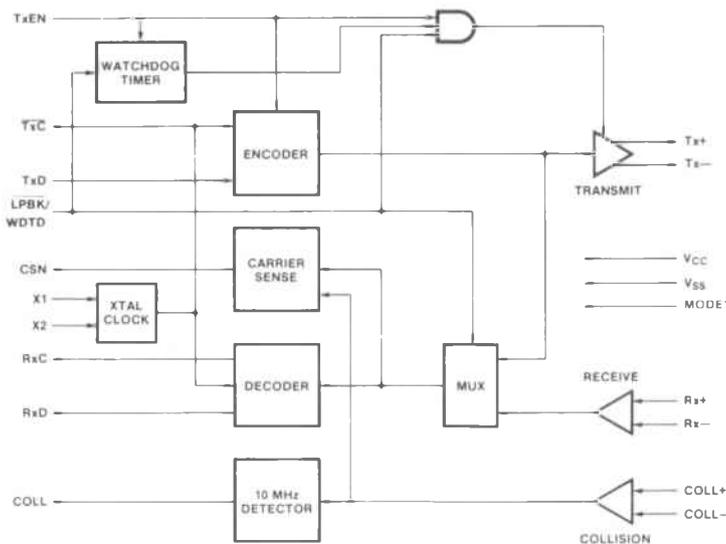


Figure 1. 8020 MCC™ Manchester Code Converter Block Diagram.

## Functional Description

The 8020 Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8020 MCC™ recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1," and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exclusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

### Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz  $\pm 0.01\%$  transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

### Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complement of the data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

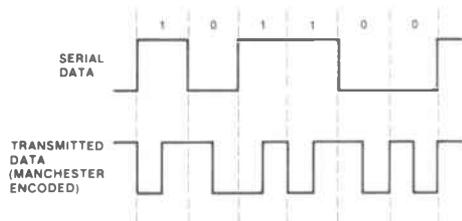


Figure 2. Manchester Coding

Data encoding and transmission begin with TxEN going active; the first transition is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and the transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero. To eliminate DC current in the transformer during idle, Tx± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

### Watchdog Timer

A watchdog timer is built on chip. It can be enabled or disabled by the LPBK/WDTD signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

### Differential Input Circuit (Rx+ and Rx-, COLL+ and COLL-)

As shown in Figure 3, the differential input for Rx+ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2  $\Omega \pm 1\%$  resistors in series for proper impedance matching.

The center tap has a 0.01  $\mu\text{F}$  capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

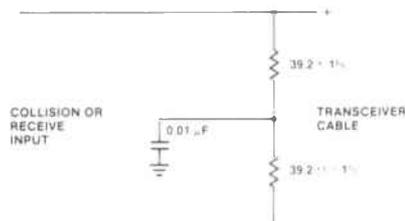


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signals less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) are always rejected, signals greater than -300 mV and wider than 30 ns (18 ns for collision pair) are always accepted.

#### **Manchester Decoder and Clock Recovery Circuit**

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to -8.25 ns within 12 bit cell times worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to -8.25 ns. The Rx $\overline{C}$  high or low time will always be greater than 40 ns. If MODE2 to high or floating, Rx $\overline{C}$  will be held low for 1.2  $\mu$ s maximum while the PLL is acquiring lock. If MODE2 is low, Rx $\overline{C}$  follows Tx $\overline{C}$  for the first 1.2  $\mu$ s and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after the node has finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5  $\mu$ s regardless of the state of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhibit period after packet reception. During clock switching, Rx $\overline{C}$  may stay high for 200ns maximum.

#### **Collision Circuit**

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz  $\pm$ 15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with Rx $\overline{C}$ . However, if a collision arrives during inhibit period 4.5  $\mu$ s from the time CSN was deasserted, CSN will not be reasserted.

#### **Loopback**

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except the differential output driver and the differential input receiver circuits which are disabled during loopback. At the end of frame transmission, the 8020 also generates a 650 ns long COLL signal

550 ns after CSN was deasserted to simulate the IEEE 802.3 SQE test. The watchdog timer remains enabled in this mode.

### **Pin Description**

The MCC™ chip signals are grouped into four categories:

- Power Supply and Clock
- Controller Interface
- Transceiver Interface
- Miscellaneous

#### **Power Supply**

V<sub>CC</sub> ..... +5V  
V<sub>SS</sub> ..... Ground

**X1 and X2 Clock (Inputs):** Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.

#### **Controller Interface**

**RxC Receive Clock (Output):** This signal is the recovered clock from the phase decoder circuit. It is switched to Tx $\overline{C}$  when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible.

**RxD Receive Data (Output):** The RxD signal is the recovered data from the phase decoder. During idle periods, the RxD pin is LOW under normal conditions. TTL and MOS level compatible. Active HIGH.

**CSN Carrier Sense (Output):** The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with Rx $\overline{C}$ . TTL compatible.

**TxC Transmit Clock (Output):** A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL and MOS level compatible.

**TxD Transmit Data (Input):** TxD is the NRZ serial input data to be transmitted. The data is clocked into the MCC by Tx $\overline{C}$ . Active HIGH, TTL compatible.

**TxEN Transmit Enable (Input):** Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with Tx $\overline{C}$ . TxEN goes active with the first bit of transmission. TTL compatible.



**Loopback:** When this pin is brought low, the Manchester encoded transmit data from TxD and Tx̄C is routed through the receiver circuit and sent back onto the Rx̄D and Rx̄C Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.

**Watchdog Timer Disable:** When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for too long, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx+ and Tx- lines. The watchdog timer is automatically reset each time TxEN is deasserted.

**Interconnection to a Data Link Controller**

Figure 5 shows the interconnections between the 8020 MCC™ and SEEQ's 8003 or 8005. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

- Transmit Data, Tx̄D
- Transmit Clock, Tx̄C
- Transmit Enable, TxEN
- Collision, COLL

Receiver connections are:

- Receive Data, Rx̄D
- Receive Clock, Rx̄C
- Carrier Sense, CSN

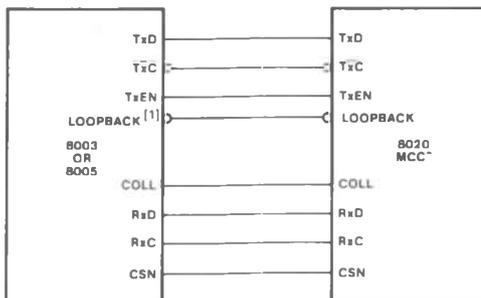


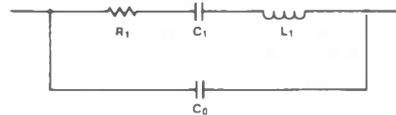
Figure 5. Interconnection of 8020 and 8003/8005

**NOTE**

1. Loopback output on 8005 only.

**D.C. and A.C. Characteristics and Timing Crystal Specification**

Resonant Frequency ( $C_L = 20$ pF) .....	20 MHz
	$\pm 0.005\%$ 0-70° C
	and $\pm 0.003\%$ at 25° C
Type .....	Fundamental Mode
Circuit .....	Parallel Resonance
Load Capacitance ( $C_L$ ) .....	20 pF
Shunt Capacitance ( $C_0$ ) .....	7 pF Max.
Equivalent Series Resistance ( $R_1$ ) .....	25 $\Omega$ Max.
Motional Capacitance ( $C_1$ ) .....	0.02 pF Max.
Drive Level .....	2 mW



EQUIVALENT CIRCUIT OF CRYSTAL

Figure 6.

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**Absolute Maximum Ratings\***

Storage Temperature .....	-65° C to 150° C
All Input and Output Voltage .....	-0.3 to $V_{CC} + 0.3$
$V_{CC}$ .....	-0.3 to 7V
( $Rx\pm$ , $Tx\pm$ , $COLL\pm$ ) High Voltage	
Short Circuit Immunity .....	-0.3 to 16V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**DC Characteristics**  $T_A=0^\circ\text{C}$  to  $70^\circ\text{C}$ ;  $V_{CC}=5\text{V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Unit	Conditions
$I_{IL}$	Input Leakage Current (except MODE1, Receive and Collision Pairs)		10	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{CC}$
	MODE1 Input Leakage Current		200	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{CC}$
	Receive and Collision Pairs ( $Rx\pm$ , $COLL\pm$ ) Input Leakage Current		2	$\text{mA}$	$V_{IN} = 0$
$I_{CC}$	$V_{CC}$ Current		75	$\text{mA}$	All Inputs, Outputs Open
$V_{IL}$	TTL Input Low Voltage	-0.3	0.8	V	
$V_{IH}$	TTL Input High Voltage (except X1)	2.0	$V_{CC} + 0.3$	V	
	X1 Input High Voltage	3.5	$V_{CC} + 0.3$	$\pm 1.2$	V
$V_{OL}$	TTL Output Low Voltage except TxC		0.4	V	$I_{OL} = 2.1\text{ mA}$
	TxC Output Low Voltage		0.4	V	$I_{OL} = 4.2\text{ mA}$
$V_{OH}$	TTL Output High Voltage (except RxC, TxC, RxD)	2.4		V	$t_{OH} = -400\mu\text{A}$
	RxC, TxC, RxD Output High Voltage	3.9		V	$t_{OH} = -400\mu\text{A}$
$V_{ODF}$	Differential Output Swing	$\pm 0.55$	$\pm 1.2$	V	78 $\Omega$ Termination Resistor and 243 $\Omega$ Load Resistors
$V_{OCM}$	Common Mode Output Voltage	$V_{CC} - 2.5$	$V_{CC} - 1$	V	78 $\Omega$ Termination Resistor and 243 $\Omega$ Load Resistors
$V_{BKSV}$	$Tx\pm$ Backswing Voltage During Idle		0.1	V	Shunt inductive load $\leq 27\ \mu\text{H}$
$V_{IDF}$	Input Differential Voltage (measured differentially)	$\pm 0.3$	$\pm 1.2$	V	
$V_{ICM}$	Input Common Mode Voltage	0	$V_{CC}$	V	
$C_{IN}^{[1]}$	Input Capacitance		15	$\text{pF}$	
$C_{OUT}^{[1]}$	Output Capacitance		15	$\text{pF}$	

**NOTE:**

1. Characterized. Not tested.

**A.C. Test Conditions**

Output Loading TTL Output:	1 TTL gate and 20 pF capacitor
Differential Output:	243 $\Omega$ resistor and 10 pF capacitor from each pin to $V_{SS}$ and a termination 78 $\Omega$ resistor load resistor in parallel with a 27 $\mu$ H inductor between the two differential output pins
Differential Signal Delay Time Reference Level:	50% point of swing
Differential Output Rise and Fall Time:	20% to 80% points
$RxC$ , $\overline{Tx}C$ , X1 High and Low Time:	High time measured at 3.0V Low time measured at 0.6V
$RxD$ , $RxC$ , $\overline{Tx}C$ , X1 Rise and Fall Time:	Measured between 0.6V and 3.0V points
TTL Input Voltage (except X1):	0.8V to 2.0V with 10 ns rise and fall time
X1 Input Voltage:	0.8V to 3.5V with 5 ns rise and fall time
Differential Input Voltage:	At least $\pm 300$ mV with rise and fall time of 10 ns measured between $-0.2V$ and $+0.2V$

**20 MHz TTL Clock Input Timing**  $T_A=0^\circ C$  to  $70^\circ C$ ;  $V_{CC}=5 V \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_1$	X1 Cycle Time	49.995	50.005	ns
$t_2$	X1 High Time	15		ns
$t_3$	X1 Low Time	15		ns
$t_4$	X1 Rise Time		5	ns
$t_5$	X1 Fall Time		5	ns
$t_{5A}$	X1 to $\overline{Tx}C$ Delay Time	10	45	ns

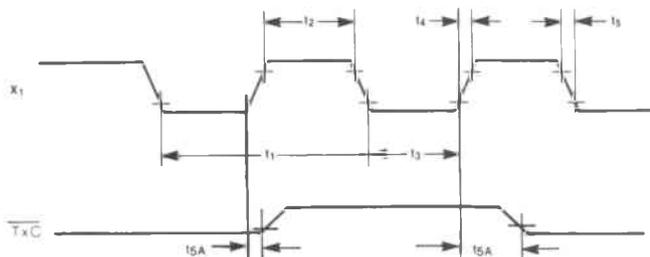


Figure 12. 20 MHz TTL Clock Timing

**Transmit Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_6^{[1]}$	TxC Cycle Time	99.99	100.01	ns
$t_7$	TxC High Time	40		ns
$t_8$	TxC Low Time	40		ns
$t_9^{[1]}$	TxC Rise Time		5	ns
$t_{10}^{[1]}$	TxC Fall Time		5	ns
$t_{11}$	TxEN Setup Time	40		ns
$t_{12}$	TxD Setup Time	40		ns
$t_{13}^{[1]}$	Bit Center to Bit Center Time	99.5	100.5	ns
$t_{14}^{[1]}$	Bit Center to Bit Boundary Time	49.5	50.5	ns
$t_{15}^{[1]}$	Tx+ and Tx- Rise Time		5	ns
$t_{16}^{[1]}$	Tx+ and Tx- Fall Time		5	ns
$t_{17}$	Transmit Active Time From The Last Positive Transition	200		ns
$t_{17A}^{[1]}$	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 100 mV of 0 V	400	600	ns
$t_{17B}^{[1]}$	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 40 mV of 0 V		7000	ns
$t_{18}$	Tx+ and Tx- Output Delay Time		70	ns
$t_{19}$	TxD Hold Time	15		ns
$t_{20}$	TxEN Hold Time	15		ns

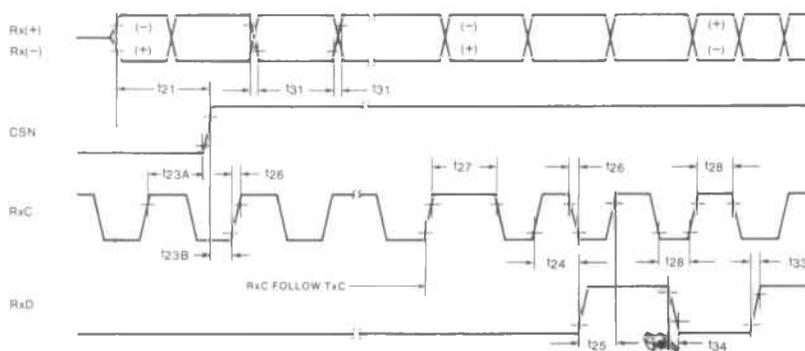
## NOTE:

1. Characterized. Not tested.



**Receive Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_{21}$	CSN Assert Delay Time		240	ns
$t_{22}$	CSN Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
$t_{23A}$	CSN Hold Time	30		ns
$t_{23B}$	CSN Set up Time	30		ns
$t_{24}$	RxD Hold Time	30		ns
$t_{25}$	RxD Set up Time	30		ns
$t_{26}^{[1]}$	RxC Rise and Fall Time		5	ns
$t_{27}^{[1]}$	During Clock Switch RxC Keeps High Time	40	200	ns
$t_{28}$	RxC High and Low Time	40		ns
$t_{29}^{[1]}$	RxC Clock Cycle Time (during data period)	95	105	ns
$t_{30}$	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	$\mu\text{s}$
$t_{31}$	Rx+/Rx- Rise and Fall Time		10	ns
$t_{32}^{[1]}$	Rx+/Rx- Begin Return to Zero from Last Positive-Going Transition	160		ns
$t_{33}^{[1]}$	RxD Rise Time		10	ns
$t_{34}^{[1]}$	RxD Fall Time		10	ns


**Figure 9. Receive Timing-Start of Packet**
**NOTE:**

1. Characterized. Not tested.

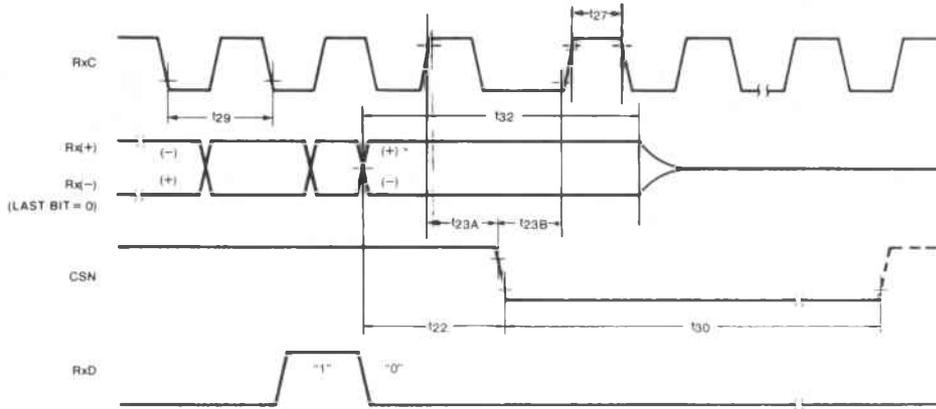


Figure 10. Receive Timing - End of Packet

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**Collision Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_{51}$	COLL+/COLL— Cycle Time	86	118	ns
$t_{52}$	COLL+/COLL— Rise and Fall Time		10	ns
$t_{53}$	COLL+/COLL— High and Low Time	35	70	ns
$t_{54}$	COLL+/COLL— Width (measured at $-0.3\text{V}$ )	26		ns
$t_{55}$	COLL Asserts Delay Time		300	ns
$t_{56}$	COLL Deasserts Delay Time		500	ns
$t_{57}$	CSN Asserts Delay Time		400	ns
$t_{58}$	CSN Deasserts Delay Time		600	ns

**Notes:**

- COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with RxC.
- If COLL+ and COLL- arrives within  $4.5\mu\text{s}$  from the time CSN was deasserted; CSN will not be reasserted (on transmission node only)
- When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active
- When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for  $4.5\mu\text{s}$ .

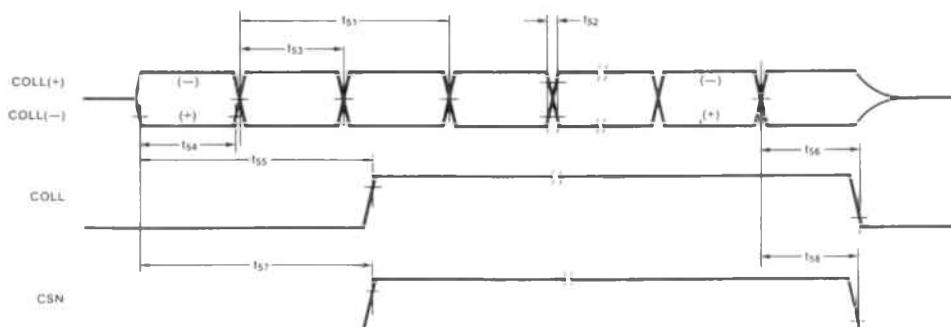


Figure 11. Collision Timing

**Loopback Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
t <sub>61</sub>	LPBK Setup Time	500		ns
t <sub>62</sub>	LPBK Hold Time	5		$\mu\text{S}$
t <sub>63</sub>	In Collision Simulation, COLL Signal Delay Time	475	625	ns
t <sub>64</sub>	COLL Duration Time	600	750	ns

**Note:**

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period.

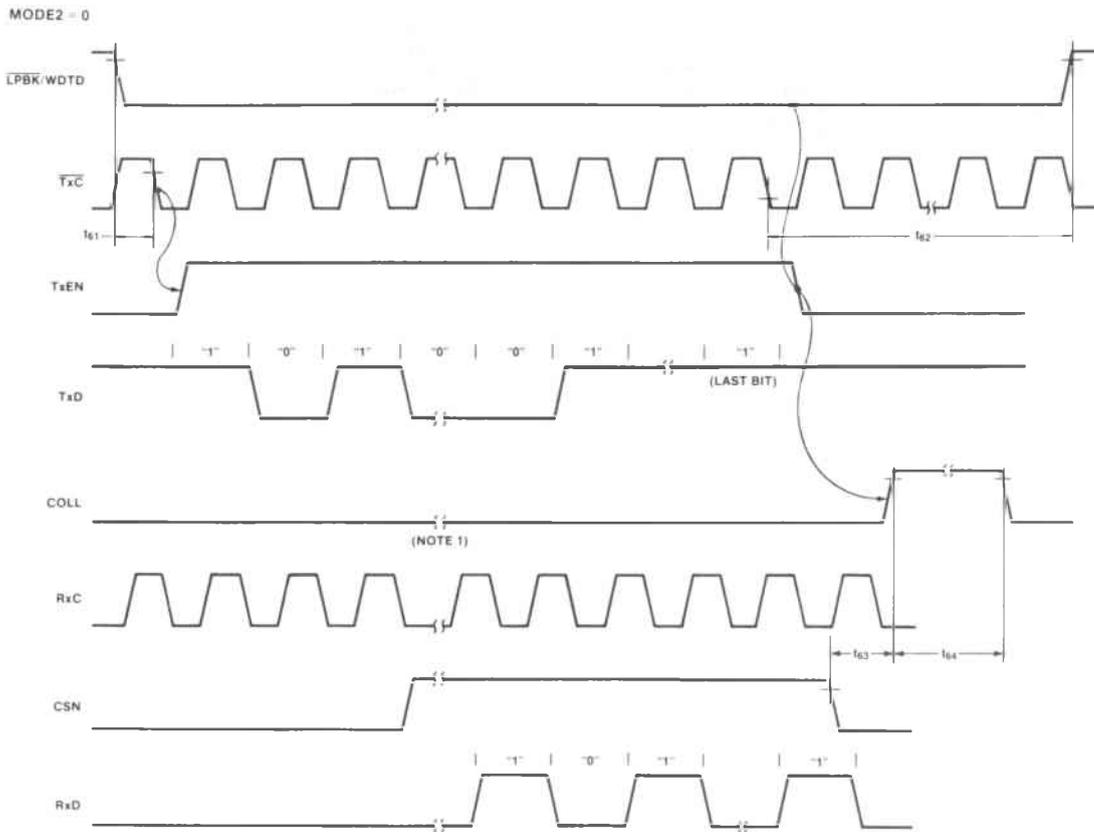
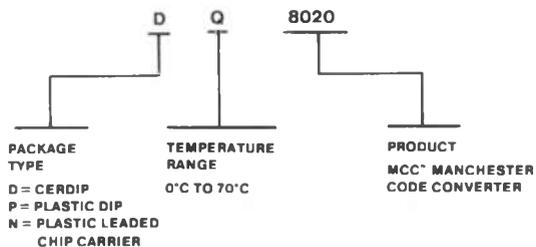


Figure 13. Loopback Timing

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**Ordering Information**



## MCC™ Manchester Code Converter

March 1987

### Features

- Compatible with IEEE 802.3 and Ethernet Rev. 1 Specification
- Compatible with the 8003 EDLC™, 8005 Advanced EDLC and Intel 82586 LAN Controller
- Manchester Data Encoding/Decoding and Receiver Clock Recovery with Phase Locked Loop (PLL)
- Receiver and Collision Squelch Circuit and Noise Rejection Filter
- Differential TRANSMIT Cable Driver
- Loopback Capability for Diagnostics and Isolation
- Fall-Safe Watchdog Timer Circuit to Prevent Continuous Transmission
- 20 MHz Crystal Oscillator
- Transceiver Interface High Voltage (16 V) and Low Voltage Short Circuit Protection
- Low Power CMOS Technology with Single 5V Supply
- 20 pin DIP & PLCC Packages

### Description

The SEEQ 8023A Manchester Code Converter chip provides the Manchester data encoding and decoding functions of the Ethernet Local Area Network physical layer. It interfaces to the SEEQ 8003 and 8005 Ethernet Data Link Controllers or to the Intel 82586 LAN Controller and any standard Ethernet transceiver as defined by IEEE 802.3 and Ethernet Revision 1.

The SEEQ 8023A MCC™ is a functionally complete Encoder/Decoder including ECL level balanced driver and receivers, on board oscillator, analog phase locked loop for clock recovery and collision detection circuitry. In addition, the 8023A includes a 25 millisecond watchdog timer, a 4.5 microsecond window generator, and a loopback mode for diagnostic operation.

Together with the 8003 or 8005 and a transceiver, the 8023A Manchester Code Converter provides a high performance minimum cost interface for any system to Ethernet.

### Functional Block Diagram

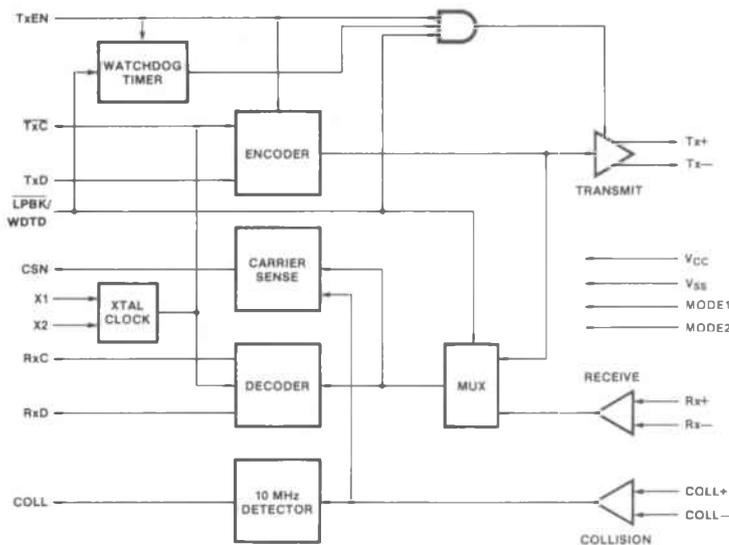
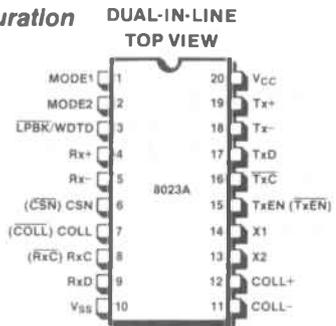
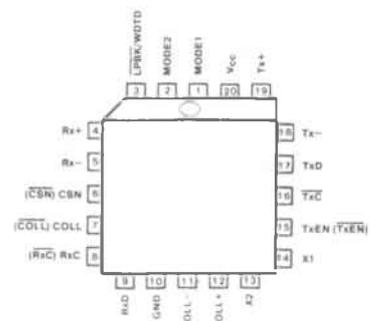


Figure 1. 8023A MCC™ Manchester Code Converter Block Diagram.

### Pin Configuration



### PLASTIC LEADED CHIP CARRIER TOP VIEW



MICRO/  
DATA COM

## Functional Description

The 8023A Manchester Code Converter chip has two portions, transmitter and receiver. The transmitter uses Manchester encoding to combine the clock and data into a serial stream. It also differentially drives up to 50 meters of twisted pair transmission line. The receiver detects the presence of data and collisions. The 8023A MCC™ recovers the Manchester encoded data stream and decodes it into clock and data outputs. Manchester Encoding is the process of combining the clock and data stream so that they may be transmitted on a single twisted pair of wires, and the clock and data may be recovered accurately upon reception. Manchester encoding has the unique property of a transition at the center of each bit cell, a positive going transition for a "1", and a negative going transition for a "0" (See Figure 2). The encoding is accomplished by exclusive-ORing the clock and data prior to transmission, and the decoding by deriving the clock from the data with a phase locked loop.

### Clock Generator

The internal oscillator is controlled by a 20 MHz parallel resonant crystal or by an external clock on X1. The 20 MHz clock is then divided by 2 to generate a 10 MHz  $\pm 0.01\%$  transmitter clock. Both 10 MHz and 20 MHz clocks are used in Manchester data encoding.

### Manchester Encoder and Differential Output Driver

The encoder combines clock and data information for the transceiver. In Manchester encoding, the first half of the bit cell contains the complement of the data and the second half contains the true data. Thus, a transition is always guaranteed in the middle of a bit cell.

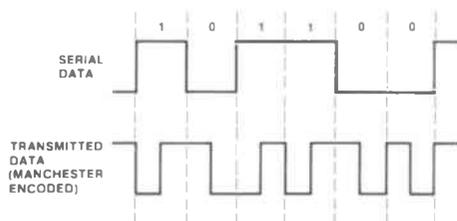


Figure 2. Manchester Coding

Data encoding and transmission begin with TxEN going active; the first transition is always positive for Tx(-) and negative for Tx(+). In IEEE mode, at the termination of a transmission, TxEN goes inactive and the transmit pair approach to zero differential. In Ethernet mode, at the end of the transmission, TxEN goes inactive and the transmit pair stay differentially high. The transmit termination can occur at bit cell center if the last bit is a one or at a bit boundary if the last bit is a zero. To eliminate DC current in the transformer during idle, Tx± is brought to 100 mV differential in 600 ns after the last transition (IEEE mode). The back swing voltage is guaranteed to be less than .1 V.

### Watchdog Timer

A 25 ms watchdog timer is built on chip. It can be enabled or disabled by the  $\overline{\text{LPBK}}/\text{WDTD}$  signal. The timer starts counting at the beginning of the transmission. If TxEN goes inactive before the timer expires, the timer is reset and ready for the next transmission. If the timer expires before the transmission ends, transmission is aborted by disabling the differential transmitter. This is done by idling the differential output drivers (differential output voltage becomes zero) and deasserting CSN.

### Differential Input Circuit (Rx+ and Rx-, COLL+ and COLL-)

As shown in Figure 3, the differential input for Rx+ and Rx- and COLL+ and COLL- are externally terminated by a pair of 39.2  $\Omega \pm 1\%$  resistors in series for proper impedance matching.

The center tap has a 0.01  $\mu\text{F}$  capacitor, tied to ground, to provide the AC common mode impedance termination for the transceiver cable.

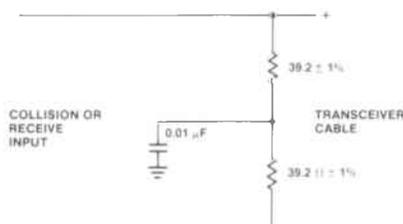


Figure 3. Differential Input Terminator

Both collision and receiver input circuits provide a static noise margin of -140 mV to -300 mV (peak value). Noise rejection filters are provided at both input pairs to prevent spurious signals. For the receiver pair, the range is 15 ns to 30 ns. For the collision pair, the range is 10 ns to 18 ns. The D.C. threshold and noise rejection filter assure that differential receiver data signals less than -140 mV in amplitude or narrower than 15 ns (10 ns for collision pair) are always rejected, signals greater than -300 mV and wider than 30 ns (18 ns for collision pair) are always accepted.

#### Manchester Decoder and Clock Recovery Circuit

The filtered data is processed by the data and clock recovery circuit using a phase-locked loop technique. The PLL is designed to lock onto the preamble of the incoming signal with a transition width asymmetry not greater than +8.25 ns to -8.25 ns within 12 bit cell times worst case and can sample the incoming data with a transition width asymmetry of up to +8.25 ns to -8.25 ns. The Rx $\bar{C}$  high or low time will always be greater than 40 ns. If MODE 2 is high or floating, Rx $\bar{C}$  will be held low for 1.2  $\mu$ s maximum while the PLL is acquiring lock. If MODE2 is low, Rx $\bar{C}$  follows Tx $\bar{C}$  for the first 1.2  $\mu$ s and then switches to the recovered clock. In addition, the Encoder/Decoder asserts the CSN signal while it is receiving data from the cable to indicate the receiver data and clock are valid and available. At the end of frame, after the node has finished transmitting, CSN is deasserted and will not be asserted again for a period of 4.5  $\mu$ s regardless of the state of the state of the receiver pair or collision pair. This is called the inhibit period. There is no inhibit period after packet reception. During clock switching, Rx $\bar{C}$  may stay high for 200ns maximum.

#### Collision Circuit

A collision on the Ethernet cable is sensed by the transceiver. It generates a 10 MHz  $\pm$ 15% differential square wave to indicate the presence of the collision. During the collision period, CSN is asserted asynchronously with Rx $\bar{C}$ . However, if a collision arrives during inhibit period 4.5  $\mu$ s from the time CSN was deasserted, CSN will not be reasserted.

#### Loopback

In loopback mode, encoded data is switched to the PLL instead of Tx+/Tx- signals. The recovered data and clock are returned to the Ethernet Controller. All the transmit and receive circuits, including noise rejection filter, are tested except the differential output driver and the differential input receiver circuits which are disabled during loopback. At the end of frame transmission,

the 8023A also generates a 650 ns long COLL signal 550 ns after CSN was deasserted to simulate the IEEE 802.3 SQE test. The watchdog timer remains enabled in this mode.

#### Pin Description

The MCC™ chip signals are grouped into four categories:

- Power Supply and Clock
- Controller Interface
- Transceiver Interface
- Miscellaneous

#### Power Supply

V<sub>CC</sub> ..... +5V  
V<sub>SS</sub> ..... Ground

**X1 and X2 Clock (Inputs):** Clock Crystal: 20 MHz crystal oscillator input. Alternately, pin X1 may be used as a TTL level input for external timing by floating pin X2.

#### Controller Interface

**RxC ( $\bar{R}x\bar{C}$ ) Receive Clock (Output):** This signal is the recovered clock from the phase decoder circuit. It is switched to Tx $\bar{C}$  when no incoming data is present from which a true receive clock is derived. 10 MHz nominal and TTL compatible. If the MODE2 signal is high, Rx $\bar{C}$  is inverted ( $\bar{R}x\bar{C}$ ) and there is a 1.25  $\mu$ sec discontinuity at the beginning of frame reception.

**RxD Receive Data (Output):** The Rx $\bar{D}$  signal is the recovered data from the phase decoder. During idle periods, the Rx $\bar{D}$  pin is LOW under normal conditions. However, if the MODE2 signal is HIGH, the Rx $\bar{D}$  output will be HIGH during idle. TTL and MOS level compatible. Active HIGH.

**CSN ( $\bar{C}S\bar{N}$ ) Carrier Sense (Output):** The Carrier Sense Signal indicates to the controller that there is activity on the coaxial cable. It is asserted when receive data is present or when a collision signal is present. It is deasserted at the end of frame or at the end of collision, whichever occurs later. It is asserted or deasserted synchronously with Rx $\bar{C}$ . TTL compatible. Normally active HIGH, unless MODE2 is HIGH, in which case  $\bar{C}S\bar{N}$  is active LOW.

**TxC Transmit Clock (Output):** A 10 MHz signal derived from the internal oscillator. This clock is always active. TTL and MOS level compatible.

**TxD Transmit Data (Input):** Tx $\bar{D}$  is the NRZ serial input data to be transmitted. The data is clocked into the MCC by Tx $\bar{C}$ . Active HIGH, TTL compatible.

**TxEN (TxEN) Transmit Enable (Input):** Transmit Enable, when asserted, enables data to be sent to the cable. It is asserted synchronously with Tx̄C. TxEN goes active with the first bit of transmission. TTL compatible. If MODE2 is HIGH, TxEN is inverted.

**COLL (COLL) Collision (Output):** When asserted, indicates to the controller the simultaneous transmission of two or more stations on network cable. TTL compatible. If MODE2 is HIGH, COLL is inverted.

#### Transceiver Interface

**Rx+ and Rx- Differential Receiver Input Pair (Input):** Differential receiver input pair which brings the encoded receive data to the 8023A. The last transition is always positive-going to indicate the end of the frame.

**COLL+ and COLL- Differential Collision Input Pair (Input):** This is a 10 MHz  $\pm 15\%$  differential signal from the transceiver indicating collision. The duty cycle should not be worse than 60%/40% — 40%/60%. The last transition is positive-going. This signal will respond to signals in the range of 5 MHz to 11.5 MHz. Collision signal may be asserted if 'MAU not available' signal is present.

**Tx+ and Tx- Differential Transmit Output Pair (Output):** Differential transmit pair which sends the encoded data to the transceiver. The cable driver buffers are source follower and require external 243  $\Omega$  resistors to ground as loading. These resistors must be rated at 1 watt to withstand the fault conditions specified by IEEE 802.3. If MODE1=1, after 200 ns following the last transition, the differential voltage is slowly reduced to zero volts in 8  $\mu$ s to limit the back swing of the coupling transformer to less than 0.1 V.

#### Miscellaneous

**MODE1 (Input):** This pin is used to select between AC or DC coupling. When it is tied high or left floating, the output drivers provide differential zero signal during idle (IEEE 802.3 specification). When pin 1 is tied low, the output is differentially high when idle (Ethernet Rev. 1 specification).

**MODE2 (Input):** The MODE2 Input signal is normally active LOW. In this configuration, the 8023A operates in a mode compatible with the SEEQ 8003. An alternate mode of operation may be achieved by configuring the MODE signal active HIGH, or by allowing it to float HIGH with its internal pullup. In this configuration, Rx̄C, TxEN, CSN and COLL become active LOW. In addition, Rx̄D is HIGH during idle, and Rx̄C has a 1.2  $\mu$ s discontinuity during signal acquisition.

**LPBK/WDTD Loopback/Watchdog Timer Disable (Input):**

**Normal Operation:** For normal operation this pin should be HIGH or tied to V<sub>CC</sub>. In normal operation the watchdog timer is enabled.

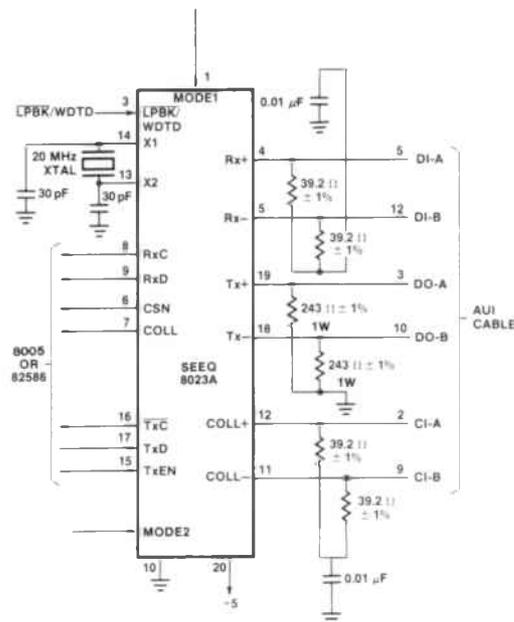


Figure 4. 8023A Interface

**Loopback:** When this pin is brought low, the Manchester encoded transmit data from Tx<sub>D</sub> and Tx<sub>C</sub> is routed through the receiver circuit and sent back onto the Rx<sub>D</sub> and Rx<sub>C</sub> Pins. During loopback, Collision and Receive data inputs are ignored. The transmit pair is idled. At the end of transmission, the signal quality error test (SQET) will be simulated by asserting collision during the inhibit window. During loopback, the watchdog timer is enabled.

**Watchdog Timer Disable:** When this pin is between 10 V (Min.) and 16 V (Max.), the on chip 25 ms Watchdog Timer will be disabled. The watchdog timer is used to monitor the transmit enable pin. If TxEN is asserted for longer than 25 ms, then the watchdog timer (if enabled) will automatically deassert CSN and inhibit any further transmissions on the Tx<sub>+</sub> and Tx<sub>-</sub> lines. The watchdog timer is automatically reset each time TxEN is deasserted.

**Interconnection to a Data Link Controller**

Figure 5 shows the interconnections between the 8023A MCC™ and SEEQ's 8003 or 8005. There are three connections for each of the two transmission channels, transmit and receive, plus the Collision Signal line (COLL).

Transmitter connections are:

- Transmit Data, Tx<sub>D</sub>
- Transmit Clock, Tx<sub>C</sub>
- Transmit Enable, TxEN
- Collision, COLL

Receiver connections are:

- Receive Data, Rx<sub>D</sub>
- Receive Clock, Rx<sub>C</sub>
- Carrier Sense, CSN

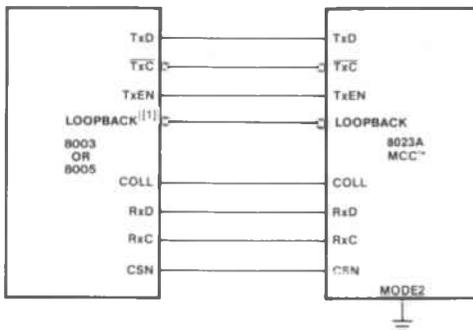


Figure 5. Interconnection of 8023A and 8003/8005

NOTE:  
1. Loopback output on 8005 only.

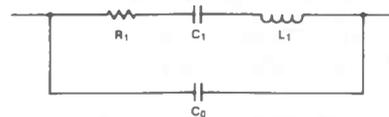
**Compatibility with Other LAN Controllers**

SEEQ's 8023A is compatible with other LAN Controllers, such as the 82586, when Pin 2 (MODE2) of the 8023A is floating or tied to V<sub>CC</sub>. In this mode of operation, timing and polarity on the controller interface lines are compatible, with the 82586 specification dated March '984.

Use of Time Domain Reflectometry in the 82586 is not recommended since the TDR transmission does not have a valid preamble.

**D.C. and A.C. Characteristics and Timing Crystal Specification**

Resonant Frequency (C <sub>L</sub> = 20 pF)	..... 20 MHz
	± 0.005% 0-70° C
	and ± 0.003% at 25° C
Type	..... Fundamental Mode
Circuit	..... Parallel Resonance
Load Capacitance (C <sub>L</sub> )	..... 20 pF
Shunt Capacitance (C <sub>0</sub> )	..... 7 pF Max.
Equivalent Series Resistance (R <sub>1</sub> )	..... 25 Ω Max.
Motional Capacitance (C <sub>1</sub> )	..... 0.02 pF Max.
Drive Level	..... 2 mW



EQUIVALENT CIRCUIT OF CRYSTAL

Figure 6.

## Absolute Maximum Ratings\*

Storage Temperature ..... -65° C to 150° C  
 All Input and Output Voltage ..... -0.3 to  $V_{CC} + 0.3$   
 $V_{CC}$  ..... -0.3 to 7V  
 ( $Rx\pm$ ,  $Tx\pm$ ,  $COLL\pm$ ) High Voltage  
 Short Circuit Immunity ..... -0.3 to 16V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics $T_A=0^\circ\text{C}$ to $70^\circ\text{C}$ ; $V_{CC}=5\text{ V} \pm 10\%$

Symbol	Parameter	Min.	Max.	Unit	Conditions
$I_{IL}$	Input Leakage Current (except MODE1, MODE2 Receive and Collision Pairs)		10	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{CC}$
	MODE1 Input Leakage Current		200	$\mu\text{A}$	$0 \leq V_{IN} \leq V_{CC}$
	Receive and Collision Pairs ( $Rx\pm$ , $COLL\pm$ ) Input Leakage Current		2	mA	$V_{IN} = 0$
$I_{CC}$	$V_{CC}$ Current		75	mA	All Inputs, Outputs Open
$V_{IL}$	TTL Input Low Voltage	-0.3	0.8	V	
$V_{IH}$	TTL Input High Voltage (except X1)	2.0	$V_{CC} + 0.3$	V	
	X1 Input High Voltage	3.5	$V_{CC} + 0.3$	$\pm 1.2$	V
$V_{OL}$	TTL Output Low Voltage except $\overline{TxC}$		0.4	V	$I_{OL} = 2.1\text{ mA}$
	$\overline{TxC}$ Output Low Voltage		0.4	V	$I_{OL} = 4.2\text{ mA}$
$V_{OH}$	TTL Output High Voltage (except $RxC$ , $\overline{TxC}$ , $RxD$ )	2.4		V	$I_{OH} = -400\mu\text{A}$
	$RxC$ , $\overline{TxC}$ , $RxD$ Output High Voltage	3.9		V	$I_{OH} = -400\mu\text{A}$
$V_{ODF}$	Differential Output Swing	$\pm 0.55$	$\pm 1.2$	V	78 $\Omega$ Termination Resistor and 243 $\Omega$ Load Resistors
$V_{OCM}$	Common Mode Output Voltage	$V_{CC} - 2.5$	$V_{CC} - 1$	V	78 $\Omega$ Termination Resistor and 243 $\Omega$ Load Resistors
$V_{BKSv}$	$Tx\pm$ Backswing Voltage During Idle		0.1	V	Shunt inductive load $\leq 27\ \mu\text{H}$
$V_{IDF}$	Input Differential Voltage (measured differentially)	$\pm 0.3$	$\pm 1.2$	V	
$V_{ICM}$	Input Common Mode Voltage	0	$V_{CC}$	V	
$C_{IN}^{(1)}$	Input Capacitance		15	pF	
$C_{OUT}^{(1)}$	Output Capacitance		15	pF	

### NOTE:

1. Characterized. Not tested.

**A.C. Test Conditions**

Output Loading TTL Output:	1 TTL gate and 20 pF capacitor
Differential Output:	243Ω resistor and 10 pF capacitor from each pin to $V_{SS}$ and a termination 78Ω resistor load resistor in parallel with a 27 μH inductor between the two differential output pins
Differential Signal Delay Time Reference Level:	50% point of swing
Differential Output Rise and Fall Time:	20% to 80% points
$RxC$ , $\overline{TxC}$ , X1 High and Low Time:	High time measured at 3.0V Low time measured at 0.6V
$RxD$ , $RxC$ , $\overline{TxC}$ , X1 Rise and Fall Time:	Measured between 0.6V and 3.0V points
TTL Input Voltage (except X1):	0.8V to 2.0V with 10 ns rise and fall time
X1 Input Voltage:	0.8V to 3.5V with 5 ns rise and fall time
Differential Input Voltage:	At least ± 300 mV with rise and fall time of 10 ns measured between -0.2V and +0.2V

**20 MHz TTL Clock Input Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_1$	X1 Cycle Time	49.995	50.005	ns
$t_2$	X1 High Time	15		ns
$t_3$	X1 Low Time	15		ns
$t_4$	X1 Rise Time		5	ns
$t_5$	X1 Fall Time		5	ns
$t_{5A}$	X1 to $\overline{TxC}$ Delay Time	10	45	ns

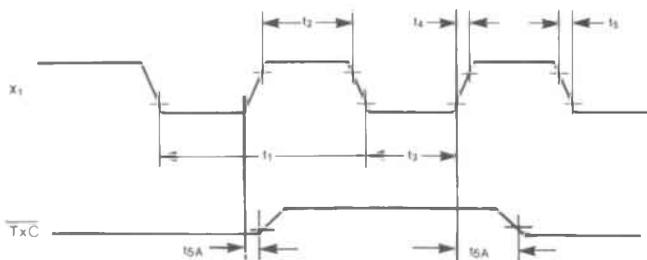


Figure 12.20 MHz TTL Clock Timing

**Transmit Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_6^{[1]}$	$\overline{\text{TxC}}$ Cycle Time	99.99	100.01	ns
$t_7$	$\overline{\text{TxC}}$ High Time	40		ns
$t_8$	$\overline{\text{TxC}}$ Low Time	40		ns
$t_9^{[1]}$	$\overline{\text{TxC}}$ Rise Time		5	ns
$t_{10}^{[1]}$	$\overline{\text{TxC}}$ Fall Time		5	ns
$t_{11}$	TxEN Setup Time if Mode2=0 TxEN Setup Time if Mode2=1	40 55		ns ns
$t_{12}$	TxD Setup Time if Mode2=0 TxD Setup Time if Mode2=1	40 55		ns ns
$t_{13}^{[1]}$	Bit Center to Bit Center Time	99.5	100.5	ns
$t_{14}^{[1]}$	Bit Center to Bit Boundary Time	49.5	50.5	ns
$t_{15}^{[1]}$	Tx+ and Tx- Rise Time		5	ns
$t_{16}^{[1]}$	Tx+ and Tx- Fall Time		5	ns
$t_{17}$	Transmit Active Time From The Last Positive Transition	200		ns
$t_{17A}^{[1]}$	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 100 mV of 0 V	400	600	ns
$t_{17B}^{[1]}$	From Last Positive Transition of the Transmit Pair to Differential Output Approaches within 40 mV of 0 V		7000	ns
$t_{18}$	Tx+ and Tx- Output Delay Time		70	ns
$t_{19}$	TxD Hold Time if Mode2=0 TxD Hold Time if Mode2=1	15 0		ns ns
$t_{20}$	TxEN Hold Time if Mode2=0 TxEN Hold Time if Mode2=1	15 0		ns ns

**NOTE:**

1. Characterized. Not tested.

MODE1 = 1  
MODE2 = 0

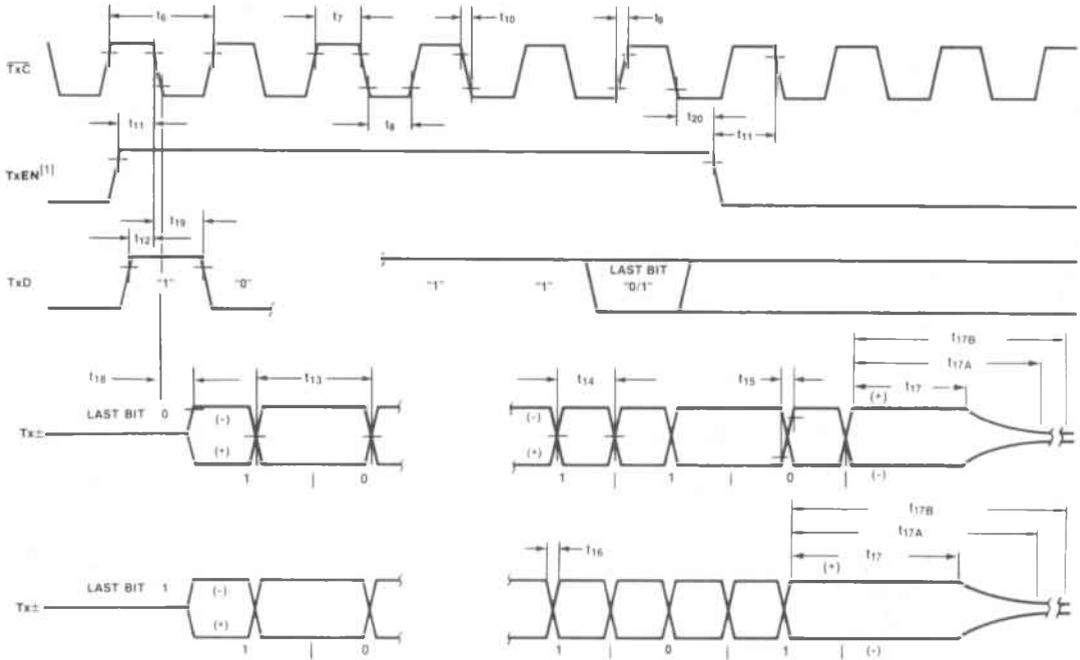


Figure 7. Transmit Timing

MODE1 = 0  
MODE2 = 0

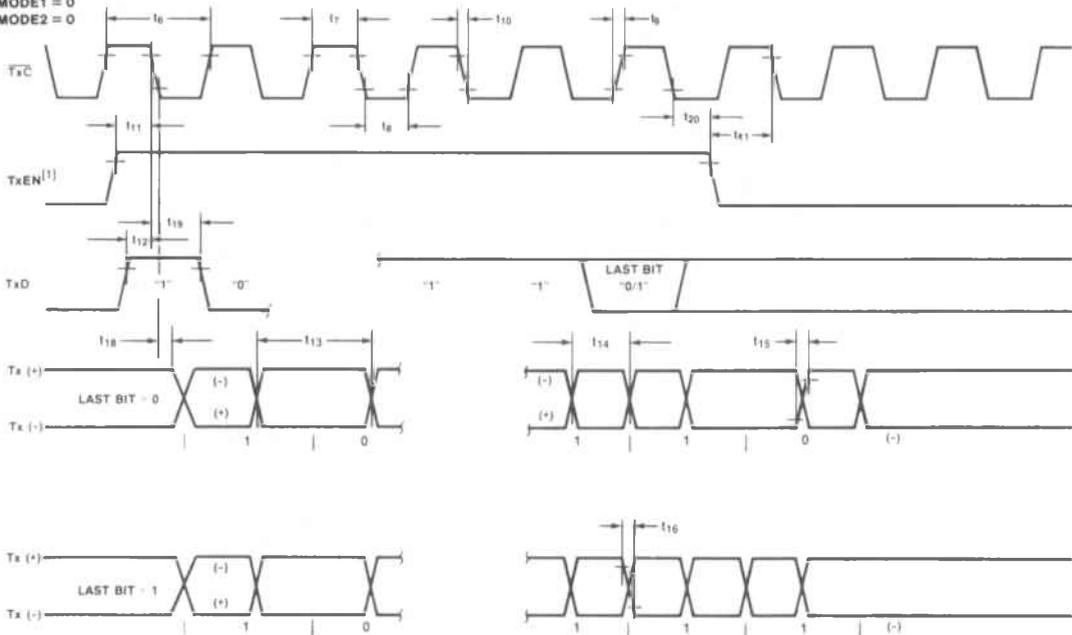
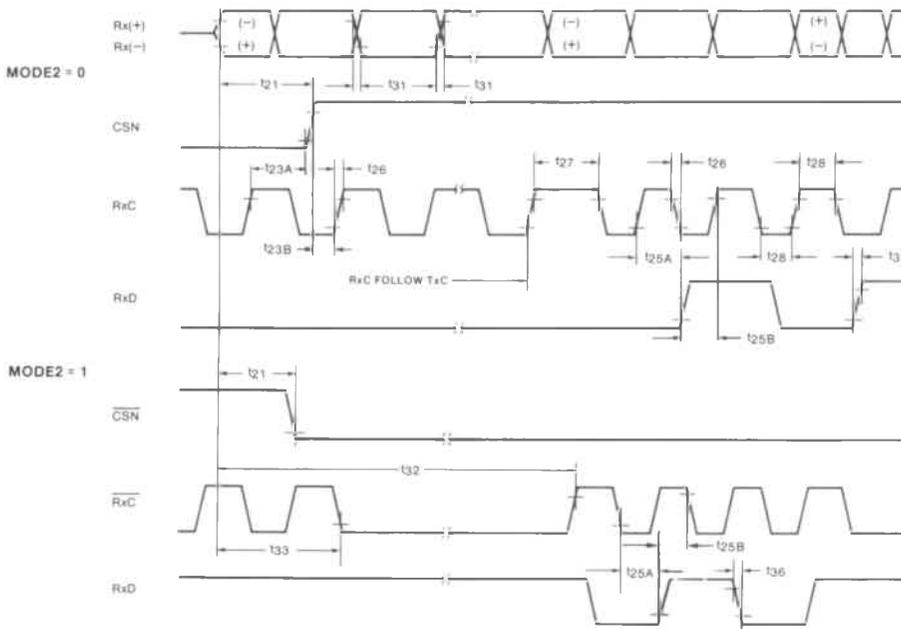


Figure 8. Transmit Timing

NOTE:

1. If MODE2= 1, TxEN becomes active low signal TxEN.

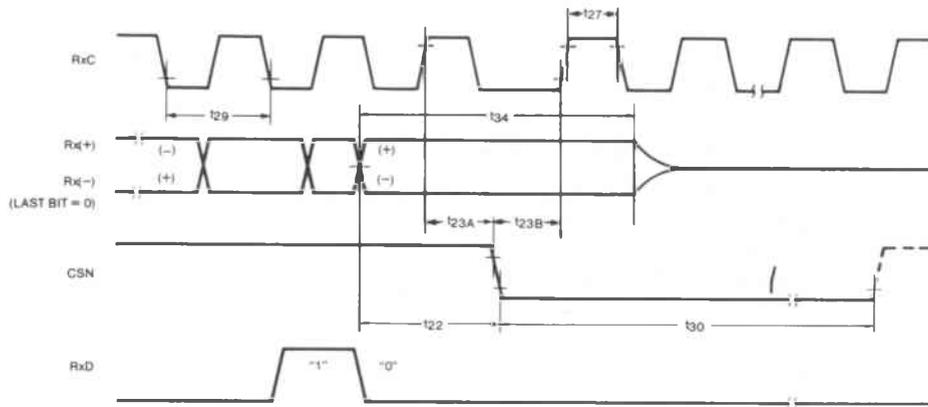
Symbol	Parameter	Min.	Max.	Units
$t_{21}$	CSN Assert Delay Time		240	ns
$t_{22}$	CSN Deasserts Delay Time (measured from Last Bit Boundary)		240	ns
$t_{23A}$	CSN Hold Time	30		ns
$t_{23B}$	CSN Set up Time	30		ns
$t_{24}$	CSN Deassertion Delay Time	10	35	ns
$t_{25A}$	RxD Hold Time	30		ns
$t_{25B}$	RxD Set up Time	30		ns
$t_{26}^{[1]}$	RxC, $\overline{\text{RxC}}$ Rise and Fall Time		5	ns
$t_{27}^{[1]}$	During Clock Switch RxC Keeps High, $\overline{\text{RxC}}$ Keeps Low Time	40	200	ns
$t_{28}$	RxC, $\overline{\text{RxC}}$ High and Low Time	40		ns
$t_{29}^{[1]}$	RxC, $\overline{\text{RxC}}$ Clock Cycle Time (during data period)	95	105	ns
$t_{30}$	CSN Inhibit Time (on Transmission Node only)	4.3	4.6	$\mu\text{s}$
$t_{31}$	Rx+/Rx- Rise and Fall Time		10	ns
$t_{32}^{[1]}$	$\overline{\text{RxC}}$ Held Low Duration from First Valid Negative-Going Transition	1.15	1.35	$\mu\text{s}$
$t_{33}$	$\overline{\text{RxC}}$ Stops Delay Time from First Valid Negative-Going Transition		240	ns
$t_{34}^{[1]}$	Rx+/Rx- Begin Return to Zero from Last Positive-Going Transition	160		ns
$t_{35}^{[1]}$	RxD Rise Time		10	ns
$t_{36}^{[1]}$	RxD Fall Time		10	ns



NOTE:  
1. Characterized. Not tested.

Figure 9. Receive Timing—Start of Packet

MODE2 = 0



MODE2 = 1

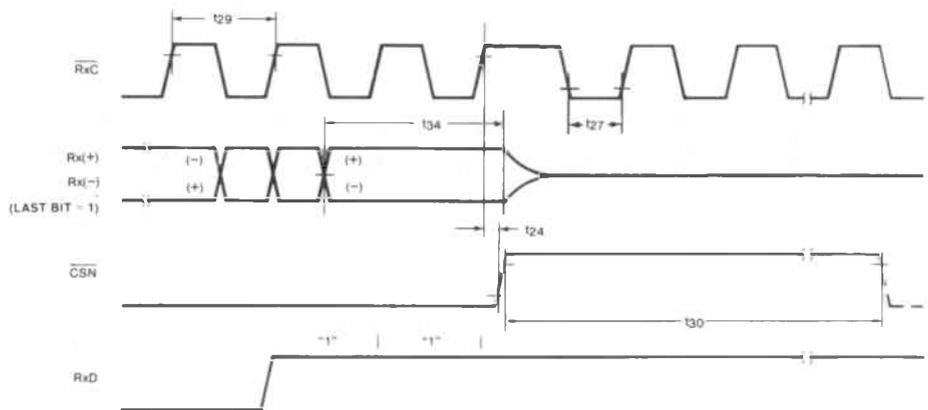


Figure 10. Receive Timing — End of Packet

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**Collision Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$ 

Symbol	Parameter	Min.	Max.	Units
$t_{s1}$	COLL+/COLL- Cycle Time	86	118	ns
$t_{s2}$	COLL+/COLL- Rise and Fall Time		10	ns
$t_{s3}$	COLL+/COLL- High and Low Time	35	70	ns
$t_{s4}$	COLL+/COLL- Width (measured at $-0.3\text{V}$ )	26		ns
$t_{s5}$	COLL Asserts Delay Time		300	ns
$t_{s6}$	COLL Deasserts Delay Time		500	ns
$t_{s7}$	CSN Asserts Delay Time		400	ns
$t_{s8}$	CSN Deasserts Delay Time		600	ns

**Notes:**

1. COLL+ and COLL- asserts and deasserts COLL, asynchronously, and asserts and deasserts CSN synchronously with Rx<sub>C</sub>.
2. If COLL+ and COLL- arrives within  $4.5\mu\text{s}$  from the time CSN was deasserted; CSN will not be reasserted (on transmission node only).
3. When COLL+ and COLL- terminates, CSN will not be deasserted if Rx+ and Rx- are still active.
4. When the node finishes transmitting and CSN is deasserted, it cannot be asserted again for  $4.5\mu\text{s}$ .
5. If MODE2 = 1, then COLL and CSN are inverted.

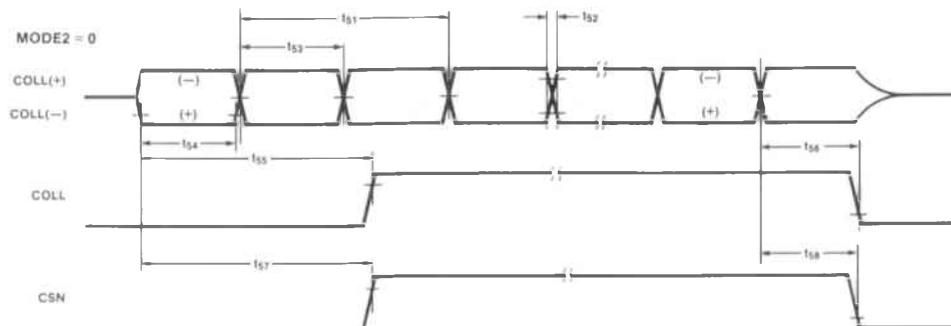


Figure 11. Collision Timing

**Loopback Timing**  $T_A=0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ ;  $V_{CC}=5\text{ V} \pm 10\%$

Symbol	Parameter	Min.	Max.	Units
$t_{s1}$	LPBK Setup Time	500		ns
$t_{h2}$	LPBK Hold Time	5		$\mu\text{S}$
$t_{s3}$	In Collision Simulation, COLL Signal Delay Time	475	625	ns
$t_{s4}$	COLL Duration Time	600	750	ns

**Note:**

1. PLL needs 12-bit cell times to acquire lock, RxD is invalid during this period. RxC is low for  $1.35\ \mu\text{s}$  (max) if  $\text{MODE2}=1$ . RxD=0 if  $\text{MODE2}=0$ . RxD=1 if  $\text{MODE2}=1$ .

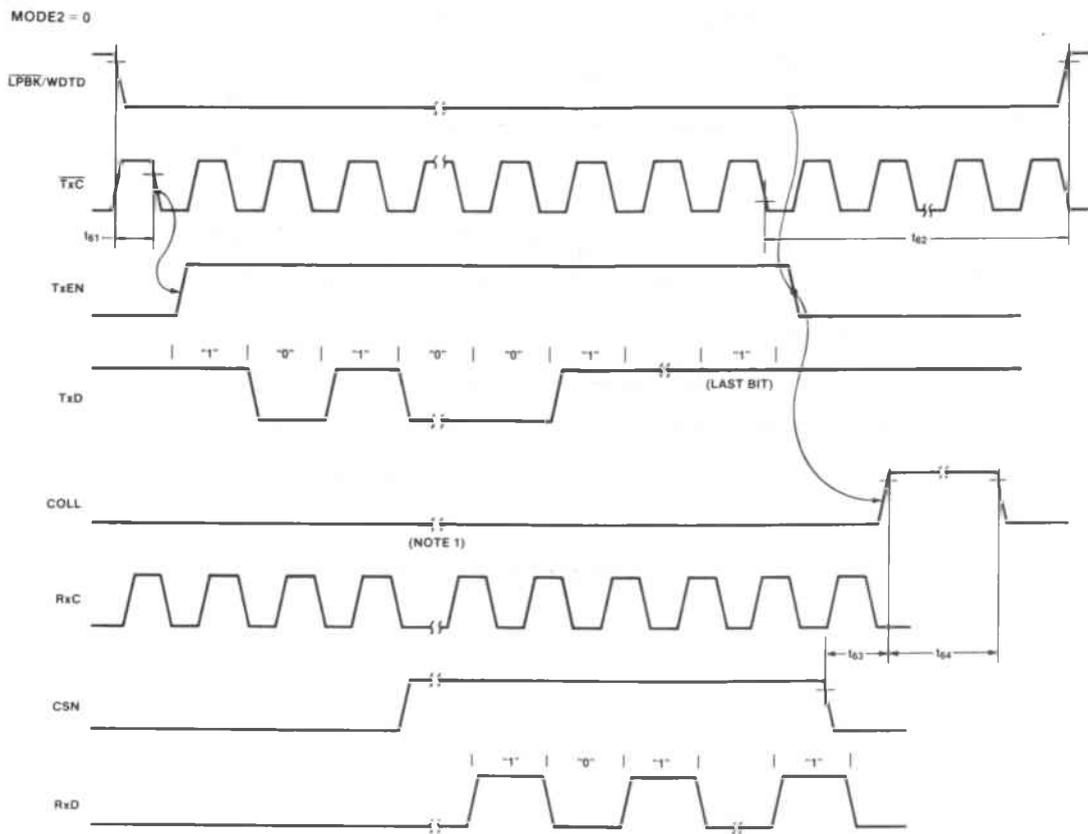


Figure 13. Loopback Timing

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MODE2 = 1

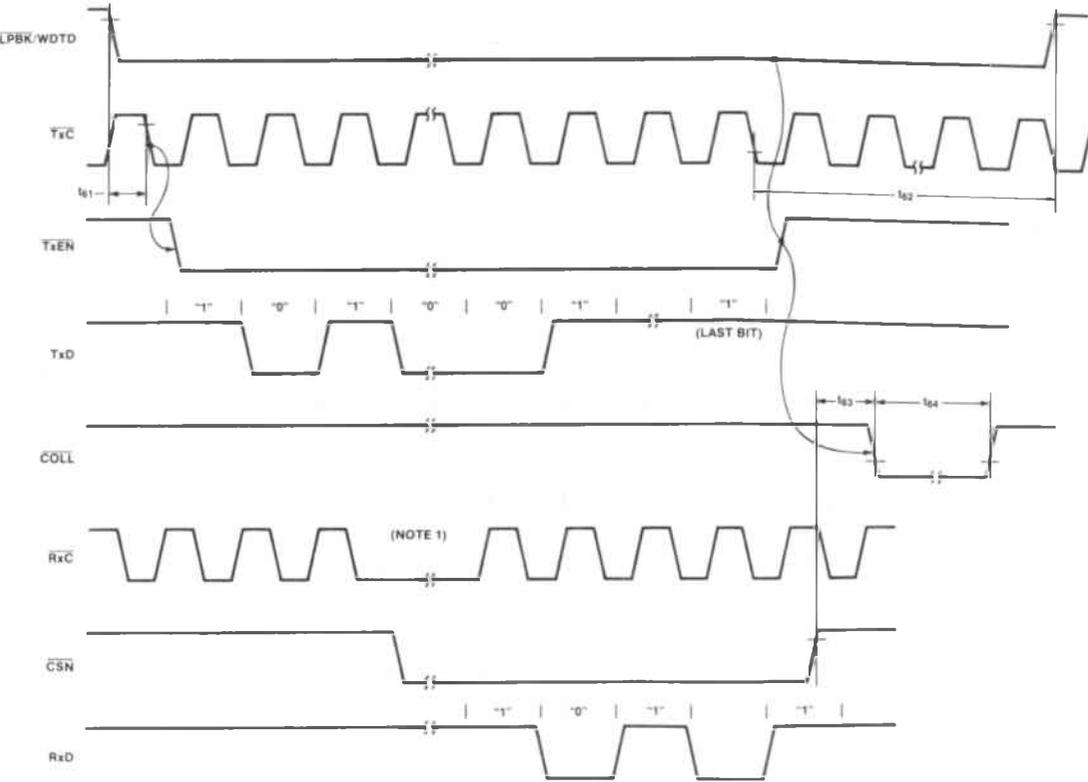
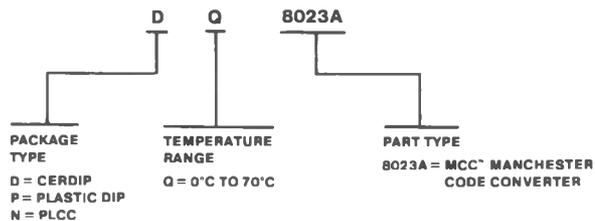


Figure 14. Loopback Timing — (Cont.)

Ordering Information



MICRO/  
DATA COM



## Advanced Ethernet Data Link Controller

October 1987

### Preliminary

#### Features

- **Conforms to IEEE 802.3 Standard for Media Access Control**
- **Recognizes One to Six Selectable Station Addresses**
- **Software Selection of 2 Byte or 6 Byte Station Addresses**
- **User Selectable Preamble and Frame Check Sequence Generation**
- **Directly Supports 64K Bytes of Local Packet Buffer**
  - Connects to RAS/CAS/Data/Control of 64K x 4 Dynamic RAMS
  - Automatic RAM Refresh
- **Manages Local Receive/Transmit Packet Buffer by Buffer Chaining Technique**
  - Automatic Posting of Status in Buffer Header
- **Flexible System Bus Interface**
  - 8 or 16 Bit Data Transfers with Byte Swap Capability
  - Programmable DMA Burst Length
  - Selectable for Intel or Motorola Compatible Bus Signals
- **Connects Directly to 8020 Manchester Code Converter**
- **68 Pin Surface Mount Plastic Leaded Chip Carrier Package**

#### Pin Description

(An asterisk after a signal name signifies a low active signal)

**D0-D15:** A 16 bit bidirectional system data bus. If *BUS-SIZE=0*, the bus is configured as 8 bits and D8-D15 are not used for data transfer. D8-D15 are used to provide address information to the address PROM in both 8 and 16 bit modes. Byte order for local buffer data transfers on a 16 bit bus is software configured.

**EN\*:** An output which can be used to control the tri-state control pin of external bi-directional drivers such as the 74LS245.

**APEN\*:** Low active address PROM enable output.

**IOW\*/R.W\*:** If *busmode=1*, this input defines the current bus cycle as a write. If *busmode=0*, this input defines the bus cycle as a read if a 1 or a write if a 0.

**IOR\*:** If *busmode=1*, this input defines the current bus cycle as a read. If *busmode=0*, this input is not used.

**CS\*:** The chip select input, used to access internal registers and the packet buffer.

**A0-A3:** Address select inputs used to select internal registers for reading or writing.

**DACK\*:** An input used to acknowledge granting of the system bus for external DMA transfers. When *DREQ* is active, *DACK\** functions as a chip select for reads and writes.

**DREQ/DREQ\*:** An output to an external DMA controller used to signal that a DMA request is being made. This signal is high active when *busmode=1*, low active when *busmode=0*.

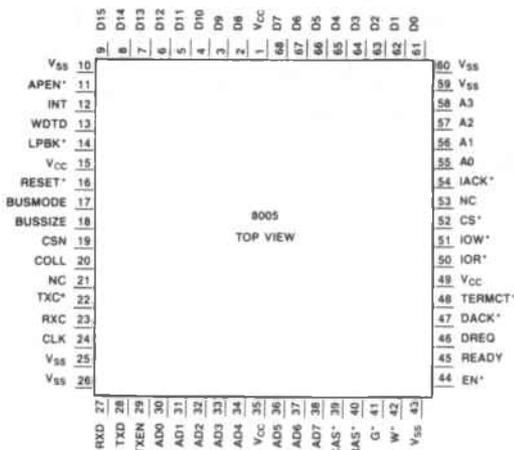
**TERMCT/TERMCT\*:** An input which signals that the last byte or word of a DMA access is on the bus. When *busmode=1*, this input is high active; when *busmode=0*, it is low active.

**READY/DTACK\*:** A tri-state output. When *busmode=1*, this output functions as a *READY* pin (Intel compatible); when *busmode=0*, this output is *DTACK\** (Motorola compatible).

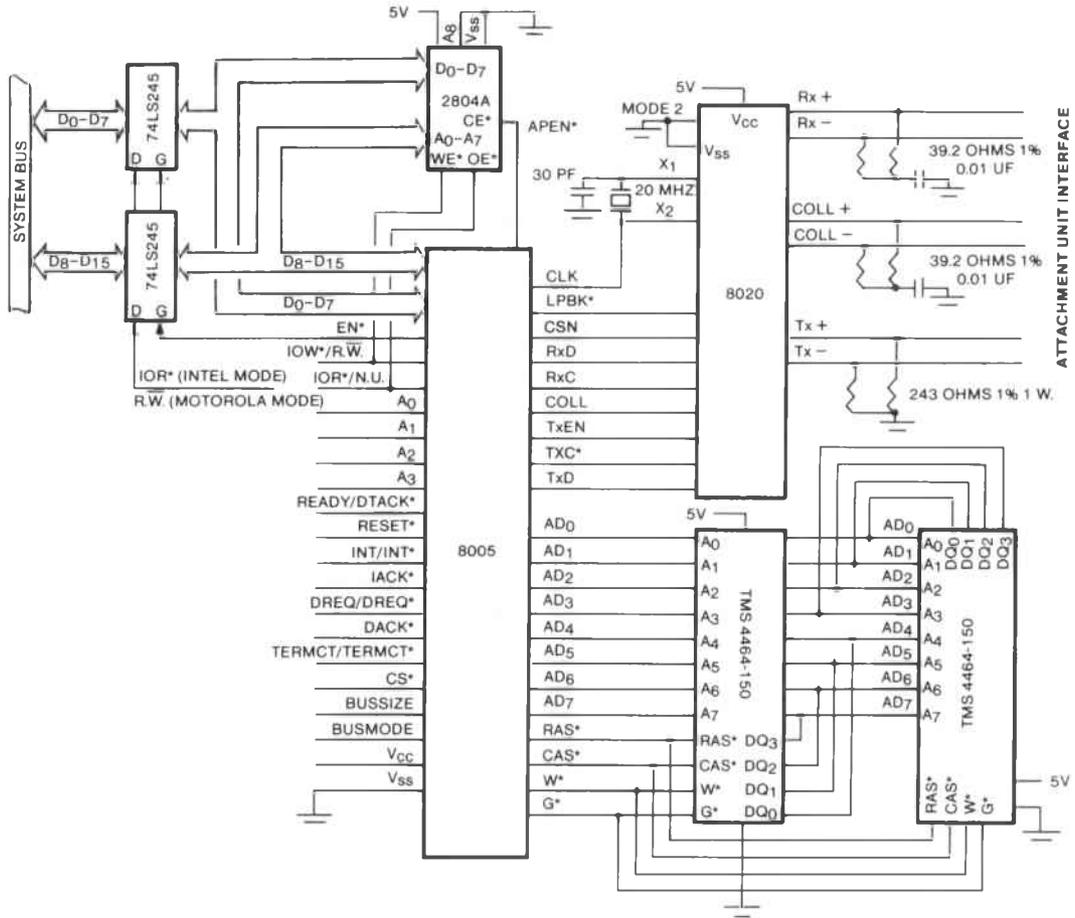
**INT/INT\*:** When *busmode=1*, this is a high active interrupt output; when *busmode=0*, this output is low active.

**IACK\*:** Active low interrupt acknowledge input. When this input is active and *INT* is active the contents of the interrupt vector register are placed on D0-D7.

**RESET\*:** The low active reset input. Asserting *RESET\** clears all configuration and pointer registers to 00. Following *reset*, a wait of 4  $\mu$ s is necessary before accessing the part.



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INTERCONNECT DIAGRAM

**BUSMODE:** An input which selects Intel-compatible bus signals when high or Motorola-compatible bus signals when low.

**BUSSIZE:** An input which selects 8 bit system bus when low or 16 bit system bus when high.

**AD0-AD7:** A multiplexed address and data bus used to provide row and column addresses and read/write data to the packet buffer dynamic RAM.

**RAS\*:** Row address strobe to the packet buffer memory.

**CAS\*:** Column address strobe to the packet buffer memory. Page mode addressing is used when possible to speed access to the buffer.

**W\*:** An output to the dynamic RAM buffer that indicates the current cycle is a write.

**G\*:** An output to the dynamic RAM buffer that enables read data onto the AD bus.

**TXEN:** An output to the Manchester Code Converter that indicates a transmission is in progress.

**TXC\*:** An input from the Manchester Code Converter that is used to synchronize transmitted data.

**TXD:** The transmit data output to the Manchester Code Converter.

**RXC:** An input from the Manchester Code Converter used to synchronize received data.

**RXD:** The receive data input from the Manchester Code Converter.

**COLL:** The collision input from the Manchester Code Converter.

**CSN:** The carrier sense input from the Manchester Code Converter.

**WDTD:** The watchdog timer disable output.

**LPBK\*:** The loopback control output.

**CLK:** The master 20 MHz input clock.

### Block Description

Three major blocks comprise the 8005: the EDLC (Ethernet Data Link Controller), PBC (Packet Buffer Controller) and BIU (Bus Interface Unit).

The EDLC supports the link layer (layer 2) of the IEEE 802.3 standard. It performs serialization/deserialization, preamble generation/stripping, frame check sequence generation/stripping, transmission deferral, collision handling and address recognition of up to 6 station addresses as well as multicast/broadcast addresses. It also supplies loopback and watchdog timer disable outputs which can be controlled by software to provide local diagnostic support. For non-IEEE 802.3 applications such as serial backplane buses, support is also provided for 2 byte address recognition, reduced slot time and reduced preamble length.

The PBC provides management for a 64K byte local packet buffer consisting of two 64K x 4 dynamic RAMS. This block provides arbitration and control for four different memory ports: the EDLC transmitter, for network transmit packets; the EDLC receiver, for received frames; the BIU, for system data and control; and an internal DRAM refresh generator. To minimize pin count, dynamic RAM addresses and data are time multiplexed on a single 8 bit bus. A control line and an 8 bit address is also provided to permit reading or writing to a locally attached EEPROM or PROM. This permits configuring a PC board with its station address(es) and configuration data independent of the network layer software used.

The BIU interfaces to the system bus and provides access to internal configuration/status registers, the local packet buffer and a control signal interface to permit DMA or programmed I/O transfer of packet data. The data path between the system bus and the local DRAM buffer is buffered by a 16 byte FIFO called the DMA FIFO. This permits high speed data transfers to occur even when the PBC is busy servicing the EDLC transmitter or receiver or refreshing the DRAM. Both 8 and 16 bit transfers are supported, and byte ordering on a 16 bit bus is under software control. The 8005 supports both Intel-compatible and Motorola-compatible buses.

### Buffer Management

The PBC manages a 64K byte packet buffer into which packets that are received are temporarily stored until the system either reads or disposes of them and packets placed there by the system are held for transmission over the link. The buffer is logically divided into separate receive and transmit areas of selectable size. The transmit area always originates at location 0. Each packet in the buffer is prefixed by a header of 4 bytes that contains command and status information and a 16 bit pointer to the start of the next packet in the buffer.

To transmit frames, the system loads one or more packets of data, complete with header information, into the transmit area of the buffer and commands the 8005 to begin transmission starting from the address contained in the transmit pointer register. When transmission is complete, the 8005 updates the status byte in the header and interrupts the system if so programmed. The transmit pointer automatically wraps to location 0 when the transmit end area is reached.

The PBC manages the buffer area as a circular buffer with automatic wraparound. As data is received from the EDLC it is stored in the buffer beginning at the location specified by the receive pointer register. While receiving, the PBC compares the most significant byte of the receive pointer register to the value in the receive end area register. If the receive pointer register is incremented to this value, one of two actions will be taken: if receive overflow is not enabled, the PBC will discard any packets

that do not fit and wait for a packet that will fit (a packet will fit if all the data plus 4 bytes for the next packet header fit in the space available); if receive overflow is enabled it will receive as much of the packet as possible in the available space, turn off the receiver, set the Receive Interrupt bit and assert interrupt (if interrupts are enabled). The header for an incomplete packet will be 4 bytes of 00. The length of the packet can be determined by reading the receive pointer, which will be frozen at the first byte of the next header. Restarting the receiver is accomplished by freeing up buffer space and turning the receiver back on.

### Transmit Packet Format

Each packet to be transmitted consists of a four byte header and up to 65,532 bytes of data which are placed into the local buffer via the BIU. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.
2. Least significant byte of the address of the next packet header.
3. A transmit command byte.
4. A transmit status byte which should be initialized to zero by the system and will contain status for this packet when transmission is complete.

Bytes 1 and 2, called the next packet pointer, point to the location immediately following the last byte of the packet, which is the first byte of the next packet header, if it exists. When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.

Byte 3 is the transmit command byte. It contains information to guide the controller in processing the packet associated with this block.

**Bit 0: Xmit Babble Int. Enable.** The 8005 will transmit frames as large as the transmit buffer can hold but will flag long frames in the transmit status byte and interrupt if this bit is set to a one. This condition is caused by an attempt to transmit a packet larger than the allowed 1514 bytes.

**Bit 1: Xmit Collision Interrupt Enable.** When set to a one, a transmit interrupt will be generated if a collision occurs during a transmit attempt.

**Bit 2: 16 Collisions Enable.** When set to a one, a transmit interrupt will be generated if 16 collisions occur during a transmit attempt.

**Bit 3: Xmit Success Interrupt Enable.** When set to a one, a transmit interrupt will be generated if the transmission is successful, that is, fewer than 16 collisions occurred.

**Bit 4:** Not used.

**Bit 5: Header Only.** If this bit is cleared to a zero, the transmitter will process this header as a pointer only, with no data associated with it.

**Bit 6: Chain Continue/End.** If set to a one, there are more headers in the chain to be processed. If this bit is a zero, this header is the last one in the chain.

**Bit 7: Xmit/Receive.** If this bit is a one, the current header is for a packet to be transmitted. If this bit is a zero, the frame header will be processed as a header only, like the header only bit (bit 5).

Byte 4 is the transmit status byte, which is written by the PBC upon conclusion of each frame transmission or retransmission attempt. It provides for reporting of both normal and error termination conditions of each transmission.

**Bit 0: Xmit Babble.** If set to a one, transmit babble occurred during the transmission attempt. This is caused by an attempt to transmit a packet larger than the allowed 1514 bytes.

**Bit 1: Xmit Collision.** If set to a one, a collision occurred during the transmission attempt.

**Bit 2: 16 Collisions.** If set to a one, 16 collisions occurred during the transmission attempt.

**Bit 3, 4, 5 and 6:** Reserved.

**Bit 7: Done.** If set to a one, the controller has completed all processing of the packet associated with this header (either the packet has been sent successfully or 16 collisions occurred) and there is now valid status in the status byte. The user may now reuse the buffer area.

### Receive Packet Format

Each packet received is preceded by a four byte header and contains up to 65,528 (64K — 2 headers) bytes of data which are placed into the local buffer via the PBC. The header contains the following information in the indicated order:

1. Most significant byte of the address of the next packet header.
2. Least significant byte of the address of the next packet header.
3. Header status byte.
4. Frame status byte.

Bytes 1 and 2, called the next packet pointer, point to the first byte of the next receive packet header. The next packet header starts immediately after the end of the current packet. The packet length is equal to the difference between the starting addresses of the two packet headers minus 4. If the value of the next packet pointer is less than the current one, the pointer has wrapped around from the end of the buffer to the Receive Start Area (the Receive Start Area equals the Transmit End Area address + 1) and then to the

value of the next pointer. When in 16 bit mode, the user should note the order of these bytes to be sure it is compatible with the MSB-LSB storage convention of the processor/bus being used.

The third byte of the header contains header information associated with this packet.

**Bits 0 through 4:** Not used.

**Bit 5: Header Only.** If this bit is cleared to a zero, there is no packet associated with this header. This enables the controller to specify the end of a chain without touching the status of a packet already received. All 4 bytes in a header-only packet will be 00.

**Bit 6: Chain Continue/End.** If this bit is set to a one, there are more headers in this chain to be processed. If this bit is a zero, this header is the last one in the chain and this header space will be used for the next packet that is received.

**Bit 7: Xmit/Receive.** This bit is always set to 0 by the controller to indicate a receive packet header.

The fourth byte of the header, called the packet status byte, contains status information resulting from processing the packet associated with this block.

**Bit 0: Oversize Packet.** If this bit is a one, the packet was larger than 1514 bytes.

**Bit 1: CRC Error.** If this bit is a one, a CRC error (frame check sequence error) occurred in this frame. CRC status is captured on byte boundaries, so that 7 or less dribble bits will not cause a CRC error.

**Bit 2: Dribble Error.** Frames are integral multiples of octets (bytes). If this bit is a one, the received frame did not end on an octet (byte) boundary. This is normally not a fatal error unless the CRC error bit is also set.

**Bit 3: Short Frame.** If this bit is a one, the frame contained less than 64 bytes including CRC. Short frames are properly received as long as they are at least 6 bytes long; frames with less than 6 bytes will only be received if the match mode bits in configuration register #1 specify promiscuous mode, multicast/broadcast is selected and the first bit of the destination address is a 1, or the 2-byte address mode has been selected.

**Bit 4 and 5:** Not used.

**Bit 6: Overflow.** If this bit is a one, an overflow occurred during the frame reception. This condition is caused by insufficient space remaining in the local buffer.

**Bit 7: Done.** If this bit is a one, the controller has completed all processing of this frame and there are now valid pointers and status in this header. The user may now move this packet out of the local buffer, if desired, and reuse this buffer space.

## Registers

There are nine directly accessible 16 bit registers in the 8005, one of which is used as a "window" into indirectly accessed registers as well as the local buffer memory. Access is controlled by chip select, I/O read, I/O write and four address inputs, A0-A3. The following description assumes a 16 bit wide system interface; as such, the low order address input, A0, is shown as "X," a don't care. In 8 bit mode, input pin A0 selects bits 0 through 7 of the register when a zero, and bits 8 through 15 when a one. Note that the byte swap bit does not affect the byte order of these registers.

### Command Register, A3-0=000X<sub>2</sub> (Write only)

**Bit 0: DMA Interrupt Enable.** When set to a 1, completion of a DMA operation, as signaled by Terminal Count, will generate an interrupt.

**Bit 1: Rx Interrupt Enable.** When set to a 1, this bit enables interrupts whenever a packet becomes available in the packet buffer.

**Bit 2: Tx Interrupt Enable.** When set to a 1, this bit enables interrupts for completion of transmit operations. See the transmit header command byte description for conditions that can cause an interrupt.

**Bit 3: Buffer Window Interrupt Enable.** Setting this bit to a one enables interrupts for buffer window register reads from the packet buffer.

**Bit 4: DMA Interrupt Acknowledge.** Setting this bit to a one causes a pending DMA interrupt to be cleared.

**Bit 5: Rx Interrupt Acknowledge.** Settling this bit to a one causes a pending receive interrupt to be cleared.

**Bit 6: Tx Interrupt Acknowledge.** Setting this bit to a one causes a pending transmit interrupt to be cleared.

**Bit 7: Buffer Window Interrupt Acknowledge.** Setting this bit to a one causes a pending buffer window interrupt to be cleared.

**Bit 8: Set DMA On.** Setting this bit to a one enables the DMA request logic. If the DMA FIFO is set to the read direction, a DMA request will be asserted when the DMA FIFO has enough bytes to satisfy the burst size. If the DMA FIFO is in the write direction the DMA request will be asserted immediately. Clearing this bit has no effect. Setting this bit with bit 11 set will force a DMA interrupt, provided the DMA interrupt enable bit is set, which permits testing the interrupt without actually performing DMA operations.

**Bit 9: Set Rx On.** Setting this bit to a one enables the EDLC receiver. Clearing this bit to a 0 has no effect. Setting this bit with bit 12 set will force an interrupt, provided the receive interrupt enable bit is set, which permits testing the interrupt without receiving packet data.

**Bit 10: Set Tx On.** Setting this bit to a 1 enables the EDLC transmitter. The PBC will read the header information pointed to by the transmit pointer and process the frame accordingly (see transmit packet header description). The conditions for interrupting upon completing packet processing are specified in the transmit header command byte, which is stored in the buffer memory. Setting this bit with bit 13 set will force a transmit interrupt for test purposes.

**Bit 11: Set DMA Off.** Setting this bit to a one disables the DMA request logic.

**Bit 12: Set Rx Off.** Setting this bit to a one disables the EDLC receive logic. If the EDLC is actively receiving a packet when bit 12 is set, the EDLC receiver will be disabled after completing reception of the packet.

**Bit 13: Set Tx Off.** Setting this bit to a one disables the EDLC transmitter. If a packet is being transmitted when this bit is set, the packet will be aborted.

**Bit 14: FIFO Read.** When set to a one, the DMA FIFO direction is set to read from the packet buffer. The FIFO direction should not be changed from a write to a read until it is empty (see FIFO status bits).

**Bit 15: FIFO Write.** When set to a one, the DMA FIFO direction is set to write to the packet buffer. Changing the DMA FIFO direction clears the DMA FIFO.

**Status Register, A3-0 = 000X<sub>2</sub> (Read only)**

**Bit 0: DMA Interrupt Enable.** When set, this bit indicates that interrupts are enabled for terminal count during a DMA operation.

**Bit 1: Rx Interrupt Enable.** When set, this bit indicates that interrupts are enabled for receive events.

**Bit 2: Tx Interrupt Enable.** When set, this bit indicates that interrupts are enabled for transmit events.

**Bit 3: Buffer Window Interrupt Enable.** When set, this bit indicates that interrupts are enabled for buffer window reads from the packet buffer.

**Bit 4: DMA Interrupt.** When set, this bit indicates that a DMA operation has been completed. If the associated interrupt enable bit is set, an interrupt will also be asserted.

**Bit 5: Rx Interrupt.** When set, this bit indicates that a receive packet chain is available. If the associated interrupt enable bit is set, an interrupt is also asserted.

**Bit 6: Tx Interrupt.** When set, this bit indicates that a transmit packet or packet chain has been completed. If the associated interrupt enable bit is set, an interrupt is also asserted.

**Bit 7: Buffer Window Interrupt.** When set, this bit indicates that data has been read from the local buffer into the DMA FIFO and is ready to be read via the BIU. If the associated interrupt enable bit has been set, an interrupt is asserted.

**Bit 8: DMA On.** When set, this bit indicates that the DMA logic is enabled. When terminal count is asserted, this bit will be reset to indicate that the DMA activity has been completed.

**Bit 9: Rx On.** When set, this bit indicates that the EDLC receiver is enabled.

**Bit 10: Tx On.** When set, this bit indicates that the EDLC transmitter is enabled.

**Bits 11 & 12: Not used.**

**Bit 13: DMA FIFO Full.** When set, this bit indicates that the DMA FIFO is full.

**Bit 14: DMA FIFO Empty.** When set, this bit indicates that the DMA FIFO is empty.

**Bit 15: FIFO Direction.** When set, this bit indicates that the DMA FIFO is in the read direction; when cleared, it indicates that the DMA FIFO is in the write direction. After hardware or software reset, this bit is cleared.

**Configuration Register 1, A3-0 = 001X<sub>2</sub>**

**Bits 0-3: BufferCode.** These four bits are the buffer window code bits, which determine the source of buffer window register reads and the destination of buffer window register writes.

**Buffer Code Selection Table**

BufferCode Bits				Buffer Window Reg. Contents
3	2	1	0	
0	0	0	0	Station addr. reg. 0
0	0	0	1	Station addr. reg. 1
0	0	1	0	Station addr. reg. 2
0	0	1	1	Station addr. reg. 3
0	1	0	0	Station addr. reg. 4
0	1	0	1	Station addr. reg. 5
0	1	1	0	Address PROM
0	1	1	1	Transmit end area
1	0	0	0	Buffer memory
1	0	0	1	Interrupt vector
1	0	1	X	Reserved — do not use
1	1	X	X	Reserved — do not use

**Bits 4-5: DmaBurstInterval.** These two bits specify the interval between DMA requests.

5	4	Burst Interval
0	0	Continuous
0	1	800 nanoseconds
1	0	1600 nanoseconds
1	1	3200 nanoseconds

If configured for continuous mode, the DMA request will persist until TermCt is asserted.

**Bits 6-7: DmaBurstSize.** These two bits specify the DMA burst size in bytes. In 16 bit mode, the number of transfers is half that in byte mode.

**DMA Burst Size Selection**

7	6	# Bytes Transferred
0	0	2
0	1	4
1	0	8
1	1	16

**Bits 8-13:** These six bits select which of the station address register sets (each register set contains 6 bytes) will be used to compare incoming destination addresses. Bit 8 corresponds to station address register set 0, bit 9 to register set 1, . . . bit 13 to register set 5. A 1 in any bit enables that station address register set for reception. These bits are both read and write.

**Bits 14-15:** These two bits define the match modes for the EDLC receiver logic.

15	14	Matchmode Description
0	0	Specific addresses only
0	1	Specific + broadcast addresses
1	0	Above + multicast addresses
1	1	All frames (promiscuous mode)

**Configuration Register 2, A0-A3 = 010X<sub>2</sub>**

**Bit 0: ByteSwap.** The normal order for packing packet bytes into a 16 bit word is low byte first, i.e., the first byte of a packet is contained in bits 0 through 7, the second byte in bits 8 through 15. Setting this bit to a 1 causes the high and low order bytes to be swapped for data reads and writes to the buffer window when the 8005 is in 16 bit mode. Control registers are not affected. This bit has no effect when the 8005 is in 8 bit mode. It should not be changed when a DMA is in progress. Changing this bit will not affect the sequence of receive data bytes in the local buffer memory since the swap occurs on the system (BIU) side of the buffer memory. This bit is both read and write.

**Bit 1: AutoUpdREA.** If this bit is set to 1, the receive end area register will be updated with the most significant byte of the DMA pointer register after each DMA transfer. In this way, as buffer memory space is released by reading from it, free buffer space is automatically allocated to the receive logic.

**Bit 2: Overflow Enable.** When set, the receive logic will retain partial packets that do not fully fit in the available local buffer space. If cleared, packets that do not fit in the remaining local buffer space will be discarded.

**Bit 3: CRC Error Enable.** When set, the receiver will accept packets with CRC errors, place them in the local buffer and indicate that a packet is available via the Rx Interrupt status bit.

**Bit 4: Dribble Error.** When set, the receiver will accept packets with a byte alignment error.

**Bit 5: Short Frame Enable.** When set, frames of less than 512 bits (64 bytes) exclusive of preamble and start frame delimiter bits will be received and placed in the local buffer. Frames shorter than 6 bytes (2 bytes if bit 8=1) will always be rejected unless the receiver is in promiscuous mode (all addresses match) or multicast/broadcast mode and the packet is a multicast/broadcast packet.

**Bit 6: SlotSelect.** This bit selects the slot time used to calculate backoff time following a collision. When a 0, which is the state after reset, the slot time is 512 bits and meets the IEEE 802.3 standard; when a 1, the slot time is 128 bits, the interframe spacing is 24 bits and the collision jam is 2 bytes long, which is useful for smaller networks such as a serial backplane buses.

**Bit 7: PreamSelect.** When this bit is a 0, which is the state after reset, the 8005 automatically transmits an IEEE 802.3 compatible 64 bit preamble; when set to 1, the user must supply the preamble as part of the packet data. The preamble must still follow the 802.3 form in order to be recognized by other 8005's, but may have arbitrary length. Note that a minimum of 16 preamble bits are required by the 8005 on reception.

**Bit 8: AddrLength.** This bit selects the length of address to be used in address matching. When a 0, which is the state after reset, the length is 6 bytes, which conforms with the IEEE 802.3 standard; when set to 1 the length is 2 bytes, which is useful in limited networks such as serial backplane buses.

**Bit 9: RecCrc.** If set to a 1, received frames will include the CRC (Frame Check Sequence). If set to a 0, which is the state after reset, the 4 byte CRC will be stripped when received.

**Bit 10: XmitNoCrc.** If set to a 1, the transmitter will not append the 4 byte frame check sequence to each frame transmitted. This is useful in local loopback to perform diagnostic checks, since it allows the software to provide its own CRC as the last four bytes of a frame to check the EDLC receiver CRC logic. It is initialized to 0 after hardware or software reset.

**Bit 11: Loopback.** This bit controls the external loopback pin. When set to a 1, the loopback output pin is at Vol; after reset or when cleared to a 0, the loopback output pin is at Voh.

**Bit 12: WatchTimeDis.** This bit controls the external watchdog timer disable pin. When set to a 1, the watchdog timer disable pin is at Voh; when cleared to 0 or after reset, the watchdog timer disable pin is at Vol.

**Bits 13-14:** Not used.

**Bit 15: ChipRst.** Writing a 1 to this bit is the same as asserting the hardware reset input. Chip reset should be followed by a 4 μs wait before attempting another access. Reads as a 0.

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**Receive End Area Register, A3-0 = 011X<sub>2</sub>**

**Bits 0-7: ReaPtr.** The receive end area pointer contains the high order byte of the local buffer address at which the receive logic must stop to prevent writing over previously received packets. If the receive logic reaches this address it will stop and wait for a packet that will fit into the available space. If receive overflow is not enabled, frames that do not fit will be discarded. If receive overflow is enabled, the receive logic will receive as much as will fit and mark receive overflow in the receive status. If space later becomes available, the receive logic will again continue to fill it. This register can be updated automatically by setting bit 1 in configuration register #2, which causes ReaPtr to be updated after each DMA read. It is both read and write.

**Buffer Window Register, A3-0 = 100X<sub>2</sub>**

This register provides access to the area specified by the buffer code bits (bits 0-3) in configuration register #1. When the buffer code points to either the buffer memory (Bcode=1000<sub>2</sub>) or the address PROM (Bcode=0110<sub>2</sub>), the address of the data transferred through this register is determined by the DMA pointer register.

**Receive Pointer Register, A3-0 = 101X<sub>2</sub>**

The receive pointer register provides a 16 bit address that points to the next buffer memory location into which data or header information will be placed by the receive logic. The low order 8 bits contain the least significant byte of the address. Prior to enabling the receiver, this register should be set to point to the beginning of the receive area in the local buffer. This initial value should be remembered by system software since it will be the address of the first byte of the header block of the first packet received. While receiving, the receive pointer will be incremented for each byte stored into the local buffer. When the receive pointer increments past hex FFFF the most significant byte will be set equal to the value of the transmit end area + 1 and the least significant byte will be set to 00. Reading this register may be done at any time. It should be written only when the receiver is idle.

**Transmit Pointer Register, A3-0 = 110X<sub>2</sub>**

The transmit pointer register points to the current location being accessed by the transmit logic. Before starting the transmitter, software loads this register with the address of the beginning of a transmit packet chain.

**DMA Address Register, A3-0 = 111X<sub>2</sub>**

The DMA address register provides 16 bits of address information to the local buffer memory and 8 bits of address to the address PROM, depending on the buffer

code written into configuration register 1. Its normal use is to provide an auto-incremented address to the local buffer so that packet data can be moved via the BIU. **When the DMA address register is loaded, the DMA FIFO is cleared.** Therefore it is important to insure that the DMA FIFO is empty if it is in the write direction before loading the DMA register. When writing a packet to be transmitted, the DMA address register automatically wraps around to 0000 when the transmit end area (contained in an indirect register, buffer code 0111<sub>2</sub>) has been reached. When reading receive packets, the DMA address register automatically wraps around to the receive start area (transmit end area + 1) when address \$FFFF has been read.

**Indirectly Accessed Registers**

Infrequently used registers, e.g., those that are normally loaded only when initially configuring the 8005, are accessed indirectly by first loading the buffer code bits in configuration register #1 with a code that points to the desired register. Reads and writes occur through the buffer window register. All indirect registers (a total of 38) are 8 bits wide, thus only D0-D7 are used.

**Station Address Registers**

The 8005 contains six 48-bit station address registers, which permits one network connection to provide up to 6 different server functions. Each of these station address registers is comprised of six 8-bit registers which must be loaded through the buffer window register. Only those station address registers that will be enabled for address matching need to be loaded.

To load a station address register, first insure that the associated station address enable bit is not set to a 1. Select the desired station number (0-5) by writing the buffer code bits in configuration register #1. Next do 6 sequential byte writes to the buffer window register as follows: Write the most significant byte of the 6 byte station address; its low order bit, bit 0, will be the first bit received. Next write the remaining 5 bytes in descending order. To read a station address register, select the desired station number by writing the buffer code bits in configuration register #1. Do 6 sequential reads to the buffer window; the first byte read will be the most significant byte. If the 8005 is configured to match 2 byte instead of 6 byte addresses, only the first 2 station address bytes are significant, although all 6 will read and write properly.

**Transmit End Area Pointer**

The 8 bit value in this register defines, with 256 location granularity, the end of the transmit packet buffer area by specifying the highest value permitted in the most significant byte of the transmit pointer register and, when loading a packet to be transmitted, the DMA address register. It also indirectly defines the receive start area

address, since the PBC automatically calculates the high order byte of this address by adding 1 to the transmit end area pointer. To read or write this value, load the buffer code bits of configuration register #1 with the code for the transmit end area, and do a read or write to the buffer window register.

#### **Interrupt Vector Register**

This read/write register is accessed through the buffer window register when the buffer code in configuration register #1 is 9. It contains an 8 bit vector which is placed on data bits D0-D7 during an interrupt acknowledge cycle. If  $BUSMODE=0$ , an interrupt acknowledge cycle is defined by  $INT^*=0$ ,  $IACK^*=0$  and  $READ/WRITE^*=1$ . When  $BUSMODE=1$ , an interrupt acknowledge cycle is defined by  $INT=1$ ,  $IACK^*=0$ , and  $IOR^*=0$ .

#### **Other Buffer Window Register Uses**

##### **Address PROM Access**

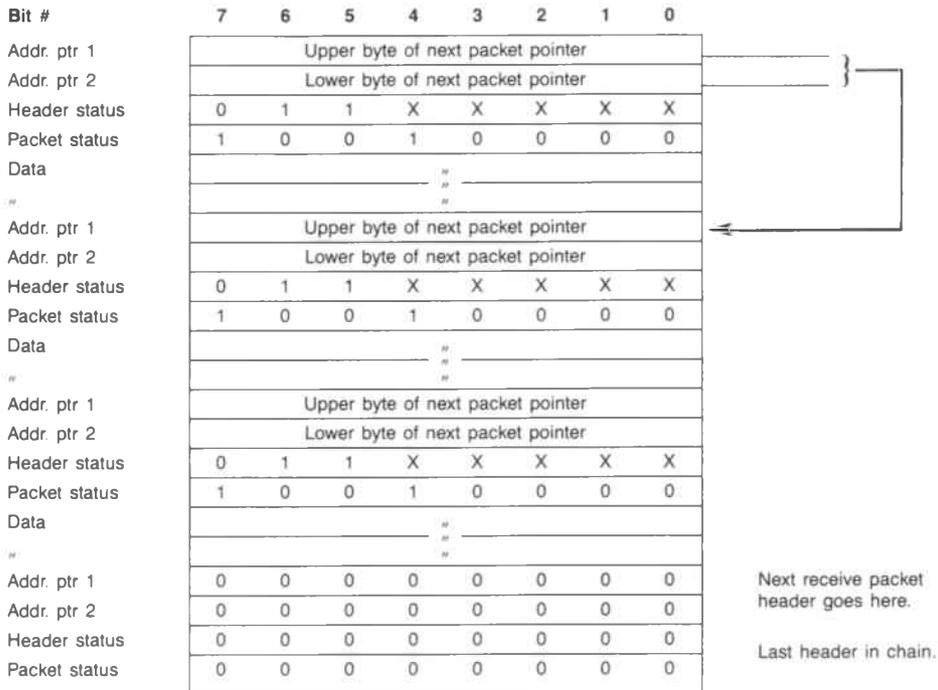
The 8005 supports access to up to 256 bytes of configuration data contained in a PROM or EEPROM. This can be used for any purpose, such as storing station addresses, register configurations, network connection data, etc. The address to the PROM is supplied by the DMA register through data bus bits D8-D15; the data lines from the PROM are connected to D0-D7. Chip select for the PROM is provided by output APEN\*. Before accessing this PROM, insure that transmit, receive and DMA sections of the 8005 are disabled. Next load the PROM starting address which you wish to access into the low

byte of the DMA register. Set the buffer code bits in configuration register #1 to point to the address PROM. Each access to the buffer window register will chip enable the PROM, permitting reads or writes. Successive accesses will increment the DMA register to point to the next byte in the PROM. If a 16 bit wide bus is used, the address supplied to the PROM will also be read on D8-D15.

##### **Buffer Memory Access**

The normal state of the buffer code bits, once the 8005 has been initialized with station addresses and buffer areas have been allocated, is with buffer memory selected. Access to the local buffer memory is provided by the DMA register, which automatically increments after each byte or word transfer. To read from or write to the local buffer, set the buffer code to select the buffer memory, load a starting address into the DMA register and read from or write to the buffer window register. This is the simplest way to access the local buffer as it requires no system DMA activity. It also permits network layer software to read network control data at the beginning of a received packet to determine if it is necessary to move the packet into global memory for further processing or simply reuse the area occupied by the packet by updating the receive end area register. For fastest transfer speed, e.g., to move packet data, an external system DMA controller is supported via the DMA Request output, DMA Acknowledge input and Terminal Count input signals.

**Example of Chained Receive Frames**



**Packet Header Bytes**

**Transmit Header Command Byte (Byte #3)**

7	6	5	4	3	2	1	0
1	Chain Continue	Data Follows	Not Used	Xmit Success Enable	16 Coll. Enable	Coll. Int. Enable	Babble Int. Enable

**Receive Header Status Byte (Byte #3)**

7	6	5	4	3	2	1	0
0	Chain Continue	Data Follows	Not Used				

**Transmit Packet Status Byte (Byte #4)**

7	6	5	4	3	2	1	0
Done	Reserved		16 Coll.	Coll. sion	Bab-	bble	

**Receive Packet Status Byte (Byte #4)**

7	6	5	4	3	2	1	0
Done	Over-flow	Not Used	Not Used	Short Frame	Drib. Error	CRC Error	Over-size

8005 Configuration and Pointer Registers

Command (write only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Write	FIFO Read	Set Tx Off	Set Rx Off	Set DMA Off	Set Tx On	Set Rx On	Set DMA On	Bufr Wndow Ack	Tx Int Ack	Rx Int Ack	DMA Int Ack	Bufr Wndow Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Status (read only) (A3-0 = 000X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIFO Dir	FIFO Empty	FIFO Full	Not Used	Not Used	Tx On	Rx On	DMA On	Bufr Wndow Int	Tx Int	Rx Int	DMA Int	Bufr Wndow Enable	Tx Int Enable	Rx Int Enable	DMA Int Enable

Configuration Register #1 (A3-0 = 001X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Addr Match Mode	Addr Match Mode	Sta. 5 Enable	Sta. 4 Enable	Sta. 3 Enable	Sta. 2 Enable	Sta. 1 Enable	Sta. 0 Enable	DMA Burst Lngth	DMA Burst Lngth	DMA Burst Intvl	DMA Burst Intvl	Bufr Code 3	Bufr Code 2	Bufr Code 1	Bufr Code 0

Configuration Register #2 (A3-0 = 010X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reset	Not Used	Not Used	Watch Time Dis.	Loop-Back	Xmit No CRC	Recv. CRC	Addr Leng.	Xmit No Pream	Slot Time Sel.	Short Frame Enable	Drib Error Enable	CRC Error Enable	Over-flow Enable	Auto Update REA	Byte Swap

Receive End Area Register (A3-0 = 011X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	Receive End Area Pointer							

Receive Pointer Register (A3-0 = 101X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT RECEIVE BYTE															

Transmit Pointer Register (A3-0 = 110X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR NEXT TRANSMIT BYTE															

DMA Address Register (A3-0 = 111X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOCAL BUFFER ADDRESS FOR SYSTEM READS OR WRITES															

Buffer Window Register (A3-0 = 100X)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BUFFER CODE BITS DETERMINE SOURCE/DESTINATION FOR READS AND WRITES															

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**Station Address Register Format**  
**2 of 6 Station Address Registers Shown**

7	6	5	4	3	2	1	0		7	6	5	4	3	2	1	0	
STATION ADDRESS REGISTER 0 BYTE 0 BUFFER CODE = 0000								M S B	STATION ADDRESS REGISTER 1 BYTE 0 BUFFER CODE = 0001								M S B
STATION ADDRESS REGISTER 0 BYTE 1 BUFFER CODE = 0000									STATION ADDRESS REGISTER 1 BYTE 1 BUFFER CODE = 0001								
STATION ADDRESS REGISTER 0 BYTE 2 BUFFER CODE = 0000									STATION ADDRESS REGISTER 1 BYTE 2 BUFFER CODE = 0001								
STATION ADDRESS REGISTER 0 BYTE 3 BUFFER CODE = 0000									STATION ADDRESS REGISTER 1 BYTE 3 BUFFER CODE = 0001								
STATION ADDRESS REGISTER 0 BYTE 4 BUFFER CODE = 0000									STATION ADDRESS REGISTER 1 BYTE 4 BUFFER CODE = 0001								
STATION ADDRESS REGISTER 0 BYTE 5 BUFFER CODE = 0000									STATION ADDRESS REGISTER 1 BYTE 5 BUFFER CODE = 0001								

**Absolute Maximum Stress Ratings**

Temperature:  
 Storage ..... -65°C to +150°C  
 Under Bias ..... -10°C to +80°C  
 All Inputs and Outputs with  
 Respect to V<sub>SS</sub> ..... +6 V to -0.3 V

**Recommended Operating Conditions**

V <sub>CC</sub> Supply Voltage	5V ± 10%
Ambient Temperature	0°C to 70°C

**DC Operating Characteristics** (Over the V<sub>CC</sub> and Temperature Ranges)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>IL</sub>	Input/Output Leakage		10 -10	μA μA	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = 0.1V
I <sub>CC</sub>	Active V <sub>CC</sub> Current		300	mA	CS* = V <sub>IL</sub> , Outputs Open
V <sub>IL</sub>	Input Low Voltage	-0.3	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 1	V	
V <sub>OL1</sub>	Output Low Voltage (except AD <sub>0-7</sub> )		0.40	V	I <sub>OL</sub> = 2.1 mA
V <sub>OL2</sub>	Output Low Voltage (AD <sub>0-7</sub> )		0.40	V	I <sub>OL</sub> = 200 μA
V <sub>OH1</sub>	Output High Voltage (except AD <sub>0-7</sub> )	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>OH2</sub>	Output High Voltage (AD <sub>0-7</sub> )	2.4		V	I <sub>OH</sub> = -200 μA

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Capacitance** (Characterized — Not Tested)  
**Ambient Temperature = 25°C, F = 1 MHz**

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
C <sub>IN</sub>	Input Capacitance		15	pF	V <sub>IN</sub> = 0
C <sub>OUT</sub>	Output Capacitance		15	pF	V <sub>OUT</sub> = 0

**Electrostatic Discharge Characteristics** (Characterized — Not Test)

Symbol	Parameter	Value	Test Condition
V <sub>ZAP</sub>	E.S.D. Tolerance	> 2000 V	Mil-STD 883 Meth. 3015

**A.C. Test Conditions**

Output Load:

AD0-AD7, RAS\*, CAS\*, W\*, G\*: I(load) = ± 200 μA,  
 C(load) = 50 pF.

All Other Outputs: 1 TTL Gate and C(load) = 100 pF.

Input Rise and Fall Times (except TXC, RXC, CLK):  
 10 ns. maximum.

Input Rise and Fall Times (TXC, RXC, CLK):  
 5 ns. maximum.

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs: 1 V and 2 V

Outputs: 0.8 V and 2 V

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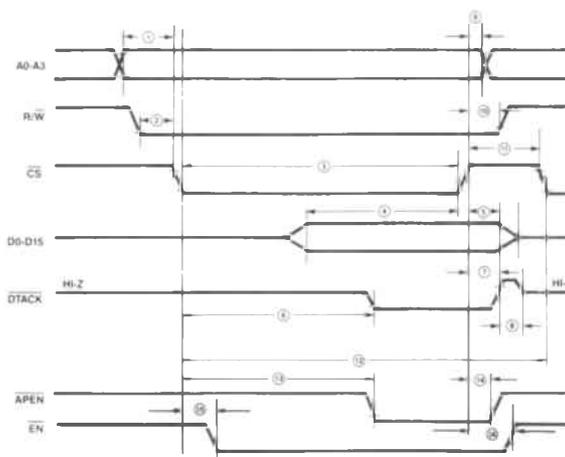
**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
Over the operating  $V_{CC}$  and Temperature Range

**Table A. Bus Write Cycle – BUSMODE = 0**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	20		ns
2	TRWVCSL	R/W* Setup Time	20		ns
3	TCSLCSH	CS* Pulse Width	100		ns
4	TDVCSL	Data Setup Time	70		ns
5	TCSHDX	Data Hold Time	0		ns
6	TCSLDTL	DTACK* Assertion Delay <sup>3</sup>		50	ns
7	TCSHDTH	DTACK* Deassertion Delay		50	ns
8	TCSHDTZ	DTACK* Hi-Z Delay		50	ns
9	TCSHAX	Address Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHCSL	Write Recovery Time	205		ns
12	TCSLCSL	Write Cycle Time: a. FIFO Data Write <sup>1</sup> b. Configuration Regs. <sup>1,2</sup> c. Pointer Regs. <sup>1,2</sup>	600 800 1600		ns ns ns ns
13	TCSLAPL	APEN* Assert Time		50	ns
14	TCSHAPH	APEN* Deassert Time		50	ns
15	TCSLENL	EN* Assert Delay		50	ns
16	TCSHENH	EN* Deassert Delay		50	ns

**NOTES:**

- Cycle times are for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns. from these times
- Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, and Station Address Registers  
Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Register
- DTACK\* assertion will be delayed for all subsequent reads or writes until reference 12 cycle time has elapsed.



**Figure A. Bus Write Cycle Timing Diagram — BUSMODE = 0**

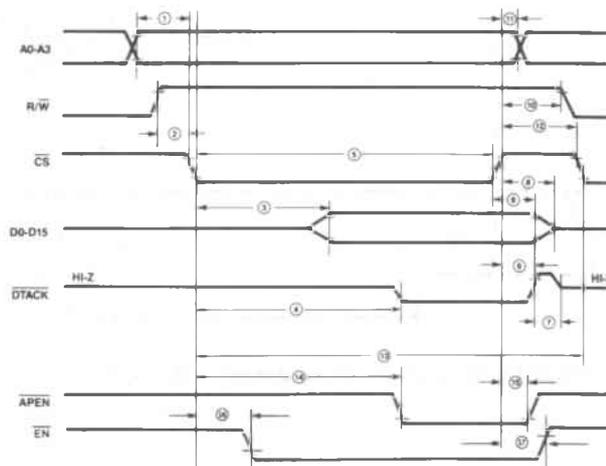
**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table B. Bus Read Cycle —  $BUSMODE = 0$**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVCSL	Address Setup Time	20		ns
2	TRWVCSL	R/W* Setup Time	20		ns
3	TCSLDV	Read Data Delay from CS*: a. FIFO Data b. Configuration Regs. <sup>1,2</sup> c. Other Pointer Regs. <sup>1,2</sup>		100 700 1500	ns ns ns ns
4	TCSLDTL	DTACK* Assertion Delay	ref. 3 + 50		ns
5	TCSLCSH	CS* Pulse Width	100		ns
6	TCSHDTH	DTACK* Deassertion Delay		50	ns
7	TCSHDTZ	DTACK* Hi-Z Delay		50	ns
8	TCSHDZ	Data Hi-Z Delay		100	ns
9	TCSHDX	Data Hold Time	20		ns
10	TCSHRWX	R/W* Hold Time	20		ns
11	TCSHAX	Address Hold Time	20		ns
12	TCSHCSL	Read Recovery Time	205		ns
13	TCSLCSL	Read Cycle Time	305		ns
14	TCSLAPL	APEN* Assert Delay		50	ns
15	TCSHAPH	APEN* Deassert Delay		50	ns
16	TCSLENL	EN* Assert Delay		50	ns
17	TCSHENH	EN* Deassert Delay		50	ns

**NOTES:**

1. Cycles times are for 16 bit writes. If  $BUSIZE = 0$  (8 bit writes), subtract 200 ns. from these times.
2. Configuration Registers are: Command/Status Register, Configuration Register # 1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers. Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register.



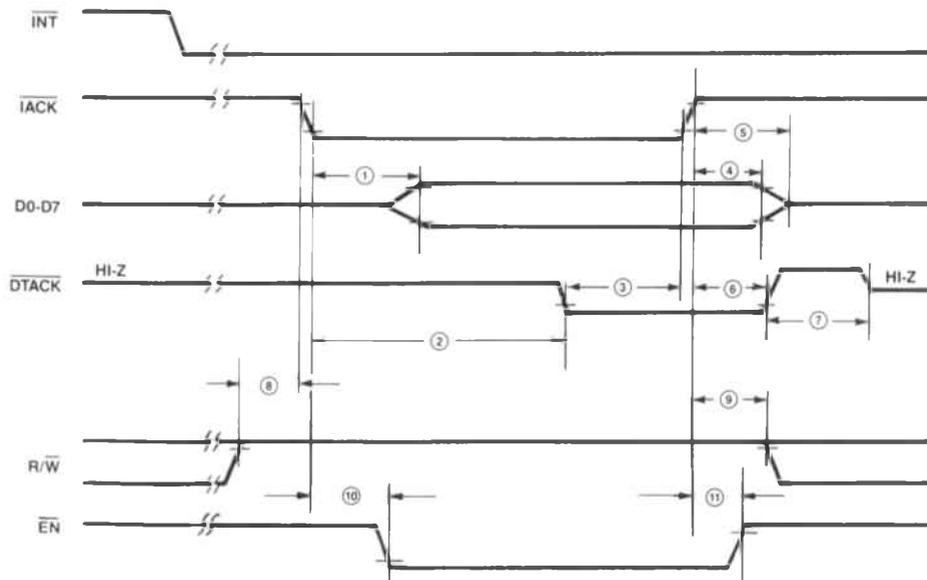
**Figure B. Bus Read Cycle Timing Diagram —  $BUSMODE = 0$**

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**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table C. Interrupt Cycle – BUSMODE = 0**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TIAVQV	Data Delay from IACK*		500	ns
2	TIAVDTV	DTACK* Delay from IACK*		500	ns
3	TDTLIAH	IACK* Hold from DTACK*	0		ns
4	TIAHDX	Data Hold from IACK* Deassert	20		ns
5	TIAHDZ	Data Hi-Z from IACK* Deassert		100	ns
6	TIAHDTH	DTACK* Deassert from IACK*		50	ns
7	TIAHDTZ	DTACK* Hi-Z from IACK* Deassert		50	ns
8	TRHIAL	R/W* Setup Time	20		ns
9	TIAHRX	R/W* Hold Time from IACK*	0		ns
10	TIALENL	EN* Assert Delay		50	ns
11	TIAHENH	EN* Deassert Delay		50	ns



**Figure C. Interrupt Cycle Timing Diagram – BUSMODE = 0**

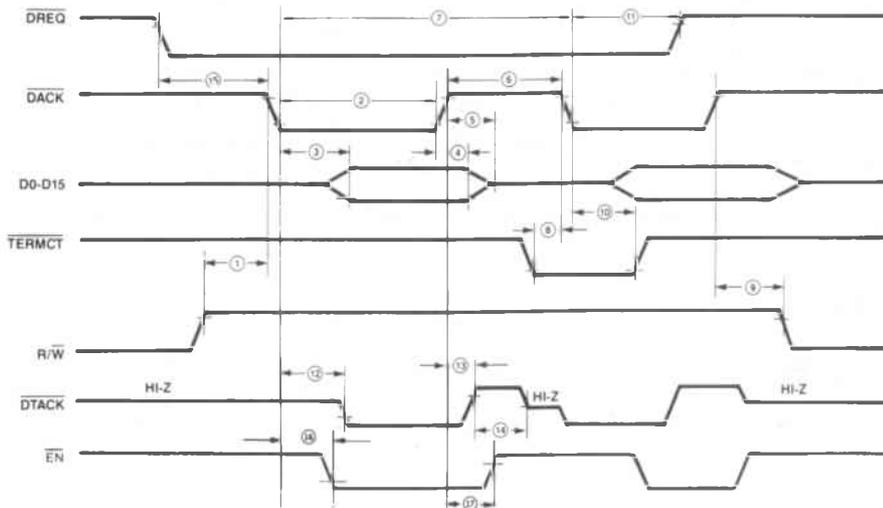
**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table D. DMA Read Cycle - BUSMODE = 0**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWHDAL	R/W* Setup Time	20		ns
2	TDALDAH	DACK* Pulse Width	100		ns
3	TDALDV	Data Delay Time		100	ns
4	TDAHDX	Data Hold Time		20	ns
5	TDAHDZ	Data Hi-Z Delay		100	ns
6	TDAHDAL	Read Recovery Time	205		ns
7	TDALDAL	DMA Read Cycle Time	305		ns
8	TTCLDAL	TERMCT Setup Time	0		ns
9	TDAHRWX	R/W* Hold Time	20		ns
10	TDAHTCX	TERMCT Hold Time	100		ns
11	TDALDRH	DREQ* Delay <sup>2</sup>		200	ns
12	TDALDTL	DTACK* Assertion Delay		100	ns
13	TDAHDTH	DTACK* Deassertion Delay		50	ns
14	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
15	TDRLDAL	DREQ* Setup to DACK*	0		ns
16	TDALLENL	EN* Assert Delay		50	ns
17	TDAHENH	EN* Deassert Delay		50	ns

**NOTES:**

- 1 Subtract 200 ns for BUSSIZE = 0 (8 bit bus).
- 2 DREQ deassert delay for end of DMA burst. If DREQ is deasserted due to TERMCT, the time is measured from the falling edge of TERMCT.



**Figure D. DMA Read Cycle Timing Diagram - BUSMODE = 0**

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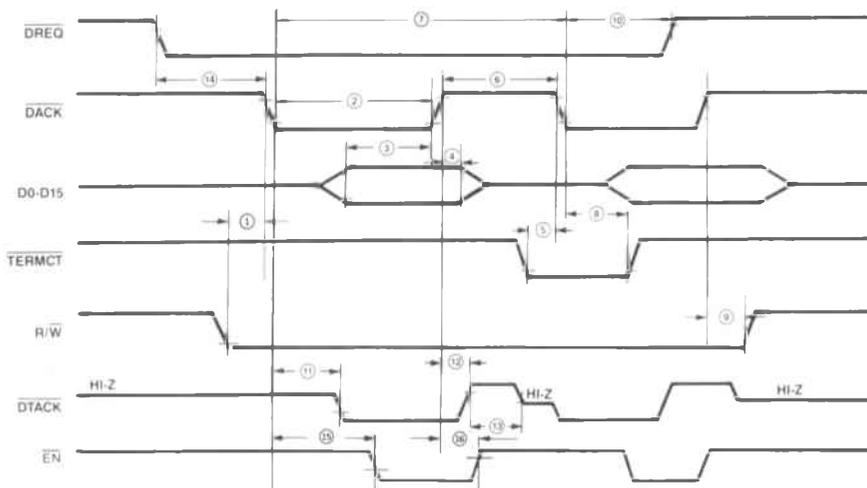
**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table E. DMA Write Cycle – BUSMODE = 0**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRWLDAL	R/W* Setup Time	20		ns
2	TDALDAH	DACK* Pulse Width	100		ns
3	TDVDAH	Data Setup Time	70		ns
4	TDAHDX	Data Hold Time	0		ns
5	TTCLDAL	TERMCT* Setup Time	0		ns
6	TDAHDAL	Write Recovery Time	205		ns
7	TDALDAL	DMA Write Cycle Time <sup>1</sup>	505		ns
8	TDALTCH	TERMCT* Hold Time	100		ns
9	TDAHRWH	R/W* Hold Time	20		ns
10	TDALDRH	DREQ* Delay <sup>2</sup>		200	ns
11	TDALDTL	DTACK* Assertion Delay		100	ns
12	TDAHDTH	DTACK* Deassertion Delay		50	ns
13	TDTHDTZ	DTACK* Hi-Z Delay		50	ns
14	TDRLDAL	DREQ* Setup to DACK*	0		ns
15	TDALLENL	EN* Assert Delay		50	ns
16	TDAHENH	EN* Deassert Delay		50	ns

**NOTES:**

- 1. Subtract 200 ns for BUSSIZE = 0 (8 bit bus).
- 2. DREQ deassert delay for end of DMA burst. If DREQ is deasserted due to TERMCT, the time is measured from the falling edge of TERMCT.



**Figure E. DMA Write Cycle Timing Diagram — BUSMODE = 0**

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

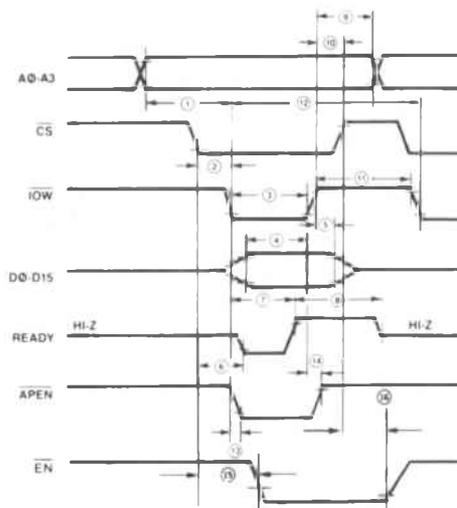
**Table F. Bus Write Cycle – BUSMODE = 1**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVWL	Address Setup Time	20		ns
2	TCSLWL	CS* Setup Time	20		ns
3	TWLWH	IOW* Pulse Width	100		ns
4	TDVWH	Data Setup Time	70		ns
5	TWHDX	Data Hold Time	0		ns
6	TCSLRYL	READY Deassert Delay		50	ns
7	TWLRyh	READY Assert Delay		50	ns
8	TRYHRYZ	READY Delay to Hi-Z		50	ns
9	TWHAX	Address Hold Time	20		ns
10	TWHCSH	CS* Hold Time	20		ns
11	TWHWL	Write Recovery Time	205		ns
12	TWLCSL	Write Cycle Time a. FIFO Data Write <sup>1</sup> b. Configuration Regs. <sup>1,2</sup> c. Pointer Registers <sup>1,2</sup>	600 800 1600		ns ns ns
13	TWLAPL	APEN* Assert Delay		50	ns
14	TWHAPH	APEN* Deassert Delay		50	ns
15	TCSLENL	EN* Assert Delay		50	ns
16	TCSHENH	EN* Deassert Delay		50	ns

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**NOTES:**

- Cycle times are for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns. from these times
- Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers  
 Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, Transmit End Area Register, and DMA Pointer Register



**Figure F. Write Cycle Timing Diagram — BUSMODE = 1**

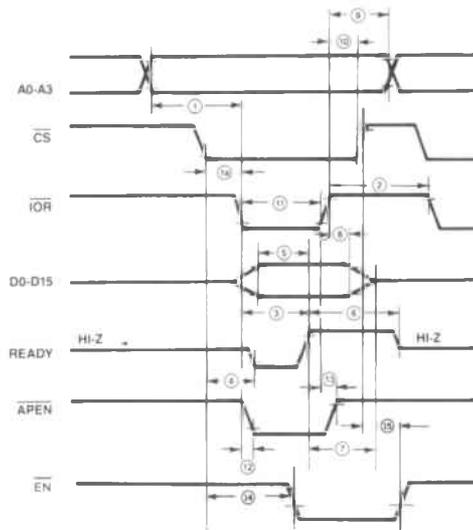
**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table G. Bus Read Cycle – BUSMODE = 1**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRL	Address Setup Time	20		ns
1a	TCSLRL	CS* Setup Time	20		ns
2	TRHRL	Read Recovery Time	205		ns
3	TRLRYH	READY Assert Delay a. FIFO Data b. Configuration Regs. <sup>1,2</sup> c. Pointer Registers <sup>1,2</sup>		100 700 1500	ns ns ns
4	TCSLRYL	READY Deassertion Delay		50	ns
5	TDVRYH	Data Setup to READY Deassert	20		ns
6	TRYHRYZ	READY Delay to Hi-Z		50	ns
7	TRHDX	Data Hold Time	20		ns
8	TRHDZ	Data Delay to Hi-Z		100	ns
9	TRHAX	Address Hold Time	20		ns
10	TRHCSH	CS* Hold Time	20		ns
11	TRLRH	IOR* Pulse Width	100		ns
12	TRLAPL	APEN* Assert Delay		50	ns
13	TRHAPH	APEN* Deassert Delay		50	ns
14	TCSLENL	EN* Assert Delay		50	ns
15	TCSHENH	EN* Deassert Delay		50	ns

**NOTES:**

- Cycle times are for 16 bit writes. If BUSSIZE = 0 (8 bit writes), subtract 200 ns. from these times.
- Configuration Registers are: Command/Status Register, Configuration Register #1 & 2, Interrupt Vector Register, DMA Pointer Register, and Station Address Registers  
 Pointer Registers are: Receive End Area Pointer, Receive Pointer Register, Transmit Pointer Register, and Transmit End Area Register

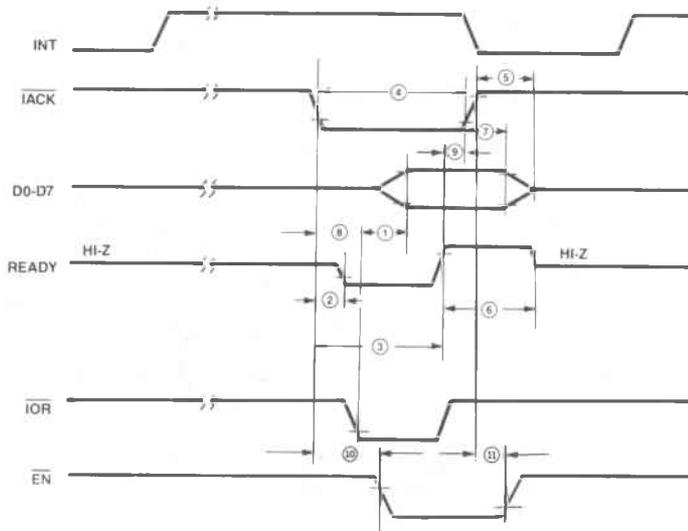


**Figure G. Read Cycle Timing Diagram – BUSMODE = 1**

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table H. Interrupt Cycle - BUSMODE = 1**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRLDV	Data Delay from IOR*		500	ns
2	TIALRYL	READY Deassertion Delay		50	ns
3	TRLRYH	READY Assert Delay		500	ns
4	TIALIAH	IACK Pulse Width	350		ns
5	TIAHDZ	Data Delay to Hi-Z		100	ns
6	TRYHRYZ	READY Delay to Hi-Z		50	ns
7	TIAHDX	Data Hold from IACK* or IOR*	20		ns
8	TELR	IACK* Setup Time	20		ns
9	TRYHIAH	READY Assert to IACK*	0		ns
10	TIALENL	EN* Assert Delay		50	ns
11	TIAHENH	EN* Deassert Delay		50	ns



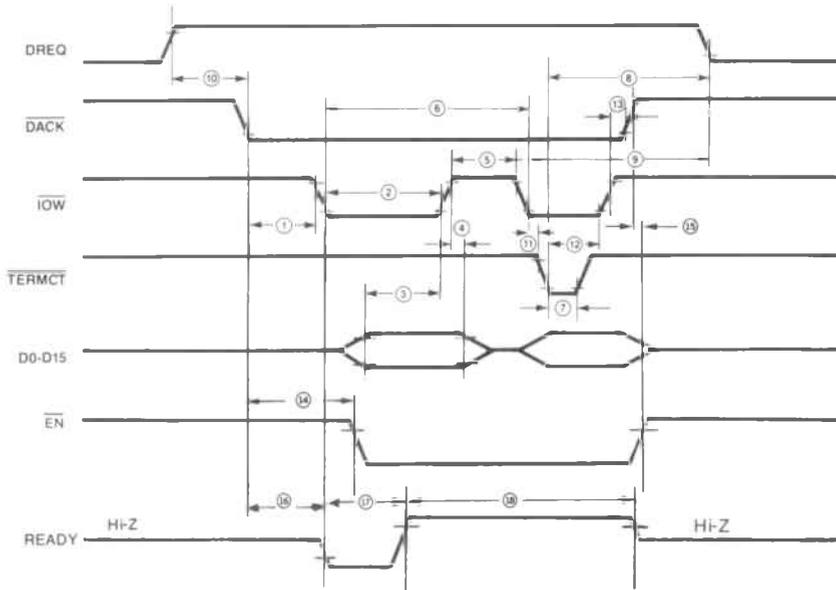
**Figure H. Interrupt Cycle Timing Diagram — BUSMODE = 1**

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**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table I. DMA Write Cycle -  $BUSMODE = 1$**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALWL	DACK* Setup Time	20		ns
2	TWLWH	IOW* Pulse Width	100		ns
3	TDVWH	Data Setup Time	70		ns
4	TWHDX	Data Hold Time	0		ns
5	TWHWL	Write Recovery Time	205		ns
6	TWLWL	Write Cycle Time	305		ns
7	TTCLTCH	TERMCT Pulse Width	80		ns
8	TTCLDRL	DREQ Delay		150	ns
9	TWLDRL	DREQ Delay from IOW*		100	ns
10	TDRHDAL	DACK* Delay	0		ns
11	TRLTCL	TERMCT* Assert Delay	20		ns
12	TTCLWH	IOW* Hold Time	80		ns
13	TWHDAH	DACK* Hold Time	0		ns
14	TDALENL	EN* Assert Delay		50	ns
15	TAHENH	EN* Deassert Delay		50	ns
16	TDALRYL	READY Deassert Delay		50	ns
17	TWLRZH	READY Assert Delay		50	ns
18	TRYHRYZ	READY Delay to Hi-Z		50	ns

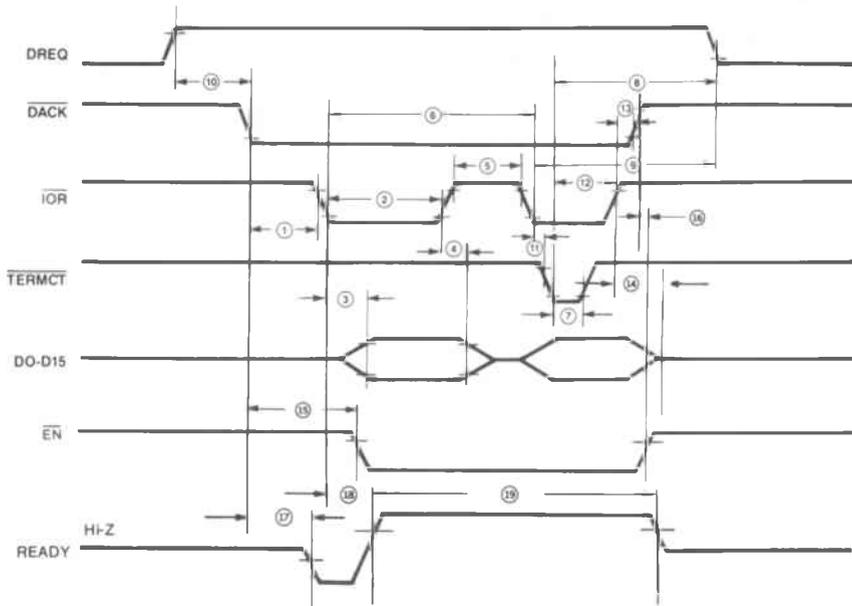


**Figure I. DMA Write Cycle Timing Diagram -  $BUSMODE = 1$**

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table J. DMA Read Cycle -  $BUSMODE = 1$**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TDALRL	DACK* Setup Time	20		ns
2	TRLRH	IOR* Pulse Width	100		ns
3	TRLDV	Data Delay Time		100	ns
4	TRHDX	Data Hold Time	20		ns
5	TRHRL	Read Recovery Time	205		ns
6	TRLRL	Read Cycle Time	305		ns
7	TTCLTCH	TERMCT* Pulse Width	80		ns
8	TTCLDRL	DREQ Delay		100	ns
9	TDALDRL	DREQ Delay from IOR*		100	ns
10	TDRHDAL	DACK* Delay	0		ns
11	TRLTCL	TERMCT* Assert Delay	20		ns
12	TTCLRHL	IOR* Hold Time	80		ns
13	TRHDAH	DACK* Hold Time	0		ns
14	TRHDZ	Data Hi-Z Delay		50	ns
15	TDALENL	EN* Assert Delay		50	ns
16	TDALENL	EN* Deassert Delay		50	ns
17	TDALRYL	READY Deassert Delay		50	ns
18	TRLRYH	READY Assert Delay		50	ns
19	TRYHRYZ	READY Delay to Hi-Z		50	ns



**Figure J. DMA Read Cycle Timing Diagram -  $BUSMODE = 1$**

MICRO/  
DATA COM

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table K. Local Buffer Read or Write Cycle**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TRSLAX	Row Address Hold Time	150		ns
2	TAVRSL	Row Address Setup Time	5		ns
3	TRSHRSL	RAS* Pulse Width High	200		ns
4	TCSLAX	Column Address Hold Time	45		ns
5	TAVCSL	Column Address Setup Time	5		ns
6	TCSHCSL	CAS* Pulse Width – High	60		ns
7	TCSLCSH	CAS* Pulse Width – Low	110		ns
8	TCSLAZ	Address Hi-Z Time	0		ns
9	TGLCH	G* Setup Time	60		ns
10	TDVCSH	Data Setup to CAS*	15		ns
11	TCSHDX	Data Hold from CAS Deassert	0		ns
12	TCSHDZ	Data Hi-Z from CAS Deassert		40	ns
13	TAVAV	Read or Write Cycle Time a. Single Cycle b. Page Mode	600 200		ns ns
14	TDVWL	Data Setup Time	10		ns
15	TWLDX	Data Hold Time	60		ns
16	TWLWH	Write Pulse Width	60		ns
17	TCSLWL	CAS* Setup to W*	50		ns
18	TWLCSH	Write Setup Time	50		ns
19	TCSLWH	Write Hold Time	150		ns
20	TRSLRSL	RAS* Cycle Time	600		ns

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

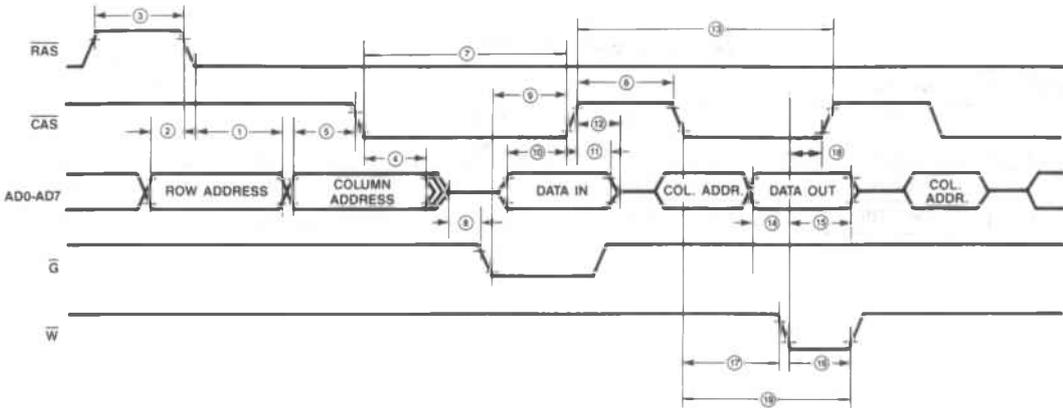


Figure K1. Local Dram Buffer Page-Mode Read and Write Cycle Timing Diagram

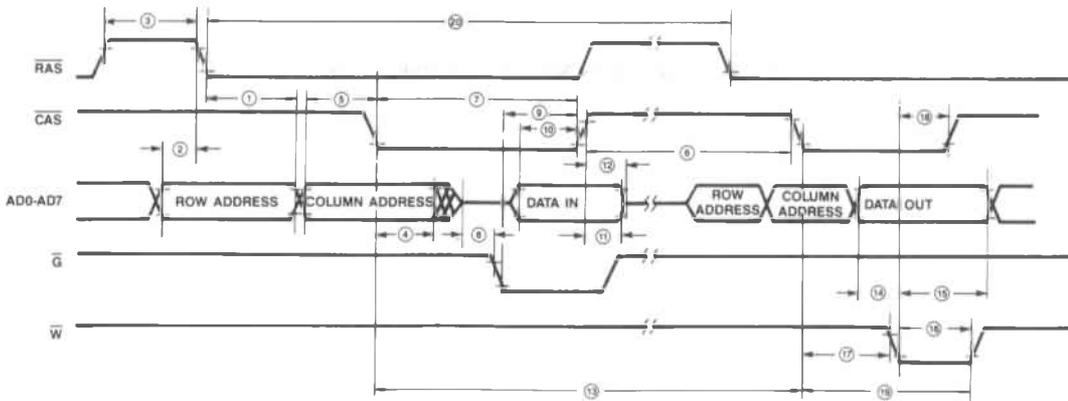


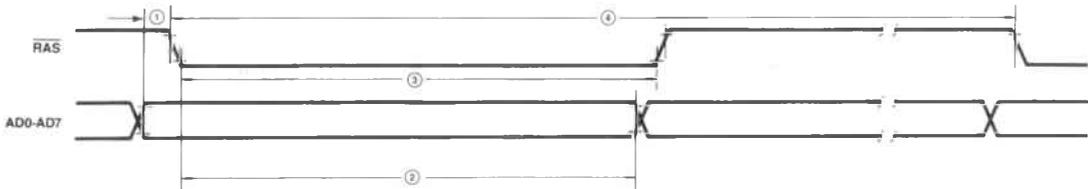
Figure K2. Local Dram Buffer Single Cycle Read and Write Cycle Timing Diagram

MICRO/  
DATA COM

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table L. Local Buffer Refresh Cycle**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TAVRSL	Address Setup Time to RAS*	5		ns
2	TRSLAX	Address Hold Time from RAS*	150		ns
3	TRSLRSH	RAS* Pulse Width	200		ns
4	TRSLRSL	RAS* Cycle Time	400		ns

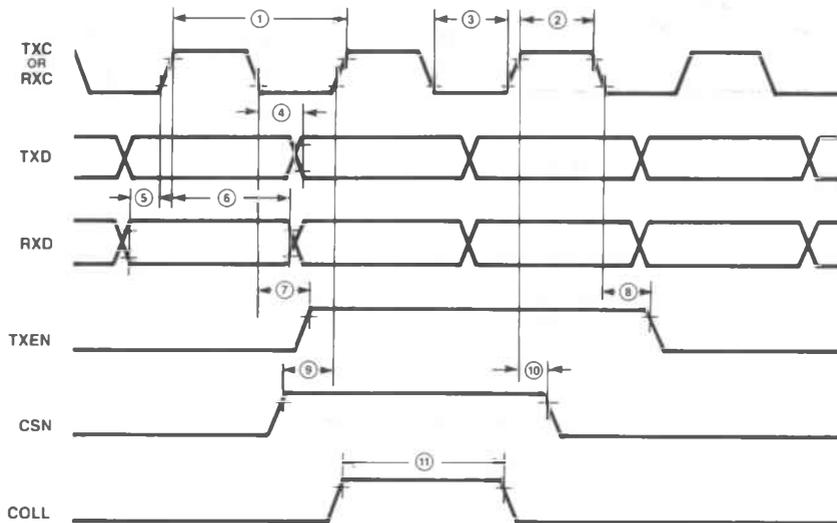


**Figure L. Local Dram Buffer Refresh Cycle Timing Diagram**

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table M. Serial Interface Timing**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKH	$T_{XC}/R_{XC}$ Cycle Time	95	1010	ns
2	TCKHCKL	$T_{XC}/R_{XC}$ High Width	45		ns
3	TCKLCKH	$T_{XC}/R_{XC}$ Low Width	45		ns
4	TCKLDV	$T_{XD}$ Delay from $T_{XC}$		60	ns
5	TDVCKH	$R_{XD}$ Setup to $R_{XC}$	30		ns
6	TCKHDX	$R_{XD}$ Hold Time from $R_{XC}$	20		ns
7	TCKLTEH	$T_{XEN}$ Delay from $T_{XC}$		60	ns
8	TCKLTEL	$T_{XEN}$ Hold Time from $T_{XC}$	20		ns
9	TCSHCKH	CSN Setup to $R_{XC}$	20		ns
10	TCKHCSL	CSN Hold Time from $R_{XC}$	20		ns
11	TCHCL	COLL Pulse Width	Ref. 1+10		ns



**Figure M. Serial Transmit & Receive Interface Timing**

MICRO/  
DATA COM

**A.C. Characteristics** (Assuming 20 MHz Input Master Clock)  
**Over the operating  $V_{CC}$  and Temperature Range**

**Table N. Master Clock and Reset Timing**

Ref. #	Symbol	Description	Min.	Max.	Units
1	TCKHCKL	CLK Pulse Width High	15		ns
2	TCKLCKH	CLK Pulse Width Low	15		ns
3	TCKHCKH	CLK Cycle Time	49.9	50.1	ns
4	TRSLRSH	Reset Pulse Width	10		$\mu$ s

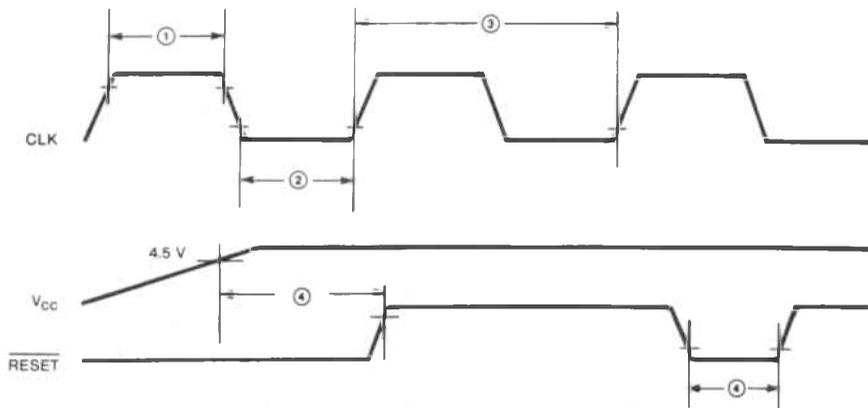


Figure N. Master Clock Timing

**Ordering Information**

**PART NUMBER**



4

**MILITARY**

(Military and Industrial Temperature Range)



SEEQ's Management emphasis is on Quality in products and performance, converting the results of the Technology evolution and innovations to the greatest benefit of our customers with an ever increased degree of system reliability, quality, and functionality.

SEEQ's comprehensive and interactive Quality program is designed to exceed military and customer expectations and requirements.

SEEQ's Quality program complies with military standards including MIL-Q-9858, MIL-I-45208, MIL-M-38510 Appendix A, MIL-STD-45662, FED-STD-209 and MIL-STD-883. Key segments of the Quality program are described below.

### **Quality Assurance**

SEEQ's Quality Assurance activity audits and monitors the operating system and reports compliance to processing requirements. Included within the activity is inspection of incoming material and outgoing product, audits and process monitors of Fab, Assembly and Test. Product improvement and corrective action is based on statistical data reduction and analysis.

### **Quality Control**

SEEQ's Quality Control activity is an in-line inspection, reporting and statistical control system. Included is product inspection, and disposition of material and processes which do not conform to specification.

### **Quality Engineering**

Quality engineering supports incoming, Fab, assembly, test, customer returns, and failure analysis through the use of statistics and analytical capabilities. Quality Engineering supplies focus, coordination and integration for quality improvement and system optimization, throughout the entire business entity of SEEQ.

### **Product Monitor Program**

SEEQ's Product Monitor Program merges the classical reliability Quality Conformance Inspection (QCI, Groups B, C, and D) and Device Qualification Activities into one comprehensive product data base. Results are published quarterly.

### **Document Control**

Document Control generates, implements and maintains procedures that will ensure control of all documents related to the design, production and testing of manufactured products, including the translation of customer specification requirements into SEEQ internal travelers, specifications and procedures.

SEEQ's Document Control program assures internal specifications and procedures are maintained to the correct revision levels (Engineering Change Notice Control) and provides historical records of all changes.

### **Reliability Engineering**

Reliability (quality over time) is built into each SEEQ device, using proven engineering techniques. Process and product performance is demonstrated using accelerated stresses and tests. Results are jointly analyzed with design and sustaining engineering; then any improvements are incorporated into manufacturing.

### **Device Physics**

The Device Physics groups help characterize the design and process, particularly in regard to quality and reliability. Potential failure mechanisms are analyzed for impact on processing and design. Overall product performance is enhanced by development of test, screens, process or design changes as necessary.

# Military Product Processing Program

SEEQ's Military product flow (Chart 1) incorporates manufacturing processing, screening and controls. Controls as specified in Military procedures or customer specifications are an integral part of the processing flows in wafer fabrication, assembly product screening and test. (Table 1)

## Quality Conformance Inspection

### Group A Tests

Group A — lot acceptance tests (see Table 1) are performed on each of SEEQ's production lots or sub-lots (splits) after completion of all processing. Q.A. electrical and mechanical inspection is performed using a sample of 116, accept on 0.

### Group B — Tests (see Table 2)

Group B testing is performed by product and package type. The Group B covers the lot's sub lot, seal date code and the next consecutive five (5\*) weeks of seal. The date code marked on the product is the week of seal.

### Group C Stresses — (see Table 3)

The product stressed, as part of Group C, is identical to that shipped or from the same process and product family. The seal date code of the product covered will be the same as or within the 51\* consecutive weeks following the Group C seal date code. Electrical test is per SEEQ data sheet.

### Group D Stresses — (see Table 4)

The package stressed, as part of Group D, is identical to that shipped. The seal date code of product covered will be the same as or within the 51\* weeks following the Group D date code.

## Product Monitors

### On-Going

Process control monitor samples of product are subjected to marking permanency, endurance, pressure pot and hermeticity. These tests are performed and reported by the Quality Assurance activity. Monitor tests and procedures are in accordance with applicable MIL-STD-883 test methods.

\*Frequency is stated for Military processed lots. Some group B, C, D stresses and tests for commercial products are performed more frequently.

## Extended Product Monitors

As part of SEEQ's product reliability data program samples of released military product are subjected to extended stresses. The extended stress are summarized as follows:

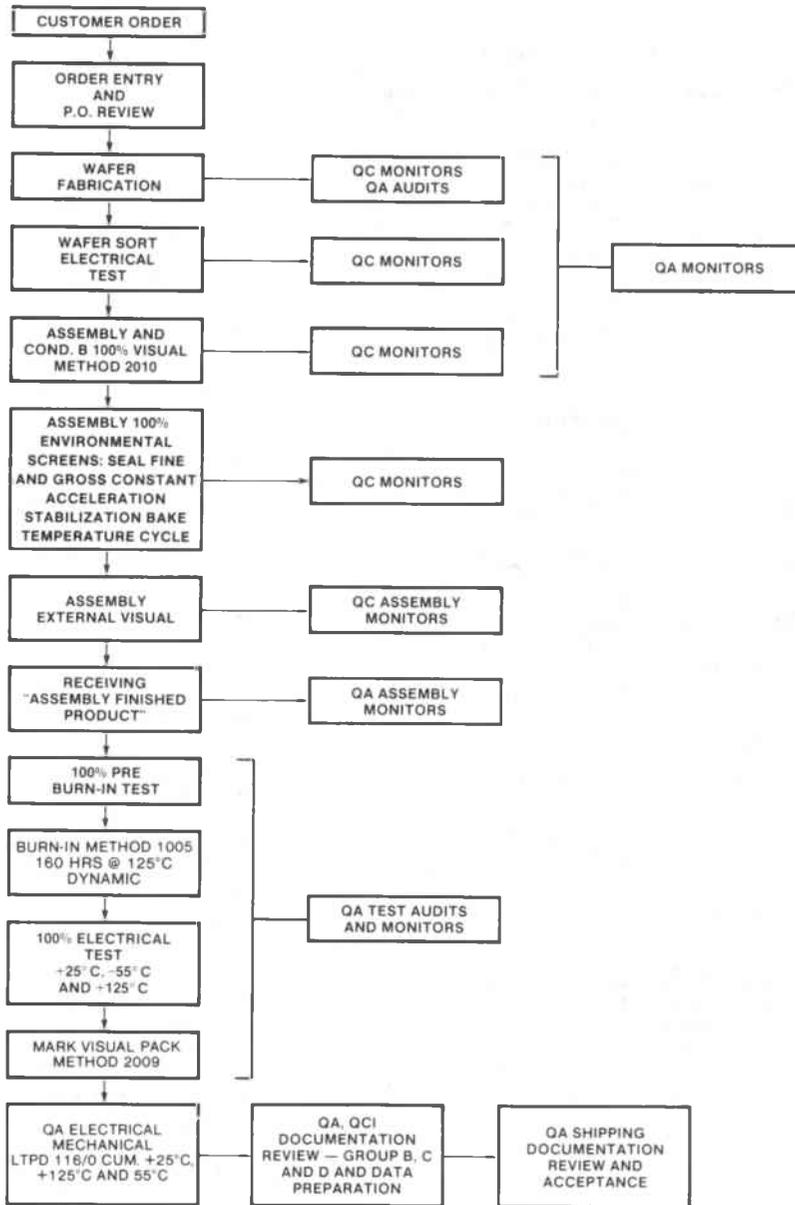
<u>Stress</u>	<u>Stress</u>	
	<u>Frequency</u>	<u>Duration</u>
Dynamic Life Stress	Annually	10,000 Hours
Endurance (E <sup>2</sup> ROM)	Quarterly	1,000,000 Cycles
Endurance (EPROM)	Quarterly	50 Cycles
Temperature Cycle	Quarterly	1,000 Cycles
Data Retention	Quarterly	1,000 Hours
Static Life Stress	Quarterly	1,000 Hours

## Product Monitor

### Quality Conformance Inspection Data

SEEQ updates quarterly all product monitor data and can supply summary data upon request. Generic data is defined for Group B, C, and D tests as well as other tests SEEQ deems necessary. Electrical end-point testing is per SEEQ data sheet using SEEQ standard test programs and equipment. Dynamic life stress (burn-in) is performed in compliance with MIL-STD-883, MIL-STD-883, Method 1015.

# Product Processing Flow (Chart 1)



MILITARY

**SEEQ Screens, Tests, & Monitors (Table 1)**

<b>Military Screen</b>	<b>MIL-STD Method</b>	<b>Reqmt.</b>
Internal Visual	2010, Test Condition B	100%
Stabilization Bake	1008, 24 Hrs @ Condition C	100%
Temperature Cycling	1010, Test Condition C	100%
Constant Acceleration	2001, Test Condition D, Y <sub>1</sub> Orientation Only	100%
Seal (A) Fine (B) Gross	1014 Condition A or B Condition C or D	100%
Visual Inspection		100%
Initial (Pre-Burn-In-Test) Electrical Parameters	Per Applicable SEEQ Specification	100%
Burn-In Stress	1015, Dynamic @ 125°C	100%
(Post-Burn-In—Test) Electrical Parameters Tested within 96 Hrs.	Per Applicable SEEQ Specification	100%
Percent Defective Allowable (PDA) Calculation	5% Cumulative	100%
Quality Assurance Group A Tests  (A) Static Tests  (B) Dynamic Tests and Switching Tests  (C) Functional Tests	Per Applicable SEEQ Specification  Cumulative across temperature (-55, 25, 125°C)	LTPD 116/0
Qualification or Quality Conformance Inspection Test Sample Selection		
External Visual	2009	100%

**SEEQ Quality Monitors**

**Wafer Fab**

- Monitors and Audits:
- Phosphorous Content
  - Spec. and ECN Control
  - Defect Density
  - Defect Inspection
  - Critical Dimensions
  - Oxide Thickness
  - On-Going Mask
  - SEM (Step Coverage)

**Assembly Processing**

- Monitors:
- 2nd Optical LTPD 10/1, Method 2010 Cond B
  - Die Shear (2 Units/4 Hours)
  - Bond Strength (2 Units/4 Hours)
  - 3rd Optical — LTPD 10/1, Method 2010 Cond B

**Assembly Environmentals**

- Monitors:
- Tin Plating Thickness
  - Solderability
  - Visual
  - Equipment Monitors
  - Fine and Gross Leak LTPD 10/1

**Assembly Receiving**

- Monitors:
- Internal Visual
  - Bond Strength
  - Die Shear
  - Lid Torque
  - Lead Fatigue

**Test and Finish**

- Monitors:
- PDA Verification
  - 96 Hour Test Time Window
  - Conformance Audits
  - Solderability
  - Fine Leak/Gross Leak
  - Marking Permanence

**Quality Conformance Inspection (QCI)**

- Monitors:
- Group B (Table 2)
  - Group C (Table 3)
  - Group D (Table 4)

**Group B Tests (Table 2)**

Test	Test Method	Test Conditions	Quality Level/ Accept Number
<b>Subgroup 1</b> Physical Dimensions	2016	Per SEEQ Outline Drawing	2 Devices (no failures)
<b>Subgroup 2</b> Resistance to Solvents	2015		4 Devices (no failures)
<b>Subgroup 3</b> Solderability	2003	Soldering Temperature of +245° C Plus or Minus 5° C	LTPD 15 Accept = 1
<b>Subgroup 4</b> Internal Visual and Mechanical	2014	Failure Criteria Based on Design and Construction Requirements of SEEQ Specification	1 Device (no failures)
<b>Subgroup 5</b> Bond Strength Ultrasonic or Wedge	2011	Test Condition C or D	LTPD 15 Accept = 1
<b>Subgroup 7</b> (A) Seal (1) Fine (2) Gross	1014	As Applicable	LTPD 5 Accept = 0

**Group C Stresses (Table 3)**

Test	Test Method	Test Conditions	Quality Level/ Accept Number
<b>Subgroup 1</b> Steady-State Life Test End-Point Electrical	1005	Condition B. 1000 Hours Per SEEQ Specification	LTPD 5 Accept = 1
<b>Subgroup 2</b> Temperature Cycling Constant Acceleration Hermeticity Fine Gross Visual Examination End-Point Electrical Parameters	1010 2001 1014	Condition C. 10 Cycles Y <sub>1</sub> Orientation 20,000 (g) As Applicable  Per SEEQ Specification	LTPD 15 Accept = 1

**Group D Stresses (Table 4)**

Test	MIL-STD Test Method	Test Conditions	Minimum Quality Level/ Accept Number
<b>Subgroup 1</b> Physical Dimensions	2016	Per SEEQ Outline Drawing	LTPD 15 Accept = 1
<b>Subgroup 2</b> Lead Integrity Hermeticity, Fine and Gross	2004 1014	Test Condition B2	LTPD 15 Accept = 1
<b>Subgroup 3</b> Thermal Shock Temperature Cycling  Moisture Resistance Hermeticity, Fine and Gross Visual Examination End-Point Electrical Parameters	1011 1010  1004 1014 1004 1010	T = -55° C to +125° C, 15 Cycles Minimum T = -55° C to +125° C, 100 Cycles Minimum 90% Minimum Relative Humidity Per SEEQ or Customer Specification Per SEEQ or Customer Specification	LTPD 15 Accept = 1
<b>Subgroup 4</b> Mechanical Shock Vibration, Variable Frequency Constant Acceleration Hermeticity, Fine and Gross Visual Examination End-Point Electrical Parameters	2002 2007 2001 1014 2009	1500 (g) 20 (g) Y <sub>1</sub> Orientation 20,000 (g) Per SEEQ or Customer Specification Per SEEQ or Customer Specification	LTPD 15 Accept = 1
<b>Subgroup 5</b> Salt Atmosphere Hermeticity, Fine and Gross Visual Examination	1009 1014 1009	24 Hours Per SEEQ or Customer Specification	LTPD 15 Accept = 1
<b>Subgroup 6</b> Internal Wafer Vapor	1018	5 000 ppm Maximum Water Content at T = +100° C	3 Devices, 0 Failures or 5 Devices, 1 Failure
<b>Subgroup 7</b> Adhesion of Lead Finish	2025	Bend 90° Inspect at 10x to 20x Magnification	LTPD 15 Accept = 1
<b>Subgroup 8</b> Lid Torque	2024	As Applicable to Glass-Frit Packages	LTPD 15 Accept = 1

# 16K Electrically Erasable PROM

October 1987

### Features

- **Full Military and Extended Temperature Range**
  - M52B13/M52B13H:  $-55^{\circ}$  to  $125^{\circ}\text{C}$
  - E52B13/E52B13H:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- **Input Latches**
- **5V  $\pm$  10% 2K X 8 EEPROM**
- **1 ms (52B13H) or 9 ms Byte TTL Erase/Byte Write**
- **10,000 Erase/Write Cycles per Byte Minimum**
- **Chip Erase and Byte Erase**
- **DITrace™**
- **Fast Read Access Time — 250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte Wide Memory Pinout**
- **M2816 E<sup>2</sup> Compatible**

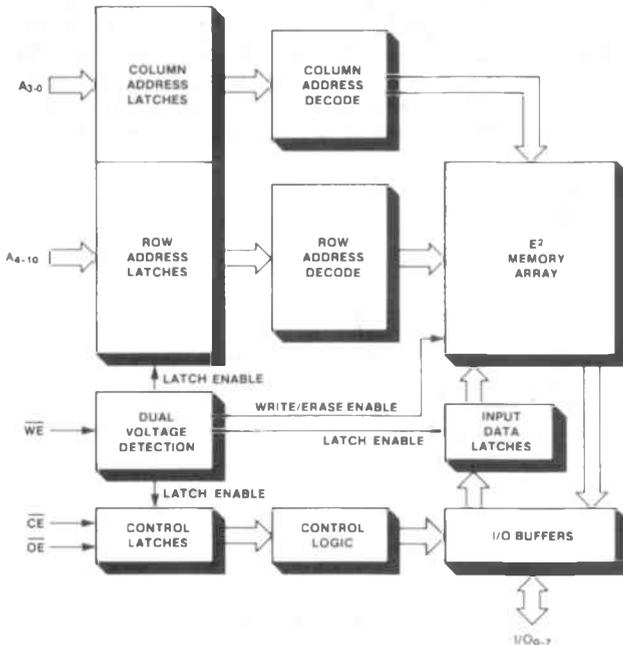
### Description

SEEQ's M52B13 and E52B13 are 2048 x 8 bit, 5 volt electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 msec), an M52B13H and E52B13H are also available. Data is latched and electrically written by a TTL (or a 21V pulse) on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

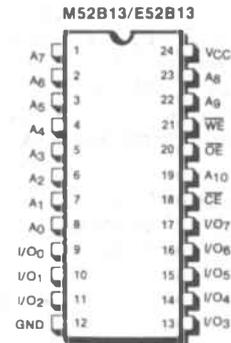
The M52B13 is compatible to the M2816 and SEEQ's M5213. For system upgrades of these older generation EEPROMs, the M52B13 is specified over the full  $-55^{\circ}$  to  $+125^{\circ}\text{C}$  temperature range and has an access time of 250 ns. The M52B13 is available in a 24 pin cerdip package.

(continued on next page)

### Block Diagram



### Pin Configuration



### Pin Names

A <sub>0</sub> -A <sub>10</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

# M52B13/M52B13H E52B13/E52B13H

These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instruments/machines, programmable industrial controllers, and an assortment of other systems. Designing the EEPROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

## Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1's) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation EEPROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detec-

tion circuit which allows either a TTL low or 21V signal to be applied to WE to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of WE.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycles is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to WE, enabling the chip, and enabling the outputs. Data is available,  $t_{CE}$  time after Chip Enable is applied or  $t_{AA}$  time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

## DiTrace™

SEEQ's family of EEPROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to the wafer level in an extra column of EEPROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection ( $V_{CC} = 5V \pm 10\%$ )

Mode \ PIN	CE (18)	OE (20)	WE (21)	I/O (9-11, 13-17)
Read <sup>1</sup>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby <sup>1</sup>	V <sub>IH</sub>	Don't Care	V <sub>IH</sub>	High Z
Byte Erase <sup>2</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub> = V <sub>IH</sub>
Byte Write <sup>2</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Chip Erase <sup>2</sup>	V <sub>IL</sub>	VOE	V <sub>IL</sub>	D <sub>IN</sub> = V <sub>IH</sub>
Write/Erase Inhibit	V <sub>IH</sub>	Don't Care	Don't Care	High Z

### NOTES:

1 WE may be from V<sub>IH</sub> to 6V in the read and standby mode.

2 We may be at V<sub>IL</sub> (TTL WE Mode) or from 15 to 21V (High Voltage WE Mode) in the byte erase, byte write, or chip erase mode of the 52B13/52B13H.

**MILITARY**

**Power Up/Down Considerations**

SEEQ's "52B" E<sup>2</sup> family has internal circuitry to minimize false erase or write during system V<sub>CC</sub> power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

1. V<sub>CC</sub> is less than 3 V.<sup>1)</sup>
2. A negative Write Enable transition has not occurred when V<sub>CC</sub> is between 3 V and 5 V.

Under the above conditions, the outputs are in a high impedance state.

**Absolute Maximum Stress Ratings\***

<i>Temperature</i>	
Storage .....	-65°C to +150°C
Under Bias .....	-65°C to +135°C
<i>All inputs or Outputs with</i>	
Respect to Ground .....	+6V to -0.3V
<i>WE during Writing/Erasing</i>	
with Respect to Ground .....	+22.5 to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range:	
M52B13/ M52B13H (Case)	-55° to +125°C
E52B13/ E52B13H (Ambient)	-40° to +85°C

**NOTE:**

1. Characterized. Not tested.

# M52B13/M52B13H E52B13/E52B13H

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

## D.C. Operating Characteristics During Read or Write/Erase (Over operating V<sub>CC</sub> and temperature range.)

Symbol	Parameter	Min.	Nom.	Max.	Unit	Test Conditions
I <sub>IN</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>O</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
I <sub>WE</sub>	Write Enable Leakage Read Mode			10	μA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	μA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode			1.5	mA	$\overline{WE} = 22V, CE = V_{IL}$
	High Voltage W/E Inhibit Mode			1.5	mA	$\overline{WE} = 22V, CE = V_{IH}$
	Chip Erase — TTL Mode			10	μA	$\overline{WE} = V_{IL}$
	Chip Erase—High Voltage Mode			1.5	mA	$\overline{WE} = 22V$
I <sub>CC1</sub>	V <sub>CC</sub> Standby Current		15	35	mA	CE = V <sub>IH</sub>
I <sub>CC2</sub>	V <sub>CC</sub> Active Current		50	90	mA	CE = $\overline{OE} = V_{IL}$
V <sub>IL</sub>	Input Low Voltage	-0.1		0.8	V	
V <sub>IH</sub>	Input High Voltage	2		V <sub>CC</sub> + 1	V	
V <sub>WE</sub>	$\overline{WE}$ Read Voltage	2		V <sub>CC</sub> + 1	V	
	$\overline{WE}$ Write/Erase Voltage TTL Mode	-0.1		0.8	V	
	High Voltage Mode	14		22	V	
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA
V <sub>OE</sub>	$\overline{OE}$ Chip Erase Voltage	14		22	V	I <sub>OE</sub> = 10 μA

**NOTE:**

1. Nominal values are for T<sub>A</sub> = 25°C and V<sub>CC</sub> = 5.0 V

# M52B13/M52B13H E52B13/E52B13H

## A.C. Operating Characteristics During Read

Symbol	Parameter	Device Number Extension	M52B13/ M52B13H		E52B13/ E52B13H		Units	Test Conditions
			Min.	Max.	Min.	Max.		
$t_{AA}$	Address Access Time	-250 -300 -350		250 300 —		250 — 350	ns ns ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid	-250 -300 -350		250 300 —		250 — 350	ns ns ns	$\overline{OE} = V_{IL}$
$t_{OE}^{[1]}$	Output Enable to Data Valid	-250 -300 -350		90 90 —		90 — 110	ns ns ns	$\overline{CE} = V_{IL}$
$t_{DF}^{[2]}$	Output Enable to High Impedance	-250 -300 -350	0 0 —	70 70 —	0 — 0	70 — 80	ns ns ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$C_{IN}/C_{OUT}^{[3]}$	Input Capacitance	All		10		10	pF	$V_{IN} = 0 V$ for $C_{IN}$ , $V_{OUT} = 0 V$ for $C_{OUT}$ , $T_A = 25^\circ C$
	Output Capacitance	All		10		10	pF	

### Equivalent A.C. Test Conditions<sup>[6]</sup>

Output Load: 1 TTL gate and  $C_L = 100$  pF

Input Rise and Fall Times:  $\leq 20$  ns

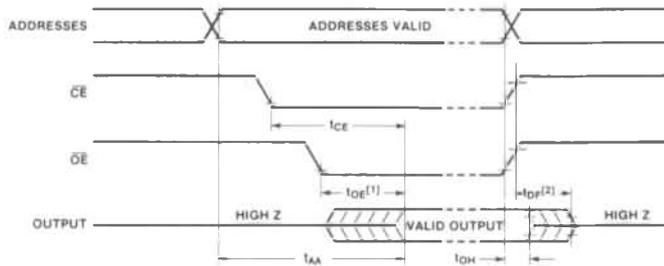
Input Pulse Levels: 0.45V to 2.4V

Timing Measurement Reference Level:

Inputs 1V and 2V

Outputs 0.8V and 2V

## READ TIMING



### NOTES:

1.  $\overline{OE}$  may be delayed to  $t_{AA} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{AA}$ .
2.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
3. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
4. After  $t_{WH}$  hold time, from  $\overline{WE}$ , the inputs  $\overline{CE}$ ,  $\overline{OE}$ , Address and Data are latched and are "Don't Care" until  $t_{WR}$ , Write Recovery Time, after the trailing edge of  $\overline{WE}$ .
5. The Write Recovery Time,  $t_{WR}$ , is the time after the trailing edge of  $\overline{WE}$  that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
6. These are equivalent test conditions and actual test conditions are dependent on the tester.

# M52B13/M52B13H E52B13/E52B13H

## A.C. Operating Characteristics During Write/Erase (Over the operating V<sub>CC</sub> and temperature range)

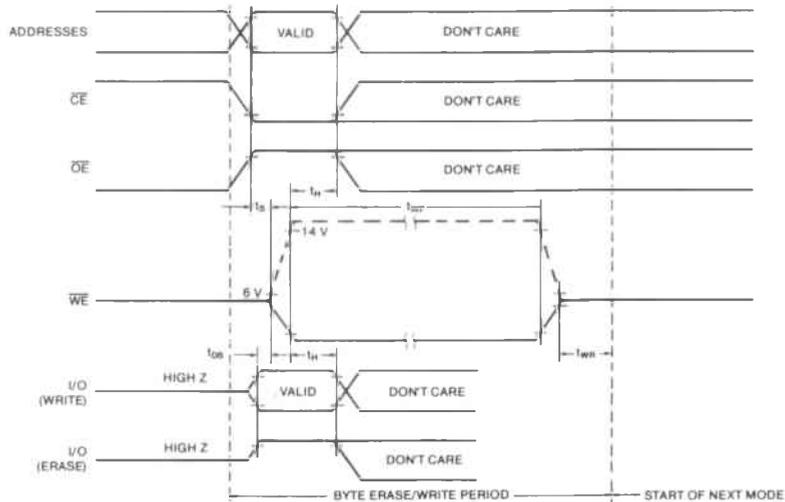
Symbol	Parameter	Min.	Max.	Units
t <sub>S</sub>	CE, OE or Address Setup to WE	50		ns
t <sub>DS</sub>	Data Setup to WE	15		ns
t <sub>H</sub> <sup>4</sup>	WE to CE, OE, Address or Data Change	50		ns
t <sub>WP</sub>	Write Enable WE Pulse Width Byte Modes — M52B13/E52B13	9		ms
	Byte Modes — M52B13H/E52B13H	1		
t <sub>WR</sub> <sup>5</sup>	WE to Mode change WE to Start of Next Byte Write Cycle	50		ns
	WE to Start of Read Cycle		2	μs

## 52B13/52B13H High Voltage Write Specifications

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications, including the TTL W/E mode.

Symbol	Function/Parameter	M52B13 E52B13		M52B13H E52B13H		Units
		Min.	Max.	Min.	Max.	
t <sub>WP</sub>	Write Enable Pulse Width Byte Write/Erase	9	20	1	20	ms
	Chip Erase	9	20	9	20	ms
V <sub>WE</sub>	WE Write/Erase Voltage High Voltage Mode	14	22	14	22	V

### BYTE ERASE OR BYTE WRITE TIMING



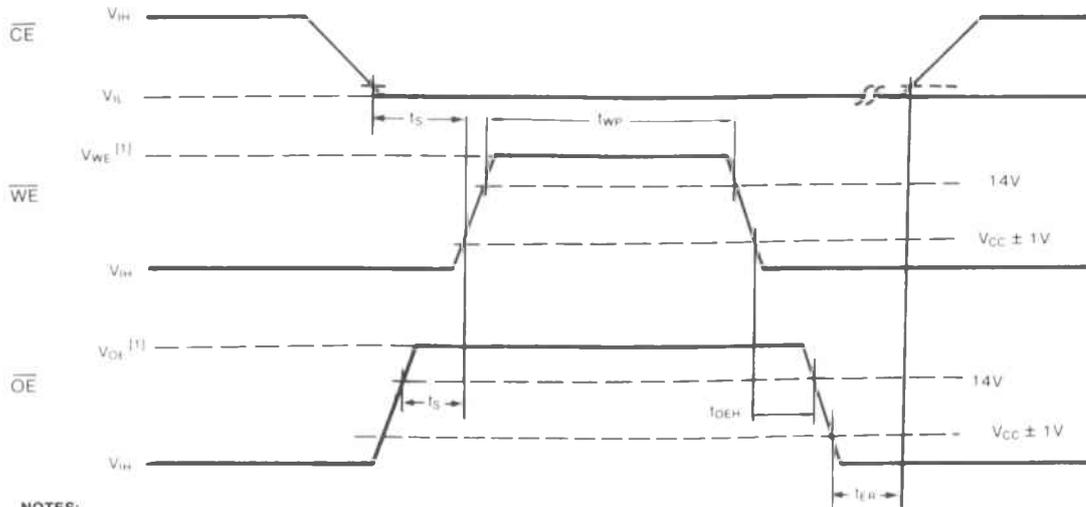
Notes: See AC notes

# M52B13/M52B13H E52B13/E52B13H

## Chip Erase Specifications

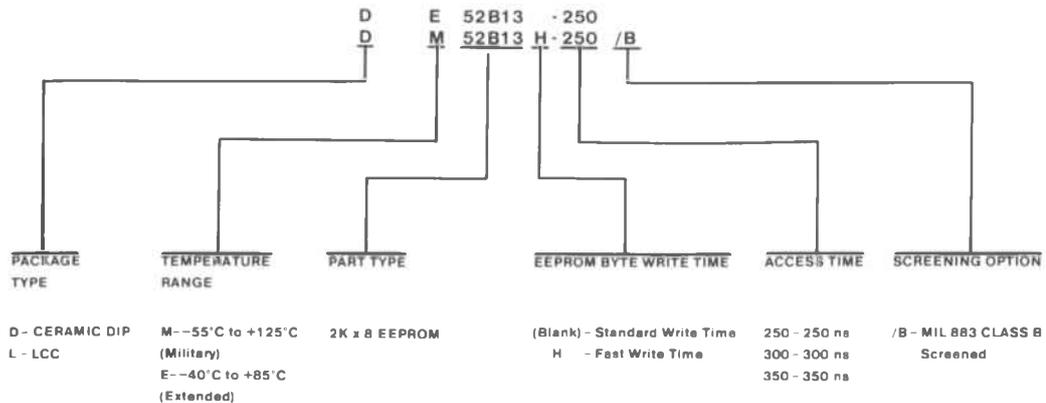
Symbol	Parameter	Min.	Max.	Units
$t_s$	$\overline{CE}$ , $\overline{OE}$ Setup to $\overline{WE}$	1		$\mu\text{s}$
$t_{OEH}$	$\overline{OE}$ Hold Time	1		$\mu\text{s}$
$t_{WP}$	$\overline{WE}$ Pulse Width	10		ms
$t_{ER}$	Erase Recovery Time		10	$\mu\text{s}$

## Chip Erase Timing



NOTES:  
1.  $V_{WE}$  and  $V_{OE}$  can be from 15V to 21V in the high voltage mode for chip erase on 52B13.

## Ordering Information



MILITARY



### 64K Electrically Erasable PROM

October 1987

#### Features

- **Full Military and Extended Temperature Range**
  - M52B33/M52B33H:  $-55^{\circ}$  to  $125^{\circ}\text{C}$
  - E52B33/E52B33H:  $-40^{\circ}$  to  $85^{\circ}\text{C}$
- **10,000 Write Cycles/Byte Over Temperature**
- **Input Latches**
- **$5\text{ V} \pm 10\% V_{CC}$**
- **1 ms (52B33H) or 9 ms (52B33) TTL Byte Erase/Byte Write**
- **Power Up/Down Protection**
- **DiTrace™**
- **Fast Read Access Time—250 ns**
- **Infinite Number of Read Cycles**
- **JEDEC Approved Byte-Wide Memory Pinout**

#### Description

SEEQ's M52B33 and E52B33 are 8192 x 8, 5V electrically erasable programmable read only memories (EEPROMs) which are specified over the military and extended temperature range respectively. They have

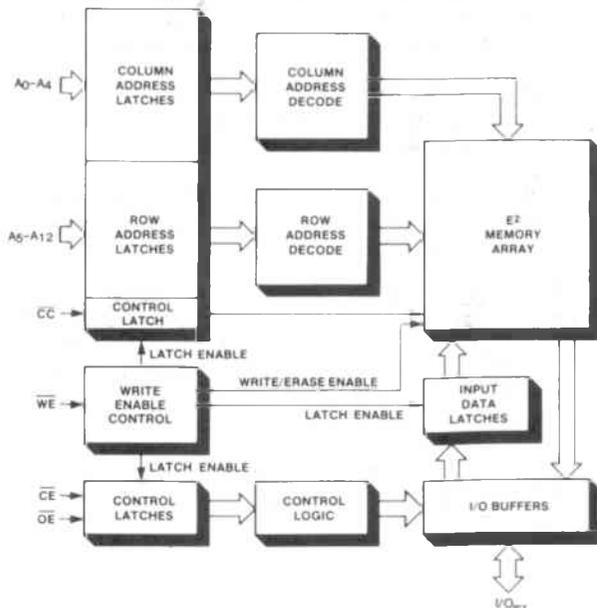
input latches on all addresses, data, and control (chip and output) lines. In addition, for applications requiring fast byte write time (1 ms), an E52B33H and M52B33H are available. Data is latched and electrically written by a TTL pulse on the Write Enable pin. Once written, there is no limit to the number of times data may be read. The erasure time is under 10 ms, and each byte may be erased and written a minimum of 10,000 times.

The E/M52B33 is available in a 28 pin cerdip or 32 pin leadless chip carrier. The pin configuration is to the JEDEC approved byte wide memory pinout for these two types of packages. These EEPROMs are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic configuration (the alteration of opening software in real-time) is made possible by this device. Applications will be found in military avionics systems, programmable character generators, self-calibrating instrument/machines, programmable industrial controllers, and an assortment of other

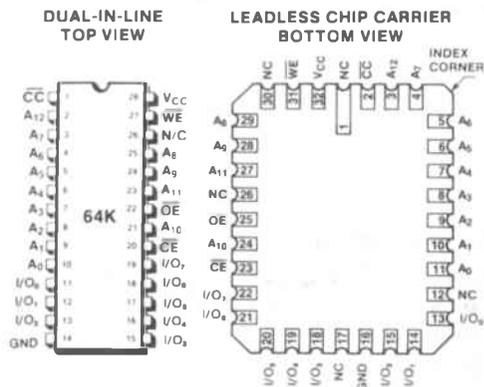
(continued on page 2)

MILITARY

#### Block Diagram



#### Pin Configurations



#### Pin Names

A <sub>0</sub> -A <sub>4</sub>	ADDRESSES - COLUMN (LOWER ORDER BITS)
A <sub>5</sub> -A <sub>12</sub>	ADDRESSES - ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>n</sub>	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
CC	CHIP CLEAR
N/C	NO CONNECT

# M52B33/M52B33H E52B33/E52B33H

systems. Designing the EEPROMs into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance.

## Device Operation

SEEQ E/M52B33 and E/M52B33H have six modes of operation (see Table 1) and require only TTL inputs to operate these modes.

To write into a particular location, that byte must first be erased. A memory location is erased by having valid addresses, Chip Enable at a TTL low, Output Enable at TTL high, and TTL highs (logical 1's) presented to all the I/O lines. Write Enable is then brought to a TTL low level to latch all the inputs. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B33H performs the same as the E/M52B33 except that the byte erase/byte write time has been enhanced to 1 ms.

A characteristic of all EEPROMs is that the total number of write and erase cycles is not unlimited. The E/M52B33 is designed for applications requiring up to 10,000 write and erase cycles per byte over the temperature range. The write and erase cycling characteristics are completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to  $\overline{WE}$ , enabling the chip, and enabling the outputs. Data is available,  $t_{CE}$  time after Chip Enable is applied or  $t_{AA}$  time from the addresses. System power may be reduced by placing the device into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

## DiTrace™

SEEQ's family of EEPROMs incorporates a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information in an extra row of EEPROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

## Chip Clear

Certain applications may require all bytes to be erased simultaneously. See A.C. Operating Characteristics for TTL chip erase timing specifications.

## Power Up/Down Considerations

SEEQ's "52B" E<sup>2</sup> family has internal circuitry to minimize false erase or write during system  $V_{CC}$  power up or down. This circuitry prevents writing or erasing under any one of the following conditions.

1.  $V_{CC}$  is less than 3 V.<sup>[1]</sup>
2. A negative Write Enable transition has not occurred when  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the Mode Selection table.

## Mode Selection (Table 1)

Mode \ Function (Pin)	$\overline{CE}$ (20)	$\overline{CC}$ (1)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13, 15-19)
Read	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IH}$	DOUT
Standby	$V_{IH}$	Don't Care	Don't Care	Don't Care	High Z
Byte Erase	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	$D_{IN} = V_{IH}$
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IH}$	$V_{IL}$	$D_{IN}$
Chip Clear	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_{IL}$ or $V_{IH}$
Write/Erase Inhibit	$V_{IH}$	Don't Care	Don't Care	Don't Care	High Z

### NOTE:

1. Characterized. Not tested.

# M52B33/M52B33H E52B33/E52B33H

## Absolute Maximum Stress Rating\*

### Temperature

Storage .....	-65°C to +150°C
Under Bias .....	-65°C to +135°C
All inputs or Outputs with Respect to Ground .....	+6V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

## Recommended Operating Conditions

V <sub>CC</sub> Supply Voltage	5 V ± 10%
Temperature Range: M52B33/M52B33H (Case)	-55° to + 125°C
E52B33/E52B33H (Ambient)	-40° to + 85°C

## DC Operating Characteristics During Read or Erase/Write

(Over the operating V<sub>CC</sub> and temperature range)

Symbol	Parameter	Min.	Nom. <sup>[1]</sup>	Max.	Unit	Test Condition
I <sub>IN</sub>	Input Leakage Current			10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max
I <sub>O</sub>	Output Leakage Current			10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max
I <sub>WE</sub>	Write Enable Leakage Read Mode W/E Mode			10 10	μA μA	$\overline{WE} = V_{IH}$ $\overline{WE} = V_{IL}$
I <sub>CC1</sub>	V <sub>CC</sub> Standby Current		15	50	mA	$\overline{CE} = V_{IH}$
I <sub>CC2</sub>	V <sub>CC</sub> Active Current		50	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V <sub>IL</sub>	Input Low Voltage	-0.1		0.8	V	
V <sub>IH</sub>	Input High Voltage	2		V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage			0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4			V	I <sub>OH</sub> = -400 μA

NOTE: See next page for notes

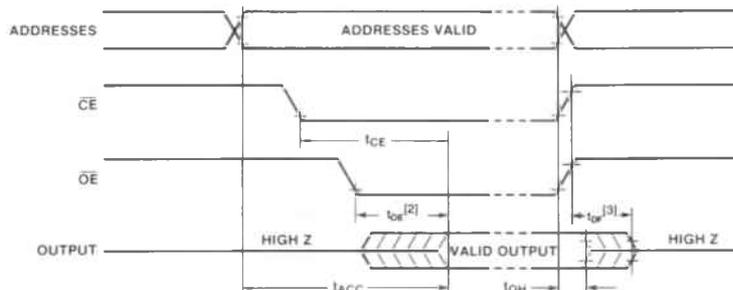
# M52B33/M52B33H E52B33/E52B33H

## A.C. Operating Characteristics During Read

(Over the operating  $V_{CC}$  and temperature range)

Symbol	Parameter	Device Number Extension	M52B33 M52B33H		E52833 E52833H		Unit	Test Conditions
			Min.	Max.	Min.	Max.		
$t_{AA}$	Address Access Time	-250 -300		250 300		250 300	ns ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid	-250 -300		250 300		250 300	ns ns	$\overline{OE} = V_{IL}$
$t_{OE}^{[2]}$	Output Enable to Data Valid	-250 -300		90 90		90 90	ns ns	$\overline{CE} = V_{IL}$
$t_{DF}^{[3]}$	Output Enable to High Impedance	-250 -300	0 0	70 70	0 0	70 70	ns ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold	All	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$C_{IN}/C_{OUT}^{[4]}$	Input/Output Capacitance	All		10		10	pF	$V_{IN} = 0\text{ V}$ for $C_{IN}$ , $V_{OUT} = 0\text{ V}$ for $C_{OUT}$ , $T_A = 25^\circ\text{ C}$

## Read Cycle Timing



### NOTES:

1. Nominal values are for  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 5.0\text{ V}$
2.  $\overline{OE}$  may be delayed to  $t_{AA} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{AA}$ .
3.  $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.
4. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
5. After  $t_H$ , hold time, from  $\overline{WE}$ , the inputs  $\overline{CE}$ ,  $\overline{OE}$ ,  $\overline{CC}$ , Address and Data are latched and are "Don't Cares" until  $t_{WR}$ , Write Recovery Time, after the trailing edge of  $\overline{WE}$ .
6. The Write Recovery Time,  $t_{WR}$ , is the time after the trailing edge of  $\overline{WE}$  that the latches are open and able to accept the next mode set-up conditions. Reference Table 1 (page 2) for mode control conditions.
7. These are equivalent test conditions and actual test conditions are dependent on the tester.

# M52B33/M52B33H E52B33/E52B33H

## A.C. Operating Characteristics During Write/Erase

(Over the operating Vcc and temperature range)

Symbol	Parameter	Limits		Units
		Min.	Max.	
t <sub>S</sub>	CE, OE or Address Setup to WE	50		ns
t <sub>DS</sub>	Data Setup to WE	15		ns
t <sub>H</sub> <sup>[6]</sup>	WE to CE, OE, Address or Data Change	50		ns
t <sub>WP</sub>	Write Enable, (WE) Pulse Width			
	Byte Modes — M52B33/E52B33	9		ms
	Byte Modes — M52B33H	1		ms
t <sub>WR</sub> <sup>[6]</sup>	WE to Mode Change			
	WE to Next Byte Write/Erase Cycle	50		ns
	WE to Start of a Read Cycle	1		μs

## Equivalent A.C. Test Conditions<sup>[7]</sup>

Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF

Input Rise and Fall Times: ≤ 20 ns

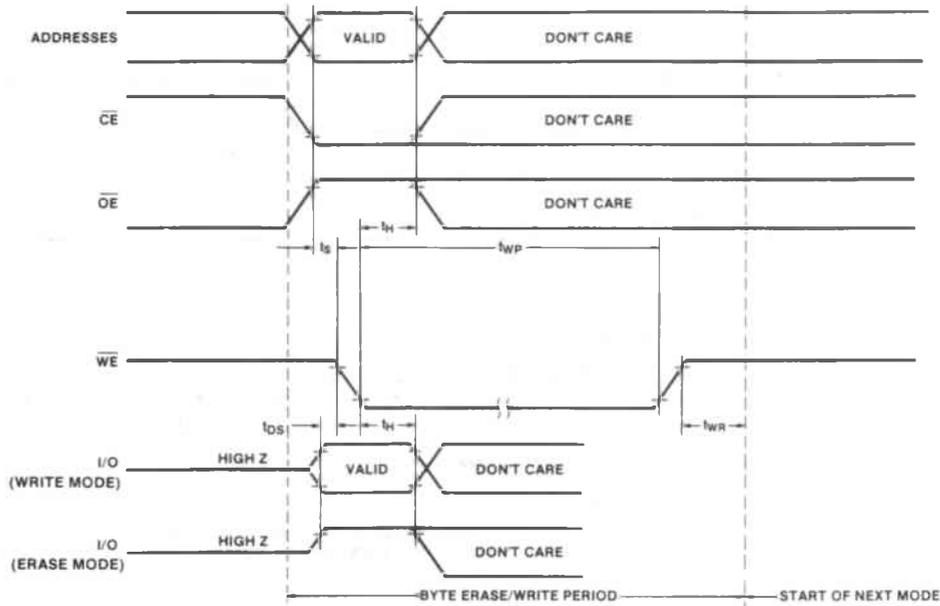
Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## Byte Erase or Byte Write Cycle Timing



### NOTES:

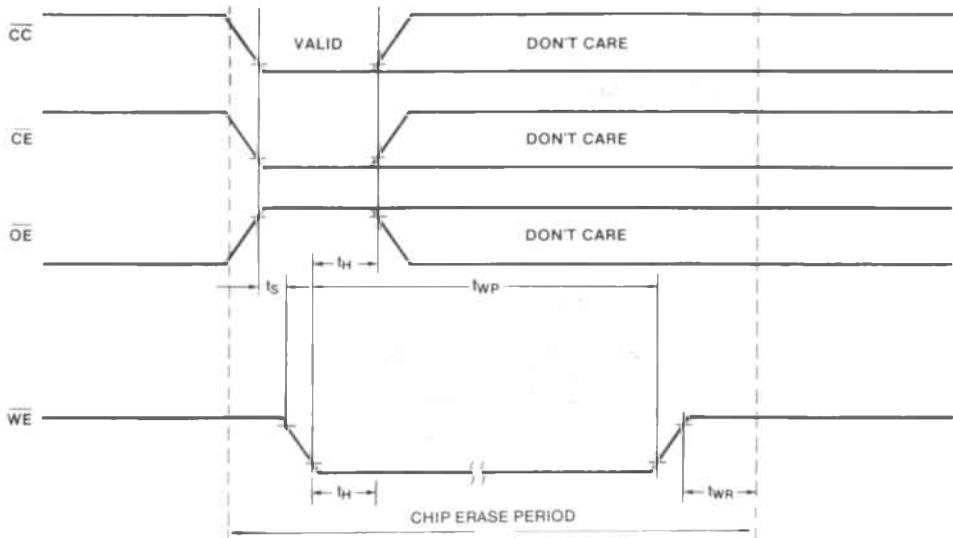
See previous page for notes.

# M52B33/M52B33H E52B33/E52B33H

## A.C. Operating Characteristics During Chip/Erase (Over the operating $V_{CC}$ and temperature range)

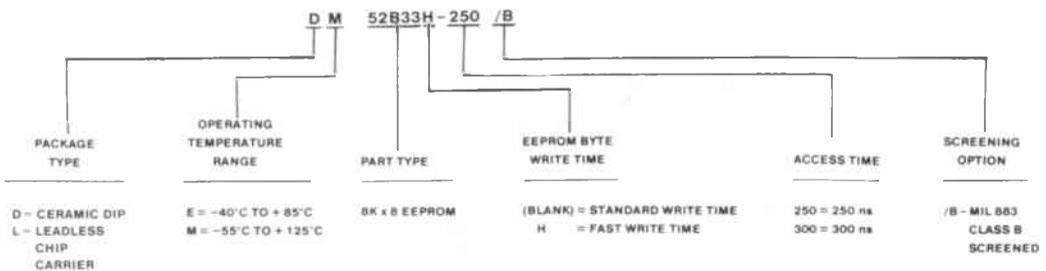
Symbol	Parameter	Min.	Max.	Units
$t_s$	CC, CE OE Setup to WE	50		ns
$t_H^{[4]}$	WE to CE, OE, CC change	50		ns
$t_{WP}$	Write Enable (WE) Pulse Width Chip Erase — M52B33/M52B33H Chip Erase — E52B33/E52B33H	10		ms
$t_{WR}^{[5]}$	WE to Mode change	50		ns
	WE to Start of Next Byte Write Cycle		1	$\mu$ s
	WE to Start of Read Cycle			

### TTL Chip Erase Timing



**NOTE:** Address, Data are don't care during Chip Erase.

### Ordering Information



### Features

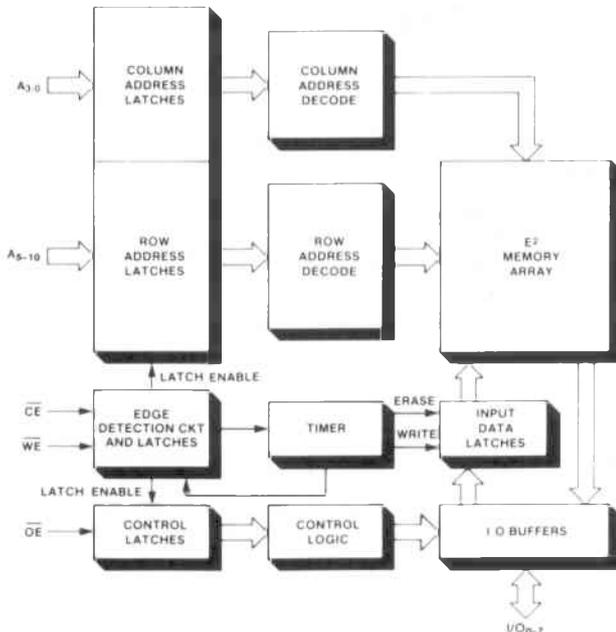
- **High Endurance Write Cycles**  
— 2816A: 10,000 Cycles/Byte Minimum
- **On-Chip Timer**  
— Automatic Erase and Write Time Out
- **All Inputs Latched by Write or Chip Enable**
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**  
— 110 mA max. Active Current  
— 40 mA max. Standby Current
- **JEDEC Approved Byte-Wide Pinout**
- **Military and Extended Temperature Range**  
— -55°C to +125°C: M2816A (Military)  
— -40°C to +85°C: E2816A (Extended)

### Description

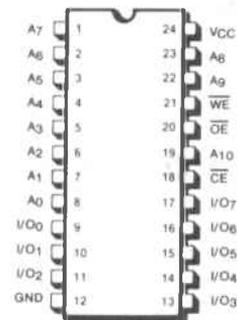
SEEQ's E/M2816A are 5V only, 2K x 8 electrically erasable programmable read only memories (EEPROM). EEPROMs are ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times that a byte may be written, is 10 thousand for the E/M2816A. The E/M2816A's high endurance was accomplished using SEEQ's proprietary oxyntride EEPROM process and its innovative "Q cell"™ design. The E/M2816A is ideal for systems that require frequent updates.

There is an internal timer that automatically times out the write time. A separate erase cycle is not required and the minimum write enable (WE) pulse width needs to be only 150 ns. The on-chip timer, along with the inputs being latched by a write or chip enable signal edge, frees the microcomputer system (continued on next page)

### Block Diagram



### Pin Configuration



### Pin Names

A <sub>0</sub> -A <sub>10</sub>	ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

for other tasks during the write time. The E/M2816's write time is 10 ms. Once a byte is written, it can be read in 250 ns. The inputs are TTL for both the byte write and read mode.

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode<sup>(1)</sup>, only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a write cycle. During a byte write cycle, addresses are latched on the last falling edge of  $\overline{CE}$  or  $\overline{WE}$  and data is latched on the first rising edge of  $\overline{CE}$  or  $\overline{WE}$ . An internal timer times out the required byte write time. An automatic byte erase is performed internally in the byte write mode.

## Mode Selection (Table 1)

MODE	CE	OE	WE	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	High Z
Byte Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Write Inhibit	X	V <sub>IL</sub>	X	High Z/D <sub>OUT</sub>
	X	X	V <sub>IH</sub>	High Z/D <sub>OUT</sub>

X: Any TTL level.

## Power Up/Down Considerations

The E/M2816A has internal circuitry to minimize a false write during system V<sub>CC</sub> power up or down. This circuitry prevents writing under any one of the following conditions.

1. V<sub>CC</sub> is less than 3 V<sup>(2)</sup>
2. A negative Write Enable ( $\overline{WE}$ ) transition has not occurred when V<sub>CC</sub> is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in a logical state other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65°C to +150°C  
Under Bias ..... -65°C to +135°C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	M2816A	E2816A
Temperature Range	(Case) -55°C to 125°C	(Ambient) -40°C to 85°C
V <sub>CC</sub> Supply Voltage	5 V ± 10%	5 V ± 10%

## Endurance and Data Retention

Condition	Symbol	Parameter	Value	Units
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

### NOTES:

1. Chip Erase is an optional mode
2. Characterized. Not tested.

## DC Operating Characteristics (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
$I_{CC}$	Active $V_{CC}$ Current		125	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = 5.5 V
$I_{SB}$	Standby $V_{CC}$ Current		40	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O's Open; Other Inputs = 5.5 V
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = 5.5 V$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = 5.5 V$
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2.0	6	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1 mA$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400 \mu A$

## AC Characteristics

### Read Operation (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Limits				Units
		E/M2816A-250		E/M2816A-350		
		Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	250		350		ns
$t_{CE}$	Chip Enable Access Time		250		350	ns
$t_{AA}$	Address Access Time		250		350	ns
$t_{OE}$	Output Enable Access Time		90		100	ns
$t_{LZ}$	$\overline{CE}$ to Output in Low Z	10		10		ns
$t_{HZ}$	$\overline{CE}$ to Output in High Z		100		100	ns
$t_{OLZ}$	$\overline{OE}$ to Output in Low Z	50		50		ns
$t_{OHZ}$	$\overline{OE}$ to Output in High Z		100		100	ns
$t_{OH}^{[1]}$	Output Hold from Address Change	20		20		ns
$t_{PU}^{[1]}$	$\overline{CE}$ to Power-up Time	0		0		ns
$t_{PD}^{[1]}$	$\overline{CE}$ to Power Down Time		50		50	ns

### Capacitance<sup>[2]</sup> $T_A=25^\circ C$ , $f=1 MHz$

Symbol	Parameter	Max	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0 V$
$C_{OUT}$	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0 V$

## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{[1]}$	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

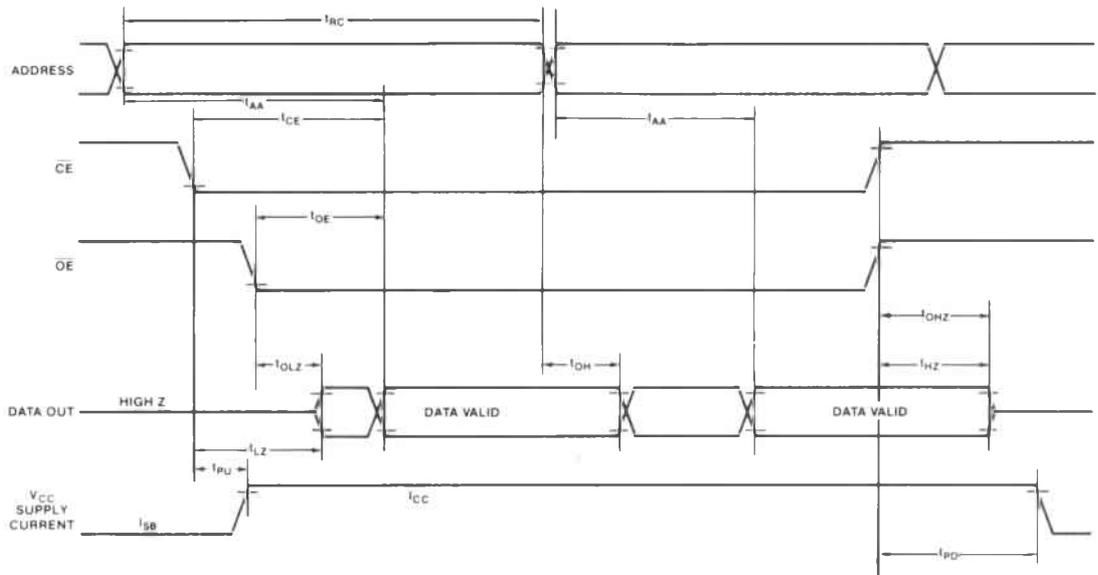
### NOTES:

1. Characterized. Not tested.
2. This parameter measured only for the initial qualification and after process or design changes which may affect capacitance.

### Equivalent A.C. Test Conditions

Output Load: 1 TTL gate and  $C_L = 100 pF$   
 Input Rise and Fall Times: <20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

## Read Cycle Timing



## AC Characteristics

### Write Operation (Over the operating $V_{CC}$ and temperature range)

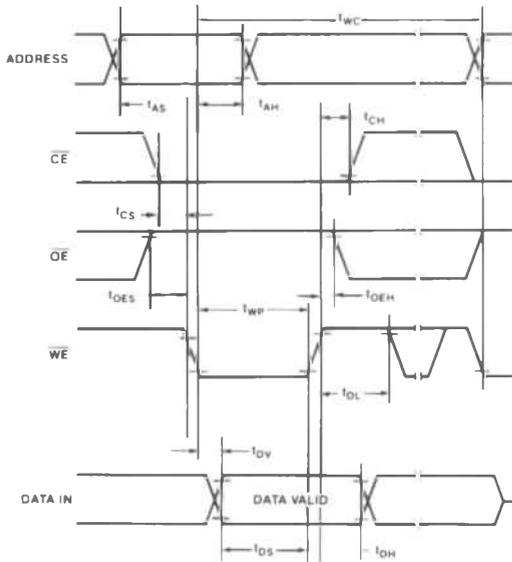
Symbol	Parameter	Limits				Units
		E/M2816A-250		E/M2816A-350		
		Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time	10		10		ms
$t_{AS}$	Address Set Up Time	10		10		ns
$t_{AH}$	Address Hold Time	50		70		ns
$t_{CS}$	Write Set Up Time	0		0		ns
$t_{CH}$	Write Hold Time	0		0		ns
$t_{CW}$	CE to End of Write Input	150		150		ns
$t_{OES}$	OE Set Up Time	10		10		ns
$t_{OEH}$	OE Hold Time	10		10		ns
$t_{WP}^{(1)}$	WE Write Pulse Width	150		150		ns
$t_{DL}$	Data Latch Time	50		50		ns
$t_{DV}^{(2)}$	Data Valid Time		1		1	$\mu$ s
$t_{DS}$	Data Set Up Time	50		50		ns
$t_{DH}$	Data Hold Time	0		0		ns

#### Notes:

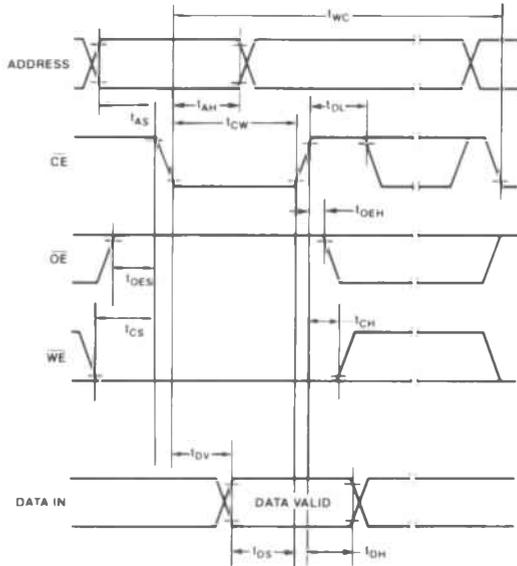
1. WE is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
2. Data must be valid within 1  $\mu$ s maximum after the initiation of a write cycle.

## TTL Byte Write Cycle

### WE CONTROLLED WRITE CYCLE



### CE CONTROLLED WRITE CYCLE



## Ordering Information

PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D - CERAMIC DIP	M - -55°C to +125°C (Military) E - -40°C to +85°C (Extended)	2K x 8 EEPROM	250 - 250 ns 350 - 350 ns	/B - MIL 883 CLASS B Screened

MILITARY



## 16K Electrically Erasable PROMs

February 1987

### Features

- **Military and Temperature Range**
  - -55°C to +125°C: M2817A (Military)
  - -40°C to +85°C: E2817A (Extended)
- **Read/Busy Pin**
- **High Endurance, 10,000 Byte Write Cycles Minimum**
- **On-Chip Timer**
  - Automatic Byte Erase Before Byte Write
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**
- **Low Power Operation**
  - 110 mA Active Current
  - 40 mA Standby Current
- **JEDEC Approved Byte-Wide Pinout**

### Description

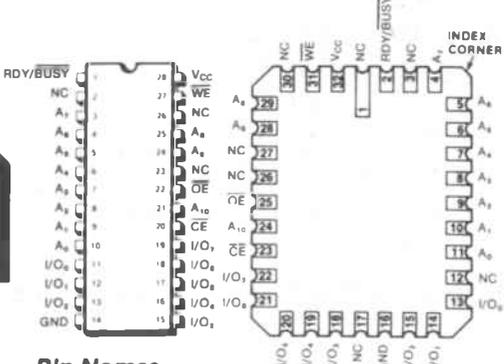
SEEQ's M2817A is a 5 V only, 2K x 8 electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/busy pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the minimum number of times which a byte may be written, is 10 thousand cycles.

The M2817A has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The 2817A's write cycle time is 10 ms over the military temperature

### Pin Configuration

DUAL-IN-LINE  
TOP VIEW

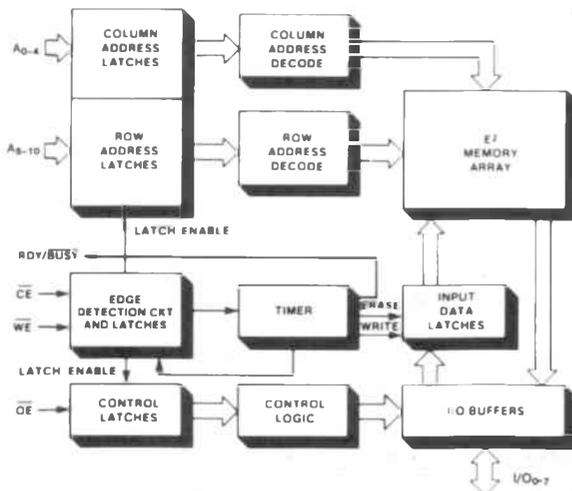
LEADLESS CHIP CARRIER  
BOTTOM VIEW



### Pin Names

A <sub>0-4</sub>	ADDRESSES — COLUMN (LOWER ORDER BITS)
A <sub>5-10</sub>	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE OR ERASE), DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
N/C	NO CONNECT

### Block Diagram



range. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode,<sup>(1)</sup> only TTL inputs are required. To write into a particular location, a TTL low is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a write cycle. During a byte write cycle, addresses are latched on either the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the RDY/BUSY output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/BUSY pin to a TTL high. The RDY/BUSY pin is an open drain output and a typical 3K  $\Omega$  pull-up resistor to  $V_{CC}$  is required. The pull-up resistor value is dependent on the number of OR-tied 2817A RDY/BUSY pins.

## Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O	RDY/BUSY
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>	High Z
Standby	$V_{IH}$	X	X	High Z	High Z
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>	$V_{OL}$
Write inhibit	X	$V_{IL}$	X	High Z/D <sub>OUT</sub>	High Z
	X	X	$V_{IH}$	High Z/D <sub>OUT</sub>	High Z

X: Any TTL Level.

## Recommended Operating Conditions

	M2817A-300 M2817A-250	E 2817A-300 E 2817A-250
$V_{CC}$ Power Supply	5 V $\pm$ 10%	5 V $\pm$ 10%
Temperature Range	(Case) -55°C to +125°C	(Ambient) -40°C to +85°C

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
$T_{DR}$	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

### NOTES:

- Chip Erase is an optional mode
- Characterized. Not tested.

## Power Up/Down Considerations

The M2817A has internal circuitry to minimize a false write during system  $V_{CC}$  power up or down. This circuitry prevents writing under any one of the following conditions.

- $V_{CC}$  is less than 3 V.<sup>(2)</sup>
- A negative Write Enable ( $\overline{WE}$ ) transition has not occurred with  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

### Temperature

Storage ..... -65°C to +150°C

Under Bias ..... -10°C to +135°C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## D.C. Operating Characteristics (Over the operating $V_{CC}$ and temperature range)

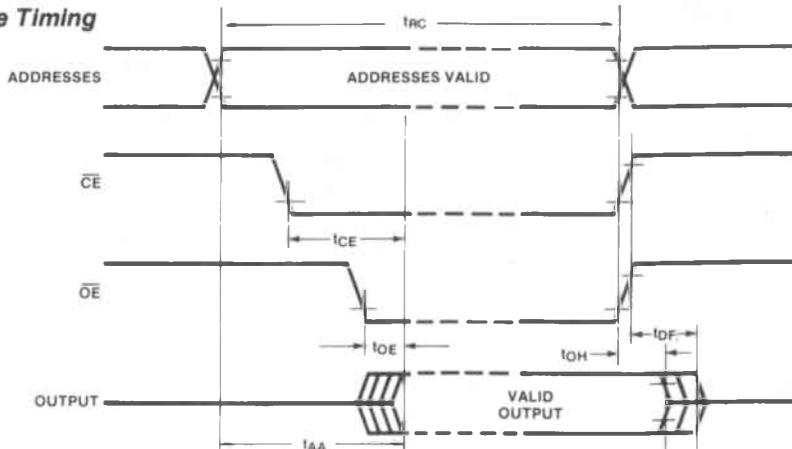
Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
$I_{CC}$	Active $V_{CC}$ Current (Includes Write Operation)		110	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = 5.5 V
$I_{SB}$	Standby $V_{CC}$ Current		40	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = 5.5 V
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = 5.5 V$
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = 5.5 V$
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 1$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1 mA$
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400 \mu A$

## A.C. Characteristics

### Read Operation (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Limits				Units	Test Conditions
		E/M2817A-250		E/M2817A-300			
		Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		100	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output Enable High to Output Not being Driven	0	60	0	60	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

### Read Cycle Timing



MILITARY

## Capacitance<sup>[1]</sup> $T_A=25^\circ\text{C}$ , $f=1\text{ MHz}$

Symbol	Parameter	Max	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0\text{ V}$
$C_{OUT}$	Data (I/O) Capacitance	10 pF	$V_{I/O} = 0\text{ V}$

## A.C. Test Conditions

Output Load: 1 TTL gate and  $C_L = 100\text{ pF}$

Input Rise and Fall Times:  $<20\text{ ns}$

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{[2]}$	E.S.D. Tolerance	$>2000\text{ V}$	MIL-STD 883 Test Method 3015

## AC Characteristics

Write Operation (Over the operating  $V_{CC}$  and temperature range)

Symbol	Parameter	Limits				Units
		E/M2817A-250		E/M2817A-300		
		Min.	Max.	Min.	Max.	
$t_{AS}$	Address to Write Set Up Time	10		10		ns
$t_{CS}$	CE to Write Set Up Time	10		10		ns
$t_{WP}^{[3]}$	WE Write Pulse Width	150		150		ns
$t_{AH}$	Address Hold Time	50		50		ns
$t_{DS}$	Data Set Up Time	50		50		ns
$t_{DH}$	Data Hold Time	0		0		ns
$t_{CH}$	CE Hold Time	0		0		ns
$t_{OES}$	OE Set Up Time	10		10		ns
$t_{OEH}$	OE Hold Time	10		10		ns
$t_{DL}$	Data Latch Time	50		50		ns
$t_{DV}^{[4]}$	Data Valid Time		1		1	$\mu\text{s}$
$t_{DB}$	Time to Device Busy		200		200	ns
$t_{WR}$	Write Recovery Time Before Read Cycle		10		10	$\mu\text{s}$
$t_{WC}$	Byte Write Time		10		10	ms

### NOTES:

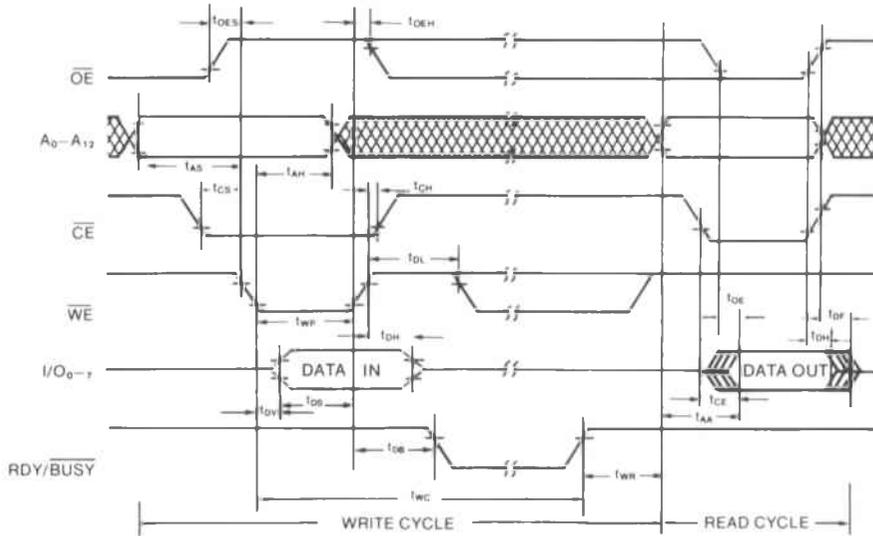
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.

2. Characterized. Not tested.

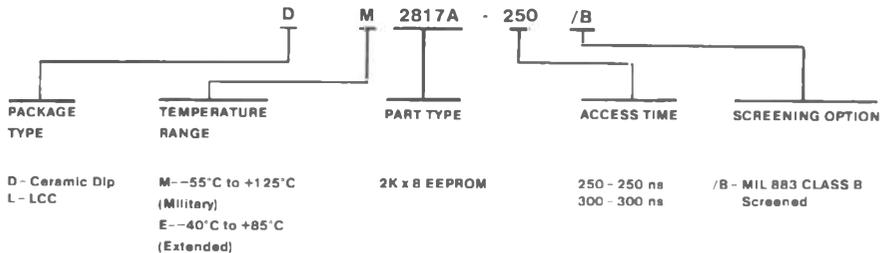
3. WE is noise protected. Less than a 20 ns write pulse will not activate a write cycle.

4. Data must be valid within 1 ms maximum after the initiation of a write cycle.

## Write Cycle Timing



## Ordering Information





#### Features

- **64K EEPROM**
  - Military Temperature M2864
  - Extended Temperature E2864
- **Ready/Busy Pin**
- **High Endurance Write Cycles**
  - 10,000 Cycles/Byte Minimum
- **On-Chip Timer**
  - Automatic Byte Erase Before Byte Write
  - 2 ms Byte Write (M2864H)
- **5 V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **250 ns max. Access Time**

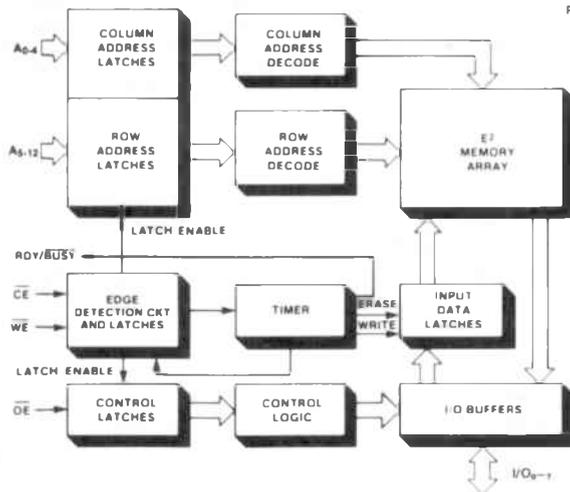
#### Description

SEEQ's M2864 is a 5 V only, 8K x 8 NMOS electrically erasable programmable read only memory (EEPROM). It is packaged in a 28 pin package and has a ready/busy pin. This EEPROM is ideal for applications which require non-volatility and in-system data modification. The endurance, the number of times which a byte may be written, is a minimum of 10 thousand cycles.

The EEPROM has an internal timer that automatically times out the write time. The on-chip timer, along with the input latches, frees the microcomputer system for other tasks during the write time. The standard byte write cycle time is 10 ms. For systems requiring faster byte write, an M2864H is specified at 2 ms. An automatic byte erase is performed before a byte operation is started. Once a byte has been written, the ready/busy pin signals the microprocessor that it is available for another write or a read cycle. All inputs are TTL for both the byte write and read mode. Data retention is specified for ten years.

These two timer EEPROMs are ideal for systems with limited board area. For systems where cost is important, SEEQ has a latch only "52B" family at 16K and 64K bit densities. All "52B" family inputs, except for write enable, are latched by the falling edge of the write enable signal.

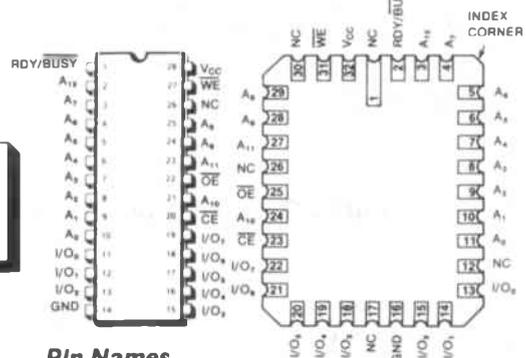
#### Block Diagram



#### Pin Configuration

DUAL-IN-LINE  
TOP VIEW

LEADLESS CHIP CARRIER  
BOTTOM VIEW



#### Pin Names

A <sub>0-4</sub>	ADDRESSES — COLUMN (LOWER ORDER BITS)
A <sub>5-12</sub>	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE); DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
N/C	NO CONNECT

# M2864/M2864H E2864/E2864H

## Device Operation

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. To write into a particular location, a 150 ns TTL pulse is applied to the write enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This, combined with output enable ( $\overline{OE}$ ) being high, initiates a 10 ms write cycle. During a byte write cycle, addresses are latched on either the falling edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred last. Data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$ , whichever one occurred first. The byte is automatically erased before data is written. While the write operation is in progress, the  $RDY/\overline{BUSY}$  output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the  $RDY/\overline{BUSY}$  pin to a TTL high. The  $RDY/\overline{BUSY}$  pin is an open drain output and a typical 3K  $\Omega$  pull-up resistor to  $V_{CC}$  is required. The pull-up resistor value is dependent on the number of OR-tied  $RDY/\overline{BUSY}$  pins. If  $RDY/\overline{BUSY}$  is not used it can be left unconnected.

## Mode Selection (Table 1)

Mode/Pin	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{WE}$ (27)	I/O (11-13,15-19)	$RDY/\overline{BUSY}$ (1)*
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>	High Z
Standby	$V_{IH}$	X	X	High Z	High Z
Byte Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>	$V_{OL}$
Write Inhibit	X	$V_{IL}$	X	High Z/D <sub>OUT</sub>	High Z
	X	X	$V_{IH}$	High Z/D <sub>OUT</sub>	High Z

\*Pin 1 has an open drain output and requires an external 3K resistor to  $V_{CC}$ . The resistor value is dependent on the number of OR-tied  $RDY/\overline{BUSY}$  pins.

## Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature is optional and the timing specifications are available from SEEQ.

## Power Up/Down Considerations

The M2864 has internal circuitry to minimize a false write during system  $V_{CC}$  power up or down. This circuitry prevents writing under any one of the following conditions.

1.  $V_{CC}$  is less than 3 V.<sup>[1]</sup>
2. A negative Write Enable ( $\overline{WE}$ ) transition has not occurred when  $V_{CC}$  is between 3 V and 5 V.

Writing will also be prevented if  $\overline{CE}$  or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

## Absolute Maximum Stress Ratings\*

Temperature

Storage	-65°C to +150°C
Under Bias	-65°C to +135°C

All Inputs or Outputs with

Respect to Ground ..... +6 V to -0.3 V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	M2864 M2864H	E2864 E2864H
$V_{CC}$ Supply Voltage	5 V $\pm$ 10%	5 V $\pm$ 10%
Temperature Range	(Case) -55°C to +125°C	(Ambient) -40°C to +85°C

## Endurance and Data Retention

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
$T_{DR}$	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

NOTE: 1 - Characterized, Not tested.

# M2864/M2864H E2864/E2864H

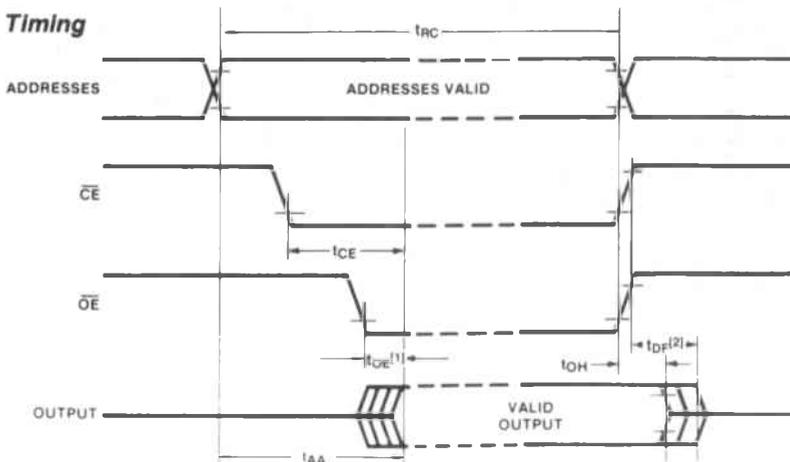
## DC Operating Characteristics (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
$I_{CC}$	Active $V_{CC}$ Current (Includes Write Operation)		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = $V_{CC}$ Max.
$I_{SB}$	Standby $V_{CC}$ Current		50	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = $V_{CC}$ Max.
$I_{LI}$	Input Leakage Current		10	$\mu A$	$V_{IN} = V_{CC}$ Max.
$I_{LO}$	Output Leakage Current		10	$\mu A$	$V_{OUT} = V_{CC}$ Max.
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2.0	$V_{CC} + 1$	V	
$V_{OL}$	Output Low Voltage		0.4	V	$I_{OL} = 2.1$ mA
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400$ $\mu A$

## AC Characteristics Read Operation (Over the operating $V_{CC}$ and temperature range)

Symbol	Parameter	Limits						Units	Test Conditions
		E/M2864H-250 E/M2864-250		E/M2864H-300 E/M2864-300		M2864-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		100		100	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output Enable High to Output Not being Driven	0	60	0	60	0	80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

### Read Cycle Timing



#### NOTES:

- $\overline{OE}$  MAY BE DELAYED TO  $t_{AA} - t_{OE}$  AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON  $t_{AA}$ .
- $t_{DP}$  IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$ , WHICHEVER OCCURS FIRST.

# M2864/M2864H E2864/E2864H

**Capacitance**  $T_A^{[1]} = 25^\circ\text{C}$ ;  $f = 1\text{ MHz}$

Symbol	Parameter	Max.	Conditions
C <sub>IN</sub>	Input Capacitance	6 pF	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	Data (I/O) Cap.	10 pF	V <sub>I/O</sub> = 0 V

## AC Test Conditions

Output Load: 1 TTL gate and C<sub>L</sub> = 100 pF

Input Rise and Fall Times: <20 ns

Input Pulse Levels: 0.45 V to 2.4 V

Timing Measurement Reference Level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

## E.S.D. Characteristics<sup>[4]</sup>

Symbol	Parameter	Value	Test Conditions
V <sub>ZAP</sub>	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

## AC Characteristics

**Write Operation** (Over operating temperature and V<sub>CC</sub> range)

Symbol	Parameter	Limits						Units
		E/M2864H-250 E/M2864-250		E/M2864H-300 E/M2864-300		E/M2864H-350 E/M2864-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>wc</sub>	Write Cycle Time/Byte Standard Family Only		10		10		10	ms
	"H" Family Only		2		2		—	ms
t <sub>AS</sub>	Address to WE Set Up Time	10		10		10		ns
t <sub>CS</sub>	CE to Write Set Up Time	0		0		0		ns
t <sub>wpl</sub> <sup>[2]</sup>	WE Write Pulse Width	150		150		150		ns
t <sub>AH</sub>	Address Hold Time	50		50		70		ns
t <sub>DS</sub>	Data Set Up Time	50		50		50		ns
t <sub>DH</sub>	Data Hold Time	20		20		20		ns
t <sub>CH</sub>	CE Hold Time	0		0		0		ns
t <sub>OES</sub>	OE Set Up Time	10		10		10		ns
t <sub>OEH</sub>	OE Hold Time	10		10		10		ns
t <sub>DL</sub>	Data Latch Time	50		50		50		ns
t <sub>DV</sub> <sup>[3]</sup>	Data Valid Time		1		1		1	μs
t <sub>DB</sub>	Time to Device Busy		200		200		200	ns
t <sub>WR</sub>	Write Recovery Time Before Read Cycle		10		10		10	μs

**Notes:**

- 1 This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
- 2 WE is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
3. Data must be valid within 1 μs maximum after the initiation of a write cycle.
- 4 Characterized. Not tested.





### Features

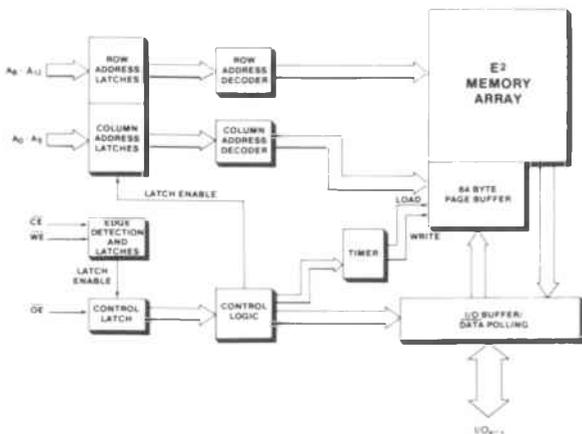
- **Military and Extended Temperature Range**
  - -55°C to +125°C Operation (Military)
  - -40°C to +85°C Operation (Extended)
- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 250 μA Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 us Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - DATA Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte Minimum
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **250 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**

### Description

SEEQ's E/M28C64 is a CMOS 5V only, 8K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The E/M28C64 is ideal for applications which require low power consumption non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and it's innovative "Q-Cell" design. System reliability, in all applications, is higher because of the low failure rate of the Q-Cell.

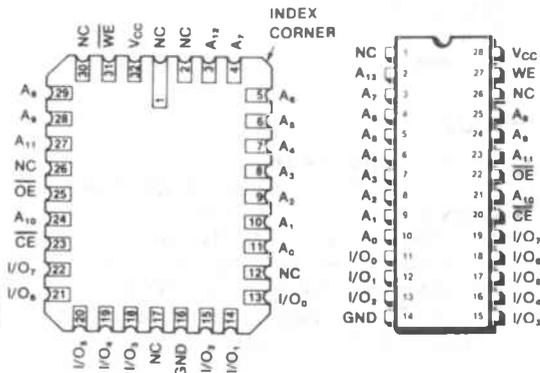
The E/M28C64 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the micro-

### Pin Configuration



LEADLESS CHIP CARRIER  
BOTTOM VIEW

DUAL-IN-LINE  
TOP VIEW



### Pin Names

A <sub>0-7</sub>	ADDRESSES—COLUMN
A <sub>8-A11</sub>	ADDRESSES—ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE)/DATA OUTPUT (READ)
NC	NO CONNECTION

processor for other tasks while the part is busy writing. The E/M28C64's write cycle time is 10 ms. An automatic erase is performed before a write. The DATA polling feature of the E/M28C64 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 250 ns. Data retention is specified for 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

### Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>
Standby	$V_{IH}$	X	X	HI Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>
Write Inhibit	X	$V_{IL}$	X	HI Z/D <sub>OUT</sub>
Chip Erase	$V_{IL}$	$V_H$	$V_{IL}$	X

X: Any TTL level

$V_H$ : High Voltage

### Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{CE}$  is brought to a TTL low in order to enable the chip. The  $\overline{WE}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{OE}$ ) to a TTL low. During read, the address,  $\overline{CE}$ ,  $\overline{OE}$ , and I/O latches are transparent.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This combined with Output Enable ( $\overline{OE}$ ) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{WP}$  time. Data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred first. An automatic erase is performed before data is written.

### Write Cycle Control Pins

For system design simplification, the E/M28C64 is designed such that either the  $\overline{CE}$  or  $\overline{WE}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{CE}$  or  $\overline{WE}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{OE}$  setup and hold are with respect to the later of  $\overline{CE}$  or  $\overline{WE}$ ; data setup and hold is with respect to the earlier of  $\overline{WE}$  or  $\overline{CE}$ .

To simplify the following discussion, the  $\overline{WE}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

### Write Mode

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the E/M28C64 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated within  $t_{BLC}$  after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle (DATA polling).

### Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the E/M28C64 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will not start the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

### DATA Polling

The E/M28C64 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time. DATA polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the E/M28C64 is **still writing**, the device will present the ones-complement of the last byte written. When the E/M28C64 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.

A DATA polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle. DATA polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a DATA polling read is the same as a normal read.

### Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

### Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}V$
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}V$  and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a write in the Mode Selection table.

**Absolute Maximum Stress Range\***

**Temperature**

Storage..... -65°C to +150°C

Under Bias ..... -65°C to +135°C

**All Input or Output Voltages**

with Respect to Ground..... +6 V to -0.3 V

\*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	<b>M28C64</b>	<b>E28C64</b>
Temperature Range	(Case) -55°C to +125°C	(Ambient) -40°C to +85°C
V <sub>CC</sub> Power Supply	5 V ± 10%	5 V ± 10%

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

**DC Characteristics** (Over operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max; Max read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = ANY TTL LEVEL
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		250	μA	$\overline{CE} = V_{CC} - 0.3$ ; Other inputs = V <sub>IL</sub> to V <sub>IH</sub> ; All I/O Open
I <sub>IL</sub> <sup>[2]</sup>	Input Leakage Current		10	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>OL</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>WI</sub> <sup>[1]</sup>	Write Inhibit Voltage	3.8		V	

**Notes:**

- 1. Characterized. Not tested.
- 2. Inputs only. Does not include I/O.

**AC Test Conditions**

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times: <20 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**Capacitance**<sup>(1)</sup>  $T_A = 25^\circ\text{C}$ ,  $f = 1$  MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

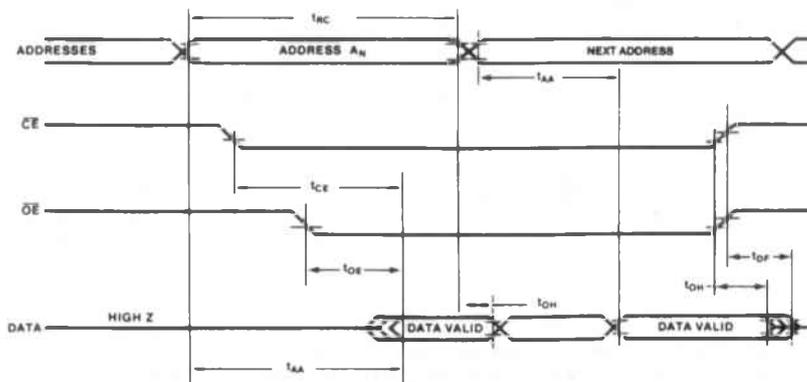
**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

**AC Characteristics Read Operation** (Over operating temperature and  $V_{CC}$  range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		E/M28C64-250		E/M28C64-300		E/M28C64-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		150		150	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output or Chip Enable High to output not being driven	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

**Read/ $\overline{DATA}$  Polling Cycle Time**



**Notes:**

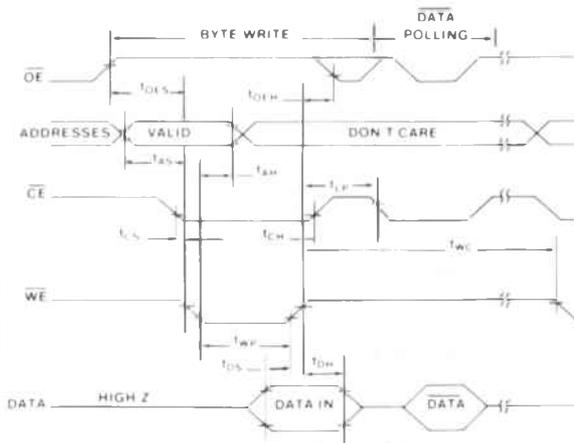
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance
2. Characterized. Not tested.

**AC Characteristics Write Operation** (Over the operating temperature and  $V_{CC}$  range, unless otherwise specified)

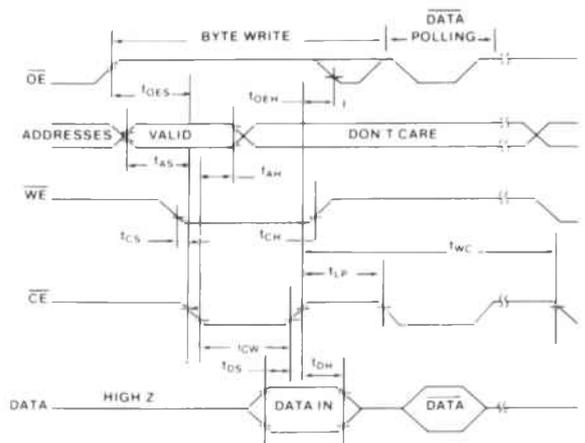
Symbol	Parameter	Limits						Units
		E/M28C64-250		E/M28C64-300		E/M28C64-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time		10		10		10	ms
$t_{AS}$	Address Set-up Time	10		10		10		ns
$t_{AH}$	Address Hold Time (see note 1)	150		150		150		ns
$t_{CS}$	Write Set-up Time	0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		ns
$t_{CW}$	$\overline{CE}$ Pulse Width (note 2)	150		150		150		ns
$t_{OES}$	OE High Set-up Time	10		10		10		ns
$t_{OEH}$	OE High Hold Time	10		10		10		ns
$t_{WP}$	$\overline{WE}$ Pulse Width (note 2)	150		150		150		ns
$t_{DS}$	Data Set-up Time	50		50		50		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{BLC}$	Byte Load Timer Cycle (Page Mode Only) (see note 3)	0.2	200	0.2	200	0.2	200	us
$t_{LP}$	Last Byte Loaded to DATA Polling		200		200		200	ns

**Write Timing**

**$\overline{WE}$  CONTROLLED WRITE CYCLE**



**$\overline{CE}$  CONTROLLED WRITE CYCLE**



**Notes:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3.  $t_{BLC}$  min. is the minimum time before the next byte can be loaded.  $t_{BLC}$  max. is the minimum time the byte load timer waits before initiating internal write cycle.





### Features

- **Military and Extended Temperature Range**
  - -55°C to +125°C Operation (Military)
  - -40°C to +85°C Operation (Extended)
- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 250 µA Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 us Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - DATA Polling
  - RDY/BUSY Pin
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte Minimum
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **250 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**

### Description

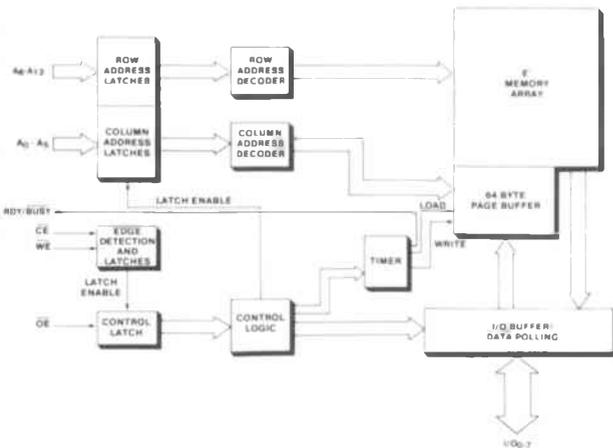
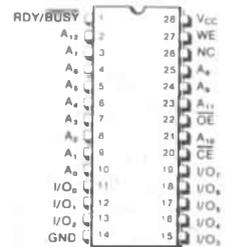
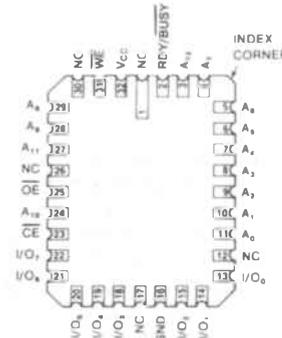
SEEQ's E/M28C65 is a CMOS 5V only, 8K x 8 electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The E/M28C65 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and it's innovative "Q-Cell" design. System reliability, in all applications, is higher because of the low failure rate of the Q-Cell.

The E/M28C65 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the microprocessor

### Pin Configuration

LEADLESS CHIP CARRIER  
BOTTOM VIEW

DUAL-IN-LINE  
TOP VIEW



### Pin Names

A <sub>0-5</sub>	ADDRESSES — COLUMN
A <sub>6-12</sub>	ADDRESSES ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)
RDY/BUSY	DEVICE READY/BUSY
NC	NO CONNECTION

MILITARY

for other tasks while the part is busy writing. The E/M28C65's write cycle time is 10 ms. An automatic erase is performed before a write. The  $\overline{\text{DATA}}$  polling feature of the E/M28C65 can be used to determine the end of a write cycle. Once the write has been completed, data can be read in a maximum of 250 ns. Data retention is specified for 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and  $\overline{\text{WE}}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of aforementioned three input lines.

### Mode Selection

MODE	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O	RDY/BUSY <sup>(1)</sup>
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>	HI Z
Standby	V <sub>IH</sub>	X	X	HI Z	HI Z
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>	V <sub>OL</sub>
Write Inhibit	X	V <sub>IL</sub>	X	HI Z/D <sub>OUT</sub>	HI Z
Inhibit	X	X	V <sub>IH</sub>	HI Z/D <sub>OUT</sub>	HI Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub>	V <sub>IL</sub>	X	HI Z

X: Any TTL level  
V<sub>H</sub>: High Voltage

### Reads

A read is accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{\text{CE}}$  is brought to a TTL low in order to enable the chip. The  $\overline{\text{WE}}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{\text{OE}}$ ) to a TTL low. During read, the address,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and I/O latches are transparent.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{\text{WE}}$ ) pin of a selected ( $\overline{\text{CE}}$  low) device. This combined with Output Enable ( $\overline{\text{OE}}$ ) being high, initiates a write cycle. During write cycle, all inputs except data are latched on the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{\text{WP}}$  time. Data is latched on the rising edge of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ , whichever occurred first. An automatic erase is performed before data is written.

### Write Cycle Control Pins

For system design simplification, the E/M28C65 is designed such that either the  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{\text{OE}}$  setup and hold are with respect to the later of  $\overline{\text{CE}}$  or  $\overline{\text{WE}}$ ; data setup and hold is with respect to the earlier of  $\overline{\text{WE}}$  or  $\overline{\text{CE}}$ .

To simplify the following discussion, the  $\overline{\text{WE}}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

#### NOTES:

1. RDY/BUSY Pin 1 (Pin 2 on LCC) has an open drain output and requires an external 3K resistor to V<sub>CC</sub>. The value of the resistor is dependent on the number of OR-tied RDY/BUSY pins

**Write Mode**

One to 64 bytes of data can be randomly loaded into the page. The part latches row addresses, A6-A12, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of the write cycle. This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the E/M28C65 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated within  $t_{BLC}$  after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can be read to determine the end of write cycle ( $\overline{DATA}$  polling).

**Extended Page Load**

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the E/M28C65 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will not start the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

 **$\overline{DATA}$  Polling**

The E/M28C65 has a maximum write cycle time of 10 ms. Typically though, a write will be completed

in less than the specified maximum cycle time.  $\overline{DATA}$  polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the E/M28C65 is **still writing**, the device will present the ones-complement of the last byte written. When the E/M28C65 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly.

A  $\overline{DATA}$  polling read can occur immediately after a byte is loaded into a page, prior to the initiation of the internal write cycle.  $\overline{DATA}$  polling attempted during the middle of a page load cycle will present a ones-complement of the most recent data byte loaded into the page. Timing for a  $\overline{DATA}$  polling read is the same as a normal read.

**READY/ $\overline{BUSY}$  Pin**

E/M28C65 provides write cycle status on this pin. RDY/ $\overline{BUSY}$  output goes to a TTL low immediately after the falling edge of  $\overline{WE}$ . RDY/ $\overline{BUSY}$  will remain low during the byte load or page load cycle and continues to remain at a TTL low while the write cycle is in progress. An internal timer times out the required write cycle time and at the end of this time, the device signals RDY/ $\overline{BUSY}$  pin to a TTL high. This pin can be polled for write cycle status or used to initiate a rising edge triggered interrupt indicating write cycle completion. The RDY/ $\overline{BUSY}$  pin is an open drain output and a typical 3 K pull-up resistor to  $V_{CC}$  is required. The pull-up value is dependent on the number of OR-tied RDY/ $\overline{BUSY}$  pins. If RDY/ $\overline{BUSY}$  is not used, it can be left unconnected.

**Chip Erase**

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

**Power Up/Down Considerations**

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$  and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a write in the Mode Selection table.

**Absolute Maximum Stress Range\***

*Temperature*

Storage..... -65°C to +150°C

Under Bias ..... -65°C to +135°C

*All Input or Output Voltages*

with Respect to Ground..... +6 V to -0.3 V

\*COMMENT: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	<b>M28C64</b>	<b>E28C64</b>
Temperature Range	(Case) -55°C to +125°C	(Ambient) -40°C to +85°C
V <sub>CC</sub> Power Supply	5 V ± 10%	5 V ± 10%

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	>10	Years	MIL-STD 883 Test Method 1008

**DC Characteristics** (Over operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		60	mA	$\overline{CE} = \overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = V <sub>CC</sub> Max.; Max read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	$\overline{CE} = V_{IH}$ , $\overline{OE} = V_{IL}$ ; All I/O Open; Other Inputs = ANY TTL LEVEL
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		250	μA	$\overline{CE} = V_{CC} - 0.3$ ; Other inputs = V <sub>IL</sub> to V <sub>IH</sub> ; All I/O Open
I <sub>IL</sub> [2]	Input Leakage Current		1	μA	V <sub>IN</sub> = V <sub>CC</sub> Max.
I <sub>OL</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> = V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> + 0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> = 2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA
V <sub>WI</sub> [1]	Write Inhibit Voltage	3.8		V	

**Notes:**

- 1. Characterized. Not tested.
- 2. Inputs only. Does not include I/O.

## AC Test Conditions

Output Load: 1 TTL gate and  $C_L = 100 \text{ pF}$   
 Input Rise and Fall Times:  $< 20 \text{ ns}$   
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

## Capacitance<sup>(1)</sup> $T_A = 25 \text{ C}, f = 1 \text{ MHz}$

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

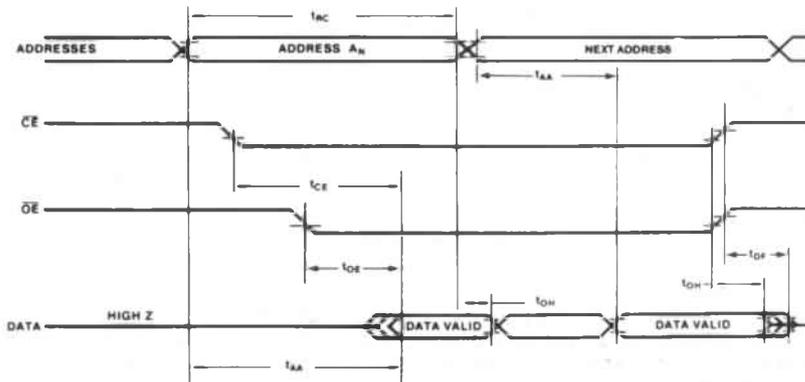
## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{(2)}$	E.S.D. Tolerance	$> 2000 \text{ V}$	MIL-STD 883 Test Method 3015

## AC Characteristics Read Operation (Over operating temperature and $V_{CC}$ range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		E/M28C65-250		E/M28C65-300		E/M28C65-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	250		300		350		ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable Access Time		250		300		350	ns	$\overline{OE} = V_{IL}$
$t_{AA}$	Address Access Time		250		300		350	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{OE}$	Output Enable Access Time		90		150		150	ns	$\overline{CE} = V_{IL}$
$t_{DF}$	Output or Chip Enable High to output not being driven	0	60	0	80	0	80	ns	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE} = V_{IL}$

## Read/Data Polling Cycle Time



**Notes:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance
2. Characterized. Not tested.

## AC Characteristics

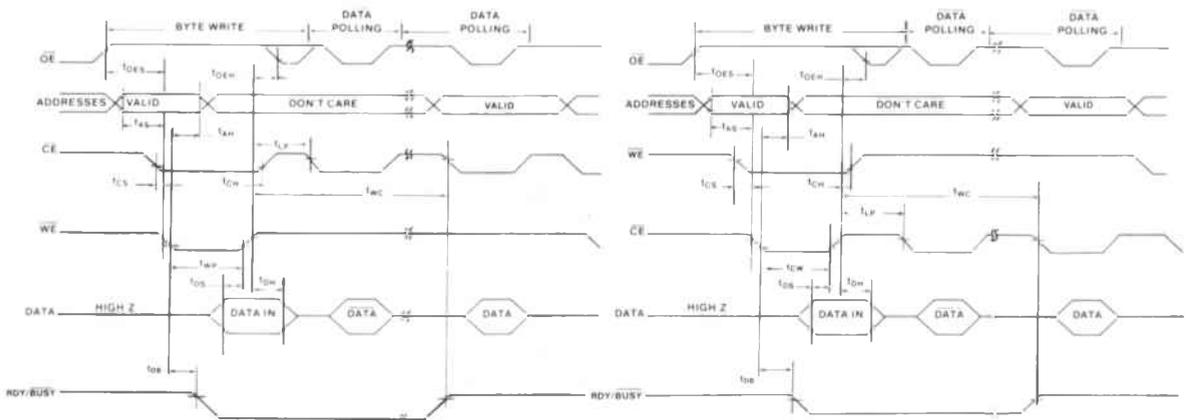
**Write Operation** (Over the operating  $V_{CC}$  and temperature range)

Symbol	Parameter	Limits						Units
		E/M28C65-250		E/M28C65-300		E/M28C65-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time		10		10		10	ms
$t_{AS}$	Address Set-up Time	10		10		10		ns
$t_{AH}$	Address Hold Time (see note 1)	150		150		150		ns
$t_{CS}$	Write Set-up Time	0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		ns
$t_{CW}$	$\overline{CE}$ Pulse Width (note 2)	150		150		150		ns
$t_{OES}$	$\overline{OE}$ High Set-up Time	10		10		10		ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	10		10		10		ns
$t_{WP}$	$\overline{WE}$ Pulse Width (note 2)	150		150		150		ns
$t_{DS}$	Data Set-up Time	50		50		50		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{BLC}$	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	200	0.2	200	0.2	200	us
$t_{LP}$	Last Byte Loaded to DATA Polling		200		200		200	ns
$t_{DB}$	Time to Device Busy		100		100		100	ns

### Write Timing

**$\overline{WE}$  CONTROLLED WRITE CYCLE**

**$\overline{CE}$  CONTROLLED WRITE CYCLE**



**NOTES:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3.  $t_{BLC}$  min. is the minimum time before the next byte can be loaded.  $t_{BLC}$  max. is the minimum time the byte load timer waits before initiating the internal write cycle.





### Features

- **Military and Extended Temperature Range**
  - -55°C to +125°C Operation (Military)
  - -40°C to +85°C Operation (Extended)
- **CMOS Technology**
- **Low Power**
  - 60 mA Active
  - 250 μA Standby
- **Page Write Mode**
  - 64 Byte Page
  - 160 us Average Byte Write Time
- **Byte Write Mode**
- **Write Cycle Completion Indication**
  - DATA Polling
- **On Chip Timer**
  - Automatic Erase Before Write
- **High Endurance**
  - 10,000 Cycles/Byte
  - 10 Year Data Retention
- **Power Up/Down Protection Circuitry**
- **250 ns Maximum Access Time**
- **JEDEC Approved Byte Wide Pinout**

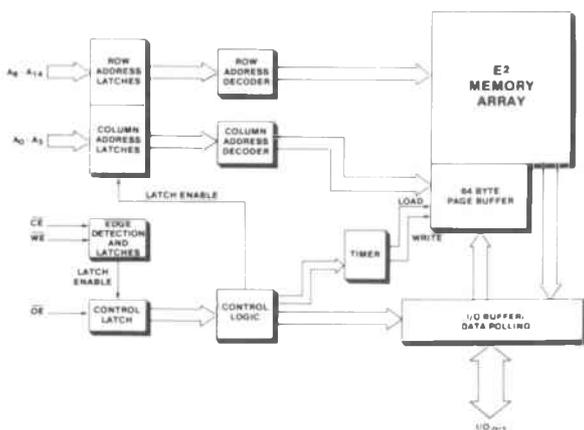
### Description

SEEQ's 28C256 is a CMOS 5V only, 32K x 8 Electrically Erasable Programmable Read Only Memory (EEPROM). It is manufactured using SEEQ's advanced 1.25 micron CMOS Process and is available in both a 28 pin Cerdip package as well as a Leadless Chip Carrier (LCC). The 28C256 is ideal for applications which require low power consumption, non-volatility and in system reprogrammability. The endurance, the number of times a byte can be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinary high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative "Q-Cell" design. System reliability, in all applications, is higher because of the low failure rate of the Q-Cell.

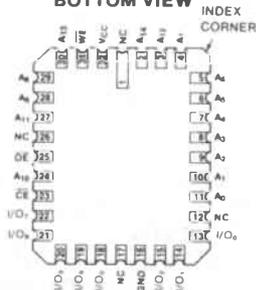
The 28C256 has an internal timer which automatically times out the write time. The on-chip timer, along with input latches free the micro-

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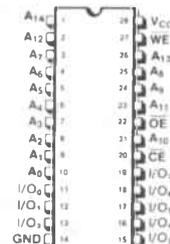
### Pin Configuration



LEADLESS CHIP CARRIER  
BOTTOM VIEW



DUAL-IN-LINE  
TOP VIEW



### Pin Names

A0-5	ADDRESSES — COLUMN
A6-14	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O	DATA INPUT (WRITE)/DATA OUTPUT (READ)

processor for other tasks while the part is busy writing. The 28C256's write cycle time is 10 ms maximum. An automatic erase is performed before a write. The DATA polling feature of the 28C256 can be used to determine the end of a write cycle. Once the write cycle has been completed, data can be read in a maximum of 250 ns. Data retention is greater than 10 years.

## Device Operation

### Operational Modes

There are five operational modes (see Table 1) and, except for the chip erase mode, only TTL inputs are required. A Write can only be initiated under the conditions shown. Any other conditions for  $\overline{CE}$ ,  $\overline{OE}$ , and  $\overline{WE}$  will inhibit writing and the I/O lines will either be in a high impedance state or have data, depending on the state of the aforementioned three input lines.

**Table 1**

### Mode Selection

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	HI Z
Write	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Write Inhibit	X	X	V <sub>IH</sub>	HI Z/D <sub>OUT</sub>
	X	V <sub>IL</sub>	X	HI Z/D <sub>OUT</sub>
Chip Erase	V <sub>IL</sub>	V <sub>H</sub>	V <sub>IL</sub>	X

X: any TTL level  
V<sub>H</sub>: High Voltage

### Reads

A read is typically accomplished by presenting the address of the desired byte to the address inputs. Once the address is stable,  $\overline{CE}$  is brought to a TTL low in order to enable the chip. The  $\overline{WE}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing Output Enable ( $\overline{OE}$ ) to a TTL low. During read, the addresses,  $\overline{CE}$ ,  $\overline{OE}$ , and input data latches are transparent.

### Writes

To write into a particular location, the address must be valid and a TTL low applied to the Write Enable ( $\overline{WE}$ ) pin of a selected ( $\overline{CE}$  low) device. This combined with Output Enable ( $\overline{OE}$ ) being high initiates a write cycle. During a byte write cycle, all inputs except data are latched on the falling edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred last. Write enable needs to be at a TTL low only for the specified  $t_{WP}$  time. Data is latched on the rising edge of  $\overline{WE}$  or  $\overline{CE}$ , whichever occurred first. An automatic erase is performed before data is written.

The 28C256 can write both bytes and blocks of up to 64 bytes. The write mode is discussed below.

### Write Cycle Control Pins

For system design simplification, the 28C256 is designed such that either the  $\overline{CE}$  or  $\overline{WE}$  pin can be used to initiate a write cycle. The device uses the latest high-to-low transition of either  $\overline{CE}$  or  $\overline{WE}$  signal to latch addresses and the earliest low-to-high transition to latch the data. Address and  $\overline{OE}$  set up and hold are with respect to the later of  $\overline{CE}$  or  $\overline{WE}$ ; data set up and hold is with respect to the earlier of  $\overline{WE}$  or  $\overline{CE}$ .

To simplify the following discussion, the  $\overline{WE}$  pin is used as the write cycle control pin throughout the rest of this data sheet. Timing diagrams of both write cycles are included in the AC Characteristics.

## Write Mode

One to 64 bytes of data can be randomly loaded into the device. The part latches row addresses, A6-A14, during the first byte write. These addresses are latched on the falling edge of the  $\overline{WE}$  signal and are ignored after that until the end of  $t_{WC}$ . This will eliminate any false write into another page if different row addresses are applied and the page boundary is crossed.

The column addresses, A0-A5, which are used to select different locations of the page, are latched every time a new write is initiated. These addresses and the  $\overline{OE}$  state (high) are latched on the falling edge of  $\overline{WE}$  signal. For proper write initiation and latching, the  $\overline{WE}$  pin has to stay low for a minimum of  $t_{WP}$  ns. Data is latched on the rising edge of  $\overline{WE}$ , allowing easy microprocessor interface.

Upon a low to high  $\overline{WE}$  transition, the 28C256 latches data and starts the internal page load timer. The timer is reset on the falling edge of the  $\overline{WE}$  signal if another write is initiated before the timer has timed out. The timer stays reset while the  $\overline{WE}$  pin is kept low. If no additional write cycles have been initiated in ( $t_{BLC}$ ) after the last  $\overline{WE}$  low to high transition, the part terminates the page load cycle and starts the internal write. During this time which takes a maximum of 10 ms, the device ignores any additional write attempts. The part can now be read to determine the end of write cycle (DATA Polling).

## Extended Page Load

In order to take advantage of the page mode's faster average byte write time, data must be loaded at the page load cycle time ( $t_{BLC}$ ). Since some applications may not be able to sustain transfers at this minimum rate, the 28C256 permits an extended page load cycle. To do this, the write cycle must be "stretched" by maintaining  $\overline{WE}$  low, assuming a write enable-controlled cycle, and leaving all other control inputs ( $\overline{CE}$ ,  $\overline{OE}$ ) in the proper page load cycle state. Since the page load timer is reset on the falling edge of  $\overline{WE}$ , keeping this signal low will inhibit the page load timer. When  $\overline{WE}$  returns high, the input data is latched and the page load cycle timer begins. In  $\overline{CE}$  controlled write the same is true, with  $\overline{CE}$  holding the timer reset instead of  $\overline{WE}$ .

## DATA Polling

The 28C256 has a maximum write cycle time of 10 ms. Typically though, a write will be completed in less than the specified maximum cycle time.  $\overline{DATA}$  polling is a method of minimizing write times by determining the actual endpoint of a write cycle. If a read is performed to any address while the 28C256 is **still writing**, the device will present the ones-complement of the last byte written. When the 28C256 has **completed** its write cycle, a read from the last address written will result in valid data. Thus, software can simply read from the part until the last data byte written is read correctly. A  $\overline{DATA}$  polling read should not be done until a minimum of  $t_{LP}$  microseconds after the last byte is written. Timing for a  $\overline{DATA}$  polling read is the same as a normal read once the  $t_{LP}$  specification has been met.

## Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

## Power Up/Down Considerations

There is internal circuitry to minimize a false write during power up or power down. This circuitry prevents writing under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$ , V
2. A high to low Write Enable ( $\overline{WE}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$ , V and  $V_{CC}$  with  $\overline{CE}$  low and  $\overline{OE}$  high.

Writing will also be inhibited when  $\overline{WE}$ ,  $\overline{CE}$ , or  $\overline{OE}$  are in TTL logical states other than that specified for a byte write in the Mode Selection table.

**Absolute Maximum Stress Range\***

Temperature

Storage..... -65°C to +150°C

Under Bias..... -65°C to +135°C

All input or Output Voltages

with Respect to V<sub>ss</sub>..... +6 V to -0.3 V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	M28C256	E28C256
Temperature Range	(Case) -55°C to +125°C	(Ambient) -40°C to 85°C
V <sub>CC</sub> Power Supply	5 V ± 10%	5 V ± 10%

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**DC Characteristics Read Operation** (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Units	Test Condition
		Min.	Max.		
I <sub>CC</sub>	Active V <sub>CC</sub> Current		60	mA	CE=OE=V <sub>IL</sub> ; All I/O open; Other Inputs = V <sub>CC</sub> Max. Min. read or write cycle time
I <sub>SB1</sub>	Standby V <sub>CC</sub> Current (TTL Inputs)		2	mA	CE=V <sub>IH</sub> , OE=V <sub>IL</sub> ; All I/O open; Other Inputs = V <sub>IL</sub> to V <sub>IH</sub>
I <sub>SB2</sub>	Standby V <sub>CC</sub> Current (CMOS Inputs)		250	µA	CE=V <sub>CC</sub> -0.3 Other Inputs = V <sub>IL</sub> to V <sub>IH</sub> All I/O Open
I <sub>IL</sub> <sup>[2]</sup>	Input Leakage Current		1	µA	V <sub>IN</sub> =V <sub>CC</sub> Max.
I <sub>OL</sub> <sup>[3]</sup>	Output Leakage Current		10	µA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2.0	V <sub>CC</sub> +0.3	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =2.1 mA
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> =-400 µA
V <sub>WI</sub> <sup>[1]</sup>	Write Inhibit Voltage	3.8		V	

NOTES:

1. Characterized. Not tested.
2. Inputs only. Does not include I/O.
3. For I/O only.

**AC Test Conditions**

Output Load: 1 TTL gate and  $C_L = 100 \text{ pF}$   
 Input Rise and Fall Times:  $< 20 \text{ ns}$   
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**Capacitance**<sup>[1]</sup>  $T_A = 25^\circ\text{C}, f = 1 \text{ MHz}$

Symbol	Parameter	Max.	Conditions
C <sub>IN</sub>	Input Capacitance	6 pF	V <sub>IN</sub> = OV
C <sub>OUT</sub>	Data (I/O) Capacitance	12 pF	V <sub>I/O</sub> = OV

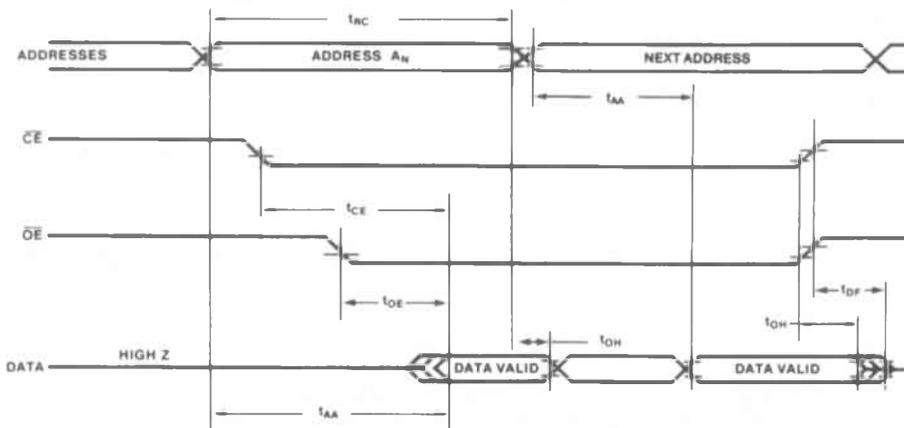
**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
V <sub>ZAP</sub> <sup>[2]</sup>	E.S.D. Tolerance	> 2000 V.	MIL-STD 883 Test Method 3015

**AC Characteristics Read Operation** (Over operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Units						Units	Test Conditions
		E/M28C256-250		E/M28C256-300		E/M28C256-350			
		Min.	Max.	Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read Cycle Time	250		300		350		ns	CE = OE = V <sub>IL</sub>
t <sub>CE</sub>	Chip Enable Access Time		250		300		350	ns	OE = V <sub>IL</sub>
t <sub>AA</sub>	Address Access Time		250		300		350	ns	CE = OE = V <sub>IL</sub>
t <sub>OE</sub>	Output Enable Access Time		150		150		150	ns	CE = V <sub>IL</sub>
t <sub>DF</sub>	Output or Chip Enable High to output in HI-Z	0	60	0	80	0	80	ns	CE = V <sub>IL</sub>
t <sub>OH</sub>	Output Hold from Address Change, Chip Enable, or Output Enable, whichever occurs first	0		0		0		ns	CE = OE = V <sub>IL</sub>

**Read/DATA Polling Cycle**



**Notes:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

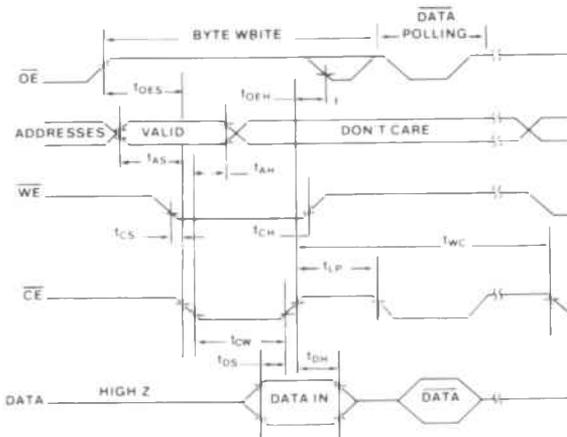
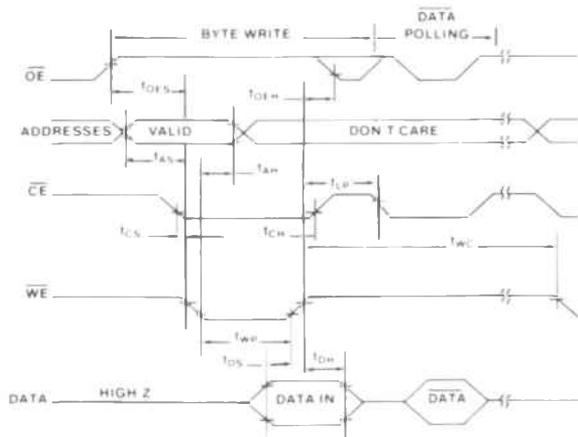
## AC Characteristics Write Operation (Over the operating temperature and V<sub>CC</sub> range, unless otherwise specified)

Symbol	Parameter	Limits						Units
		E/M28C256-250		E/M28C256-300		E/M28C256-350		
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>WC</sub>	Write Cycle Time		10		10		10	ms
t <sub>AS</sub>	Address Set-up Time	20		20		20		ns
t <sub>AH</sub>	Address Hold Time (see note 1)	150		150		150		ns
t <sub>CS</sub>	Write Set-up Time	0		0		0		ns
t <sub>CH</sub>	Write Hold Time	0		0		0		ns
t <sub>CW</sub>	$\overline{CE}$ Pulse Width (note 2)	150		150		150		ns
t <sub>OES</sub>	$\overline{OE}$ High Set-up Time	20		20		20		ns
t <sub>OEH</sub>	$\overline{OE}$ High Hold Time	20		20		20		ns
t <sub>WP</sub>	$\overline{WE}$ Pulse Width (note 2)	150		150		150		ns
t <sub>DS</sub>	Data Set-up Time	50		50		50		ns
t <sub>DH</sub>	Data Hold Time	0		0		0		ns
t <sub>BLC</sub>	Byte Load Timer Cycle (Page Mode Only) (note 3)	0.2	200	0.2	200	0.2	200	us
t <sub>LP</sub>	Last Byte Loaded to $\overline{DATA}$ Polling		650		650		650	us

### Write Timing

#### $\overline{WE}$ CONTROLLED WRITE CYCLE

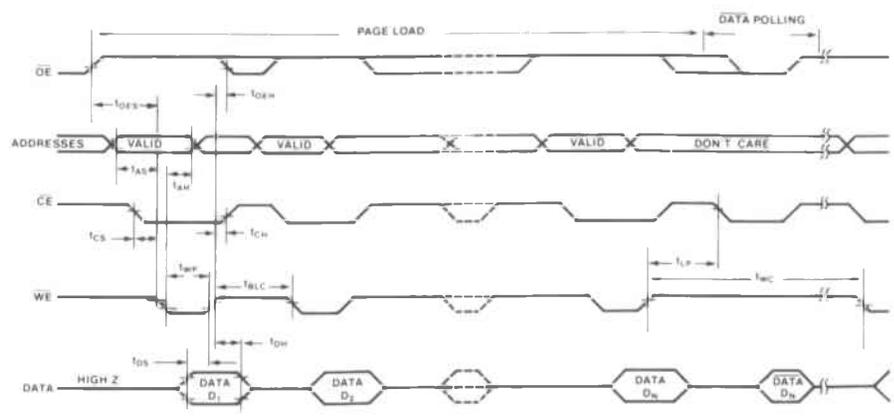
#### $\overline{CE}$ CONTROLLED WRITE CYCLE



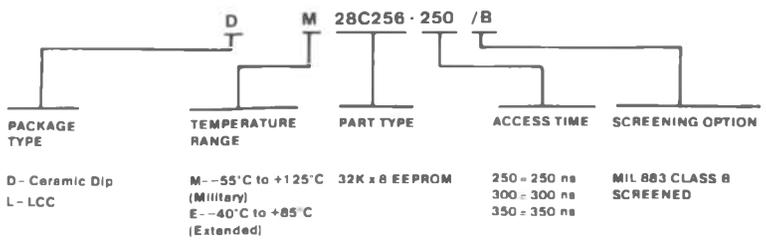
**Notes:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .
2.  $\overline{WE}$  and  $\overline{CE}$  are noise protected. Less than a 20 nsec write pulse will not activate a write cycle.
3. t<sub>BLC</sub> min. is the minimum time before the next byte can be loaded. t<sub>BLC</sub> max. is the minimum time the byte load timer waits before initiating internal write cycle.

**Page Write Timing**



**Ordering Information**



PACKAGE TYPE	TEMPERATURE RANGE	PART TYPE	ACCESS TIME	SCREENING OPTION
D - Ceramic Dip	M - -55°C to +125°C (Military)	32K x 8 EEPROM	250 = 250 ns	MIL 883 CLASS B
L - LCC	E - -40°C to +85°C (Extended)		300 = 300 ns	SCREENED
			350 = 350 ns	

**MILITARY**



# seeq

# E/M36C16 E/M36C32

## High Speed CMOS Electrically Erasable PROM

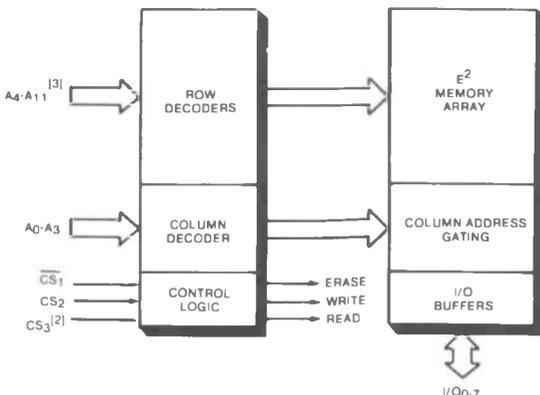
PRELIMINARY DATA SHEET

October 1987

### Features

- **Military and Extended Temperature Range**
  - -55°C to +125°C Operation (Military)
  - -40°C to +85°C Operation (Extended)
- **High Speed:**
  - 45 ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 400 mW
- **10 Year Data Retention**
- **High Output Drive**
  - Sink 16 mA At 0.45 V
  - Source 4 mA At 2.4 V
- **5V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **50 ms Chip Erase**
- **Fast Byte Write**
  - 5 ms/Byte
- **Automatic byte clear before write**
- **Jedec approved byte wide pinout**
- **Direct replacement for bipolar PROMS**
- **Slim 300 mil Packaging Available**

### Block Diagram



### Pin Names

A <sub>0</sub> -A <sub>3</sub>	ADDRESSES — COLUMN
A <sub>4</sub> -A <sub>11</sub> <sup>[3]</sup>	ADDRESSES — ROW
CS <sub>1</sub> CS <sub>2</sub> CS <sub>3</sub>	CHIP SELECT INPUTS
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)

### Description

SEEQ's 36C16/32 are high speed 2K x 8 / 4K x 8 Electrically Erasable Programmable Read Only Memories, manufactured using SEEQ's advanced 1.25 micron CMOS process.

The 36C16/32 are intended as bipolar PROM replacements in high speed applications. The 45 ns maximum read access time meets the requirements of many of today's high performance processors. In addition they offer in-system reprogrammability. The endurance, the number of times the part can be erased/written, is specified to be greater than 100 cycles. The 36C16/32 are built using SEEQ's proprietary oxynitride EEPROM process and its innovative "DQ cell" design. System reliability in applications where writes are frequent is increased because of the low endurance-failure rate of the DQ-cell.

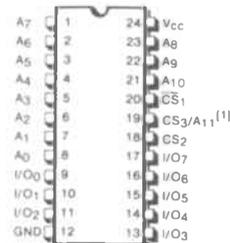
Data retention is specified to be greater than 10 years.

The 36C16/32 are available in 24 pin Slim 300 mil CERAMIC DIP. 24/28 pin full featured EEPROM versions are also available (38C16/32).

### Pin Configuration

DUAL-IN-LINE  
TOP VIEW

36C16/36C32  
(24 pins)



- NOTES: 1. Pin 19 is A11 on the 36C32  
2. CS3 is on the 36C16 only.  
3. A4-A10 on 36C16.

**Device Operation**  
**Operational Modes**

MODE PIN	CS <sub>1</sub>	CS <sub>2</sub>	CS <sub>3</sub> <sup>[2]</sup>	I/O
Read	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Standby	V <sub>IH</sub>	X	X	HI Z
	X	V <sub>IL</sub>	X	
	X	X	V <sub>IL</sub>	
Write	V <sub>H</sub> <sup>[1]</sup>	V <sub>IL</sub>	X	D <sub>IN</sub>

X: Any TTL level

**Read**

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable, the chip select inputs should be brought to the proper levels in order to enable the outputs (see Table above).

**Write**

To write into a particular location, addresses and data must be valid, CS<sub>2</sub> must be TTL low and a V<sub>H</sub><sup>[1]</sup> pulse has to be applied to CS<sub>1</sub> for 5ms. An automatic internal byte clear is done prior to the byte write. The byte clear feature is transparent to the user.

**NOTES:**

1. V<sub>H</sub> - High Voltage.
2. CS<sub>3</sub> applies only to the 36C16. This pin becomes A<sub>11</sub> in the 36C32 and a don't care during operational modes.

**Absolute Maximum Rating**

Temperature

Storage..... -65°C to +150°C

Under Bias..... -65°C to +135°C

All Inputs and Outputs

with Respect to Ground..... -0.5 V to +7 V

Dedicated High Voltage Inputs

with Respect to Ground..... -0.5 V to +14V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	<b>E36C16</b> <b>E36C32</b>	<b>M36C16</b> <b>M36C32</b>
V <sub>CC</sub> Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range	(Ambient) -40°C to +85°C	(Case) -55°C to +125°C

**DC Operating Characteristics** (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		120	mA	CS <sub>2</sub> =CS <sub>3</sub> =V <sub>IH</sub> ; $\overline{CS_1}$ =V <sub>IL</sub> ; All inputs = V <sub>CC</sub> Max. Max read/write cycle time
I <sub>IN</sub>	Input Leakage Current		1	μA	0.1V > V <sub>IN</sub> < V <sub>CC</sub> Max.
I <sub>OUT</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2	V <sub>CC</sub> + 1	V	
V <sub>H</sub>	Input High Voltage During Write/Chip Erase	10.8	13.2	V	For $\overline{CS_1}$ , Input Only
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =16 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> =-4 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
I <sub>OS</sub> <sup>(1)</sup>	Output Short Circuit Current	-20	-90	mA	V <sub>CC</sub> =V <sub>CC</sub> Max, V <sub>OUT</sub> =0
V <sub>CI</sub> <sup>(1)</sup>	Input Clamp Voltage	-1.5		V	V <sub>IN</sub> Pulse width ≤ 10ns

**NOTE:**

1. Only one output at a time for less than one second

**AC Test Conditions**

Output Load: 10 TTL gates and total  $C_L = 30$  pF  
 Input Rise and Fall Times: < 5 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{[2]}$	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

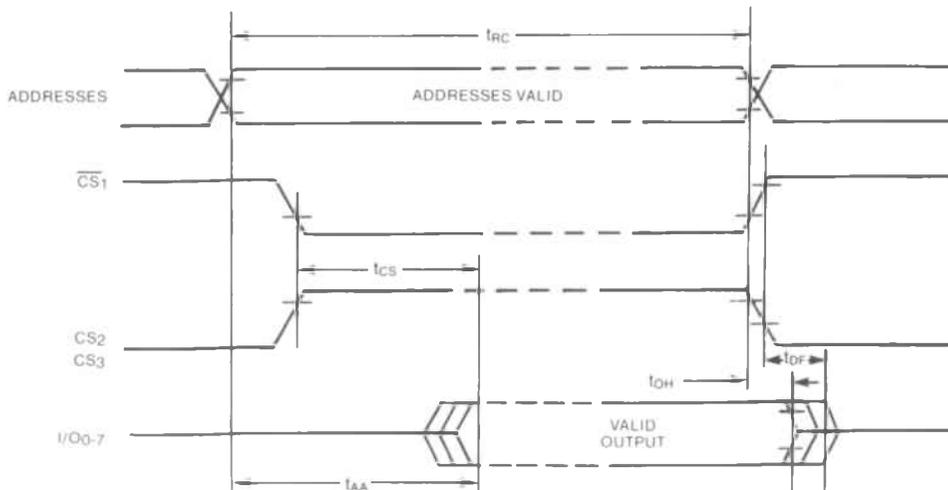
**Capacitance**<sup>[1]</sup>  $T_A=25^\circ\text{C}$ ,  $f=1$  MHz

Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

**AC Characteristics Read Operation** (Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	Limits						Units
		E/M36C16-45 E/M36C32-45		E/M36C16-55 E/M36C32-55		E/M36C16-70 E/M36C32-70		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	45		55		70		ns
$t_{CS}$	Chip Select Access Time		30		35		45	ns
$t_{AA}$	Address Access Time		45		55		70	ns
$t_{DF}$	Output Enable to Output not being Driven		25		30		35	ns
$t_{OH}$	Output Hold from Address Change or Chip Select whichever occurs first	0		0		0		ns

**Read Cycle Timing**



**Notes:**

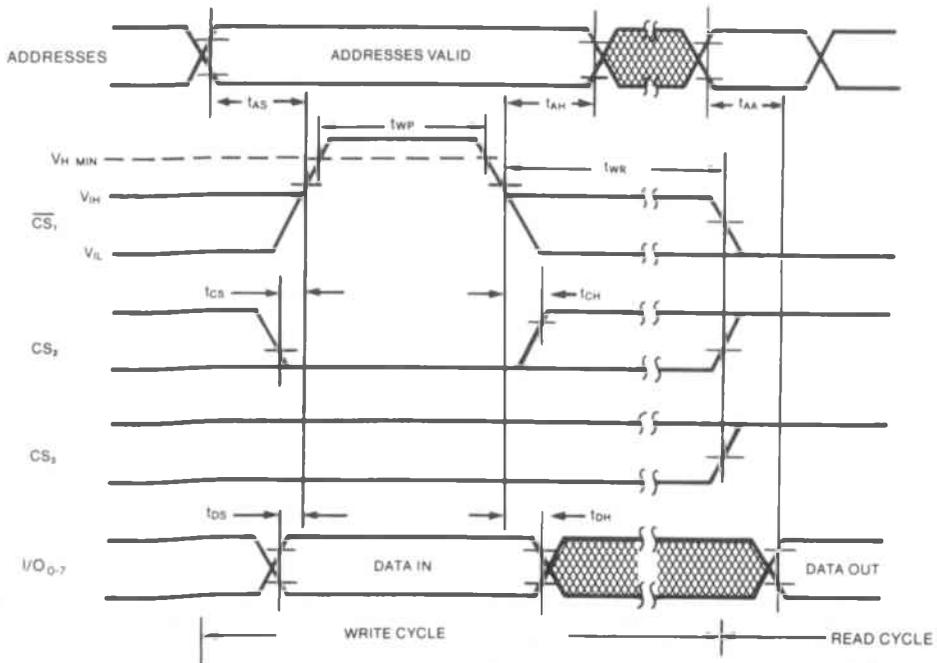
1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

**AC Characteristics Write Operation (All Speeds)**

(Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	E/M36C16 E/M36C32		Units
		Min.	Max.	
$t_{WP}$	Write Pulse Width	5	50	ms
$t_{AS}$	Address Set-up Time	0		$\mu$ s
$t_{AH}$	Address Hold Time	0.5		$\mu$ s
$t_{CS}$	$CS_2$ Set-up Time	0		$\mu$ s
$t_{CH}$	$CS_2$ Hold Time	0		$\mu$ s
$t_{DS}$	Data Set-up Time	0		$\mu$ s
$t_{DH}$	Data Hold Time	0		$\mu$ s
$t_{WR}$	Write Recovery		10	$\mu$ s

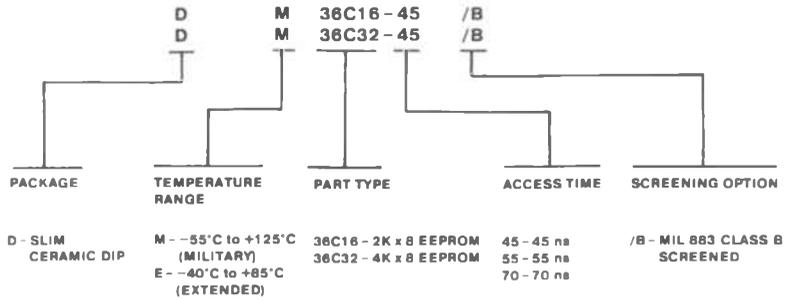
**Write Cycle Timing**



MILITARY

# Ordering Information

**E/M36C16**  
**E/M36C32**  
 PRELIMINARY DATA SHEET



The "Preliminary Data Sheet" designation on a SEEQ data sheet indicates that the product is not fully characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. SEEQ Technology or an authorized sales representative should be consulted for current information before using this product. No responsibility is assumed by SEEQ for its use, nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. SEEQ reserves the right to make changes in specifications at any time and without notice.

## High Speed CMOS Electrically Erasable PROM

PRELIMINARY DATA SHEET

October 1987

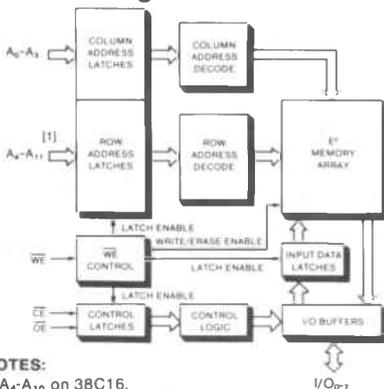
### Features

- **Military and Extended Temperature Range**
  - -55°C to +125°C Operation (Military)
  - -40°C to +85°C Operation (Extended)
- **High Speed:**
  - 45 ns Maximum Access Time
- **CMOS Technology**
- **Low Power:**
  - 400 mW
- **High Endurance:**
  - 10,000 Cycles/Byte Minimum
  - 10 Year Data Retention
- **On-Chip Timer and Latches**
  - Automatic Byte Erase Before Write
  - Fast Byte Write: 5 ms/Byte
- **High Speed Address/Data Latching**
- **50 ms Chip Erase**
- **5V ± 10% Power Supply**
- **Power Up/Down Protection Circuitry**
- **DATA Polling of Data Bit 7**
- **Jedec approved Byte Wide Pinout**
  - 38C16: 2816A Pin Compatible
  - 38C32: 28C64 Pin Compatible

### Pin Names

A <sub>0</sub> -A <sub>3</sub>	ADDRESSES — COLUMN
A <sub>4</sub> -A <sub>11</sub> <sup>[1]</sup>	ROW ADDRESSES
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0-7</sub>	DATA INPUT (WRITE) DATA OUTPUT (READ)

### Block Diagram



#### NOTES:

1. A<sub>4</sub>-A<sub>10</sub> on 38C16.
2. NC — No Connect

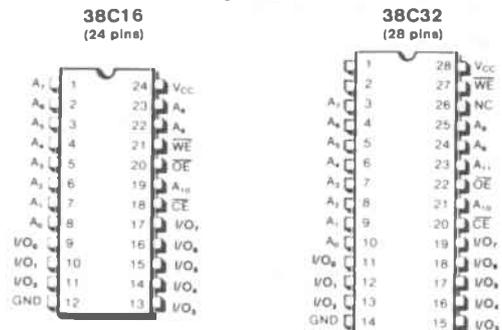
### Description

SEEQ's 38C16/32 are high speed 2K x 8 / 4K x 8 Electrically Erasable Programmable Read Only Memories (EEPROM), manufactured using SEEQ's advanced 1.25 micron CMOS process.

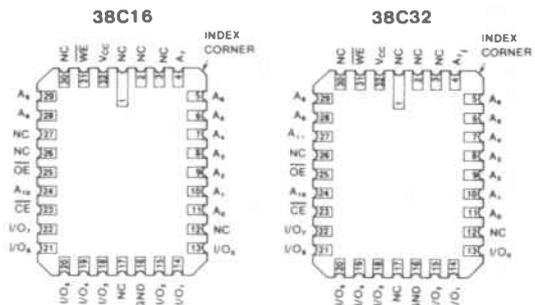
The 38C16/32 are ideal for high speed applications which require non-volatility and in-system reprogrammability. The endurance, the number of times a byte may be written, is specified at 10,000 cycles per byte and is typically 1,000,000 cycles per byte. The extraordinarily high endurance was accomplished using SEEQ's proprietary oxynitride EEPROM process and its innovative "DQ cell" design. System reliability in applications where writes are frequent is increased because of the low endurance-failure rate of the DQ-cell. The 45 ns maximum access

### Pin Configuration

#### DUAL-IN-LINE TOP VIEW



#### LEADLESS CHIP CARRIER BOTTOM VIEW



time meets the requirements of many of today's high performance processors. The 38C16/32 have an internal timer which automatically times out the write time. The on-chip timer, along with the input latches, frees the microprocessor for other tasks during the write time.  $\overline{\text{DATA}}$  Polling can be used to determine the end of a write cycle. All inputs are TTL compatible for both write and read modes.

Data retention is specified to be greater than 10 years.

The 38C16 is available in 24 pin CERAMIC DIP; the 38C32 in 28 pin CERAMIC DIP; 32 pin LCC packaged versions are also available. 24 pin versions of both 38C16 and 38C32 intended for bipolar PROM replacement are also available (36C16/36C32). All parts are available in commercial as well as military temperature ranges.

## Device Operation Operational Modes

MODE PIN	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	$D_{OUT}$
Standby	$V_{IH}$	X	X	HI Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	$D_{IN}$
Write Inhibit	X $V_{IH}$ X $V_{IL}$	X X $V_{IL}$ $V_{IL}$	$V_{IH}$ X $V_{IH}$ $V_{IL}$	HI Z/ $D_{OUT}$ HI Z HI Z/ $D_{OUT}$ No Operation (HI Z)
Chip Erase <sup>[1]</sup>	$V_{IH}$	$V_H$ <sup>[2]</sup>	$V_{IH}$	HI Z

X: Any TTL level

### Read

A read is started by presenting the addresses of the desired byte to the address inputs. Once the address is stable,  $\overline{\text{CE}}$  is brought to a TTL low in order to enable the chip. The  $\overline{\text{WE}}$  pin must be at a TTL high during the entire read cycle. The output drivers are made active by bringing output enable ( $\overline{\text{OE}}$ ) to a TTL low. During read, the address,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}}$ , and I/O latches are transparent.

#### NOTES:

1. Chip erase is an optional mode.
2.  $V_H$  — High Voltage.

### Write

To write into a particular location, addresses must be valid and a TTL low is applied to the write enable ( $\overline{\text{WE}}$ ) pin of a selected ( $\overline{\text{CE}}$  low) device. This initiates a write cycle. During a write cycle, all inputs except for data are latched on the falling edge of  $\overline{\text{WE}}$  (or  $\overline{\text{CE}}$ , whichever one occurred last). Write enable needs to be at a TTL low only for the specified  $t_{WP}$  time. Data is latched on the rising edge of  $\overline{\text{WE}}$  (or  $\overline{\text{CE}}$ , which ever one occurred first). An automatic byte erase is performed before data is written.

### $\overline{\text{DATA}}$ Polling

The EEPROM has a specified  $t_{WC}$  write cycle time of 5ms. The typical device has a write cycle time faster than the  $t_{WC}$ .  $\overline{\text{DATA}}$  polling is a method to indicate the completion of a timed write cycle. During the internal write cycle, the complement of the data bit 7 is presented at output 7 when a read is performed. Once the write cycle is finished, the true data is presented at the outputs. A software routine can be used to "poll", i.e. read the output, for true or complemented data bit 7. The polling cycle specifications are the same as for a read cycle. During data polling, the addresses are don't care.

### Chip Erase

Certain applications may require all bytes to be erased simultaneously. This feature, which requires high voltage, is optional and timing specifications are available from SEEQ.

### Power Up/Down Considerations

Protection against false write during  $V_{CC}$  power up/down is provided through on chip circuitry. Writing is prevented under any one of the following conditions:

1.  $V_{CC}$  is less than  $V_{WI}$ .
1. A high to low Write Enable ( $\overline{\text{WE}}$ ) transition has not occurred when the  $V_{CC}$  supply is between  $V_{WI}$  and  $V_{CC}$  with  $\overline{\text{CE}}$  low and  $\overline{\text{OE}}$  high.

Writing will also be inhibited when  $\overline{\text{WE}}$ ,  $\overline{\text{CE}}$ , or  $\overline{\text{OE}}$  are in TTL logical states other than those specified for a byte write in the Mode Selection table.

**Absolute Maximum Rating**

Temperature  
 Storage..... -65°C to +150°C  
 Under Bias..... -65°C to +135°C  
 All Inputs and Outputs  
 with Respect to Ground..... -0.5 V to +7 V  
 Dedicated High voltage Inputs  
 with Respect to Ground..... -0.5 V to +14 V

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

	M38C16 M38C32	E38C16 E38C32
V <sub>CC</sub> Supply Voltage	5 V ± 10%	5 V ± 10%
Temperature Range	(Case) -55°C to 125°C	(Ambient) -40°C to 85°C

**Endurance and Data Retention**

Symbol	Parameter	Value	Units	Condition
N	Minimum Endurance	10,000	Cycles/Byte	MIL-STD 883 Test Method 1033
T <sub>DR</sub>	Data Retention	> 10	Years	MIL-STD 883 Test Method 1008

**DC Operating Characteristics** (Over operating temperature and V<sub>CC</sub> Range, unless otherwise specified)

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
I <sub>CC</sub>	V <sub>CC</sub> Active Current		120	mA	CE=OE=V <sub>IL</sub> ; All I/O open; All other inputs = V <sub>CC</sub> Max. Max read/write cycle time
I <sub>SB</sub>	Stand by V <sub>CC</sub> Current		60	mA	CE=V <sub>IH</sub> ; All I/O open; All other inputs TTL don't care;
I <sub>IN</sub>	Input Leakage Current		1	μA	0.1V >= V <sub>IN</sub> <= V <sub>CC</sub> Max.
I <sub>OUT</sub>	Output Leakage Current		10	μA	V <sub>OUT</sub> =V <sub>CC</sub> Max.
V <sub>IL</sub>	Input Low Voltage	-0.1	0.8	V	
V <sub>IH</sub>	Input High Voltage	2	V <sub>CC</sub> + 1	V	
V <sub>OL</sub>	Output Low Voltage		0.45	V	I <sub>OL</sub> =2 mA, V <sub>CC</sub> = V <sub>CC</sub> Min.
V <sub>OH</sub>	Output High Voltage	2.4		V	I <sub>OH</sub> = -400 μA, V <sub>CC</sub> Min.
V <sub>WI</sub> <sup>[1]</sup>	Write Inhibit Voltage	3.8		V	

**NOTES:**

1. Characterized. Not tested.

MILITARY

**AC Test Conditions**

Output Load: 1 TTL gate and total  $C_L = 30$  pF  
 Input Rise and Fall Times: < 5 ns  
 Input Pulse Levels: 0.45 V to 2.4 V  
 Timing Measurement Reference Level:  
 Inputs 1 V and 2 V  
 Outputs 0.8 V and 2 V

**E.S.D. Characteristics**

Symbol	Parameter	Value	Test Conditions
$V_{ZAP}^{[2]}$	E.S.D. Tolerance	>2000 V	MIL-STD 883 Test Method 3015

**Capacitance<sup>[1]</sup>**  $T_A=25^\circ\text{C}$ ,  $f=1$  MHz

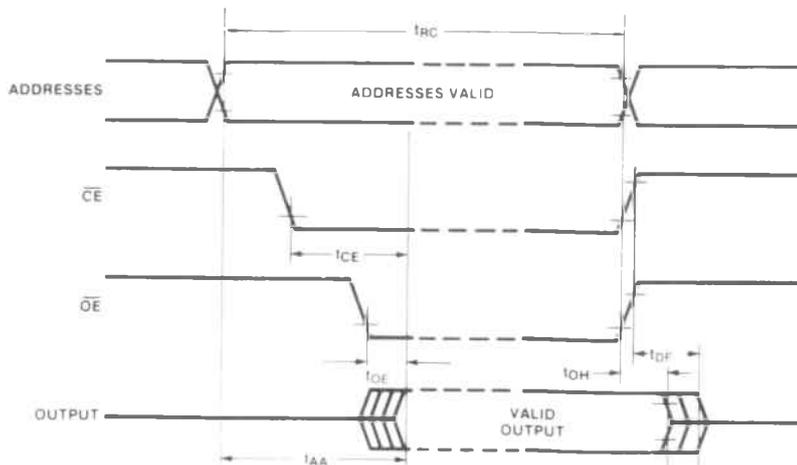
Symbol	Parameter	Max.	Conditions
$C_{IN}$	Input Capacitance	6 pF	$V_{IN} = 0V$
$C_{OUT}$	Data (I/O) Capacitance	12 pF	$V_{I/O} = 0V$

**AC Characteristics Read Operation**

(Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

Symbol	Parameter	Limits						Units	Test Conditions
		E/M38C16-45 E/M38C32-45		E/M38C16-55 E/M38C32-55		E/M38C16-70 E/M38C32-70			
		Min.	Max.	Min.	Max.	Min.	Max.		
$t_{RC}$	Read Cycle Time	45		55		70		ns	$\overline{CE}=\overline{OE}=V_{IL}$
$t_{CE}$	Chip Enable Access Time		30		35		45	ns	$\overline{OE}=V_{IL}$
$t_{AA}$	Address Access Time		45		55		70	ns	$\overline{CE}=\overline{OE}=V_{IL}$
$t_{OE}$	Output Enable Access Time		25		30		40	ns	$\overline{CE}=V_{IL}$
$t_{DF}$	Output Or Chip Enable To Output Float		25		30		35	ns	$\overline{CE}=V_{IL}$
$t_{OH}$	Output Hold from Address Change, Chip Enable Or Output Enable Which ever occurs first	0		0		0		ns	$\overline{CE}$ or $\overline{OE}=V_{IL}$

**Read Cycle Timing**



**NOTES:**

1. This parameter is measured only for the initial qualification and after process or design changes which may affect capacitance.
2. Characterized. Not tested.

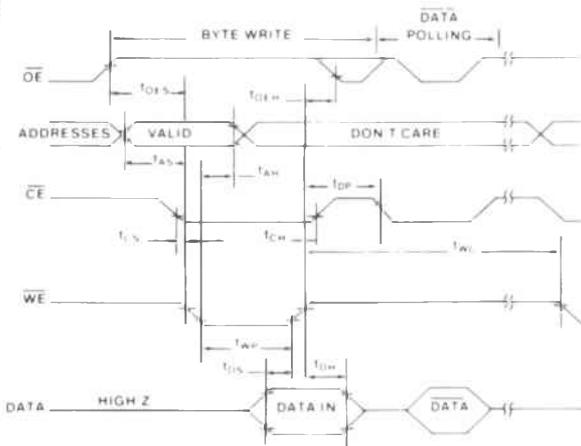
**AC Characteristics Write Operation**

(Over operating temperature and  $V_{CC}$  Range, unless otherwise specified)

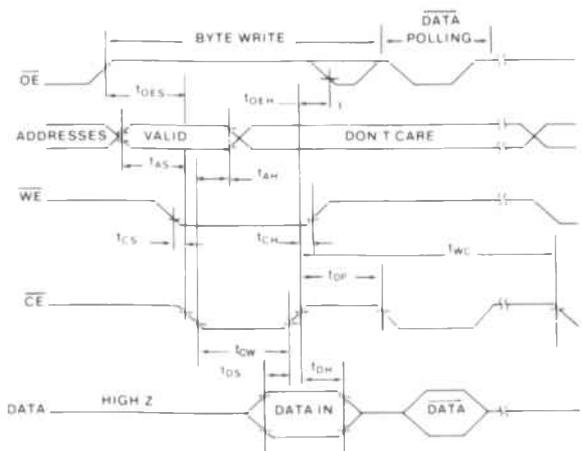
Symbol	Parameter	E/M38C16-45 E/M38C32-45		E/M38C16-55 E/M38C32-55		E/M38C16-70 E/M38C32-70		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{WC}$	Write Cycle Time		5		5		5	ms
$t_{AS}$	Address Set-up Time	0		0		0		ns
$t_{AH}$	Address Hold Time	25		30		40		ns
$t_{CS}$	Write Set-up Time	0		0		0		ns
$t_{CH}$	Write Hold Time	0		0		0		ns
$t_{CW}$	$\overline{CE}$ Pulse Width	25		30		40		ns
$t_{OES}$	$\overline{OE}$ High Set-up Time	5		5		5		ns
$t_{OEH}$	$\overline{OE}$ High Hold Time	0		0		0		ns
$t_{WP}$	$\overline{WE}$ Pulse Width	25		30		40		ns
$t_{DS}$	Data Set-up Time	25		30		40		ns
$t_{DH}$	Data Hold Time	0		0		0		ns
$t_{DP}$	Time to DATA Polling from Byte Latch		45		55		70	ns

**Write Cycle Timing**

**$\overline{WE}$  CONTROLLED WRITE CYCLE**



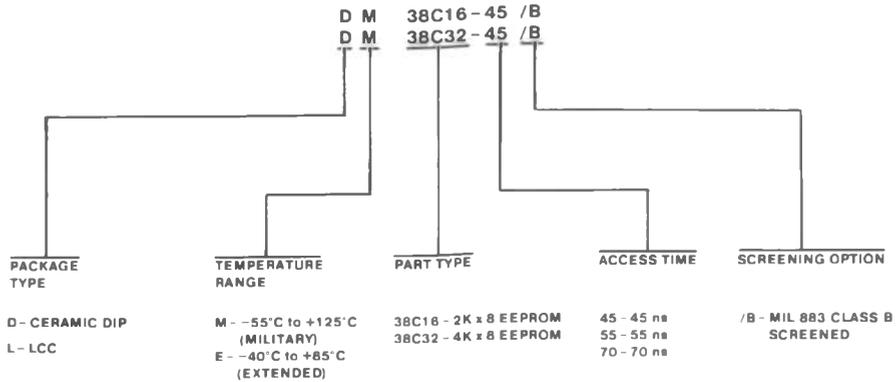
**$\overline{CE}$  CONTROLLED WRITE CYCLE**



**NOTES:**

1. Address hold time is with respect to the falling edge of the control signal  $\overline{WE}$  or  $\overline{CE}$ .

**Ordering Information**



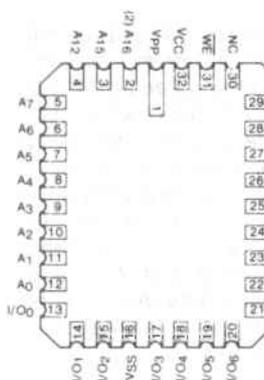
The "Preliminary Data Sheet" designation on a SEEQ data sheet indicates that the product is not fully characterized. The specifications are subject to change, are based on design goals or preliminary part evaluation, and are not guaranteed. SEEQ Technology or an authorized sales representative should be consulted for current information before using this product. No responsibility is assumed by SEEQ for its use, nor for any infringements of patents and trademarks or other rights of third parties resulting from its use. SEEQ reserves the right to make changes in specifications at any time and without notice.

## Features

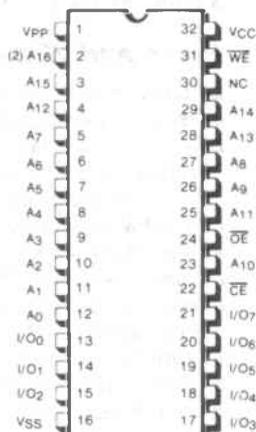
- 64K/128K Byte Writable non-volatile memory
- Low Power CMOS Process
- Electrical Chip and Block Erase
  - 7.5 Second Maximum Erase Time
- Electrical Byte Write
  - 1 ms. Maximum, 500  $\mu$ s typical
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- Flash™ EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
  - Minimum 100 Cycle Endurance
  - Optional 1000 Cycle Endurance Screening
  - Minimum 10 Year Data Retention
- 5V  $\pm$  10% V<sub>CC</sub>
- -55°C to +125°C Temperature Range (Reads)
- -55°C to +85°C Temperature Range (Erase/Write)
- Silicon Signature™ and DiTrace™
- Jedec Standard Byte Wide Pinout
  - 32 Pin D.I.P.
  - 32 Pin Ceramic Leadless Chip Carrier

## Pin Configuration

TOP VIEW  
LEADLESS CHIP CARRIER

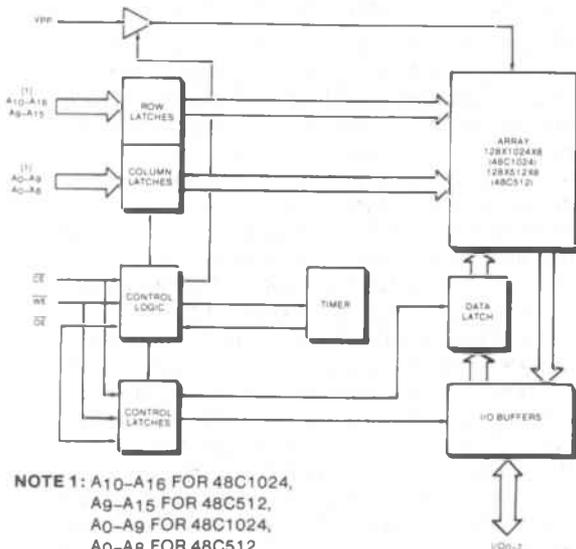


DUAL-IN-LINE  
TOP VIEW



MILITARY

## Block Diagram



NOTE 1: A<sub>10</sub>-A<sub>16</sub> FOR 48C1024,  
A<sub>9</sub>-A<sub>15</sub> FOR 48C512,  
A<sub>0</sub>-A<sub>9</sub> FOR 48C1024,  
A<sub>0</sub>-A<sub>8</sub> FOR 48C512

NOTE 2: PIN 2 IS N.C. ON THE 48C512

SILICON SIGNATURE™, FLASH™ and DiTRACE™ are registered trademarks of SEEQ Technology.

## Pin Names

A <sub>0</sub> -A <sub>8</sub>	COLUMN ADDRESS INPUT (48C512)
A <sub>0</sub> -A <sub>9</sub>	COLUMN ADDRESS INPUT (48C1024)
A <sub>9</sub> -A <sub>15</sub>	ROW ADDRESS INPUT (48C512)
A <sub>10</sub> -A <sub>16</sub>	ROW ADDRESS INPUT (48C1024)
CE	CHIP ENABLE
OE	OUTPUT ENABLE
WE	WRITE ENABLE
I/O <sub>0</sub> -7	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V <sub>PP</sub>	WRITE/ERASE INPUT VOLTAGE

### Description

The M48C512 and M48C1024 are 512 Kbit and 1024 Kbit CMOS Flash EEPROMS organized as 64K x 8 and 128K x 8 bits. Built using Seeq's proprietary Flash EEPROM single transistor memory cell, they feature input latches on address and data inputs for both erasing and writing, chip erase and block erase capability and a fast byte write. Endurance, the number of times a byte can be written, is specified as 100 with an optional screen to 1000 cycles.

### Read

Reading is accomplished by presenting a valid address with chip enable and output enable at  $V_{IL}$ , write enable at  $V_{IH}$ , and  $V_{PP}$  at any level. See timing waveforms for A.C. parameters.

### Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected; a pulse of less than 20 ns. will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

### Block Erase

Block erase erases all bits in a block of the array to a logical one. It requires that the  $V_{PP}$  pin be brought to a high voltage and a write cycle performed. The block to be erased is defined by address inputs  $A_9$  through  $A_{15}$  for the 48C512 and  $A_{10}$  through  $A_{16}$  for the 48C1024. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time  $T_{abort}$  to allow aborting the erase by writing again. This permits recovering from an unintentional block erase if, for example, in loading a block of data a byte of 'FF' was written. After the  $T_{abort}$  delay the block erase will begin. The erase is accomplished by following the erase algorithm in figure 2.  $V_{PP}$  can be brought to any TTL level or left at high voltage after the erase.

### Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm.  $V_{PP}$  can be brought to any TTL level or left at high voltage after the erase.

### Block and Chip Erase Algorithm

To reduce the block and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the block erase and chip erase flow charts.

### Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either block erase or chip erase.

Data are organized in these Flash EEPROMs in a group of bytes called a block. There are 128 blocks in both the 48C512 and the 48C1024. A block, which is 512 bytes in the 48C512 and 1024 bytes in the 48C1024, is conceptually like a sector on a disk drive. Individual bytes must be written as part of a block write algorithm which is detailed in figure 1. This algorithm is designed to minimize the total time to write a block of data.

Blocks are written by applying a high voltage to the  $V_{PP}$  pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of  $t_{WC}$  ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. Following each loop, a read-verification is done. If any bytes do not verify, another write loop is performed. When all bytes read correctly, additional loops are performed to insure adequate bit cell margin. The total number of loops will vary by device and depends on temperature; low temperature reduces the number of loops required. For example, a typical (room temperature) loop count is 4. Blocks need not be written individually; the entire device or any combination of blocks can be written using the write algorithm.

Because bytes can only be written as part of a block write, if data is to be added to a partially written block or one or more bytes in a block must be changed, the contents of the block must first be read into system RAM; the bytes can then be added to the block of data in RAM and the block written using the block write algorithm.

## Power Up/Down Protection

These two devices contain a  $V_{CC}$  sense circuit which disables internal erase and write operations when  $V_{CC}$  is below 3.5 volts. In addition, erases and writes are prevented when any control input (CE, OE, WE) is in the wrong state for writing or erasing (see mode table).

## High Voltage Input Protection

The  $V_{PP}$  pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1  $\mu$ f decoupling capacitor with good high frequency response connected from  $V_{PP}$  to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize  $V_{PP}$  voltage sag when a device goes from standby to a write or erase cycle.

## Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$V_{PP}$	$A_9-15$ $A_{10-16}$	$A_0-8$ $A_{0-9}$	$D_0-7$
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	Address	Address	$D_{OUT}$
Standby	$V_{IH}$	X	X	X	X	X	HI-Z
Byte write	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	Address	Address	$D_{IN}$
Chip erase select	$V_{IL}$	$V_{IH}$	$V_{IL}$	TTL	X	X	X
Chip erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	X	X	'FF'
Block erase	$V_{IL}$	$V_{IH}$	$V_{IL}$	$V_P$	Address	X	'FF'

## Absolute Maximum Stress Ratings

Temperature:

Storage.....  $-65^{\circ}\text{C}$  to  $+150^{\circ}\text{C}$

Under bias.....  $-65^{\circ}\text{C}$  to  $+135^{\circ}\text{C}$

All inputs except  $V_{PP}$  and

outputs with respect to  $V_{SS}$ ...  $+6\text{ V.}$  to  $-0.3\text{ V.}$

$V_{PP}$  pin with respect to  $V_{SS}$ ...  $14\text{ V.}$

## Silicon Signature™

A row of fixed ROM is present in the 48C512 and 48C1024 which contains the device's Silicon Signature™. Silicon Signature™ contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature™ is read by raising address  $A_9$  to  $12 \pm 0.5\text{ V.}$  and bringing all other address inputs plus chip enable and output enable to  $V_{IL}$  with  $V_{CC}$  at 5 V. The two Silicon Signature™ bytes are selected by address input  $A_0$ . Silicon Signature™ is functional at room temperature only (25 C.)

## Silicon Signature™ Bytes

	$A_0$	Data (Hex)
Seeq Code	$V_{IL}$	94
Product code (48C512)	$V_{IH}$	1A
Product code (48C1024)	$V_{IH}$	1C

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## Recommended Operating Conditions

	M48C512/ M48C1024
$V_{CC}$ supply voltage	$5\text{ V} \pm 10\%$
Temperature range (for reads)	$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$ (case temp.)
Temperature range (for writes and erases)	$-55^{\circ}\text{C}$ to $85^{\circ}\text{C}$ (case temp.)

### DC Operating Characteristics

Over the  $V_{CC}$  and temperature range

Symbol	Parameter	Limits			Test Condition
		Min.	Max.	Unit	
$I_{IH}$	Input leakage high		1	$\mu A$	$V_{IN} = V_{CC}$
$I_{IL}$	Input leakage low		-1	$\mu A$	$V_{IN} = 0.1 V$
$I_{OL}$	Output leakage		10	$\mu A$	$V_{IN} = V_{CC}$
$V_P$	Program/erase voltage	11.5	12.5	V	
$V_{PR}$	$V_{PP}$ voltage during read	0	$V_P$	V	
$I_{PP}$	$V_P$ current				
	Standby mode		200	$\mu A$	$\overline{CE} = V_{IH}, V_{PP} = V_P$
	Read mode		200	$\mu A$	$\overline{CE} = V_{IL}, V_{PP} = V_P$
	Byte write		40	mA	$V_{PP} = V_P$
	Erase		60	mA	$V_{PP} = V_P$
$I_{CC1}$	Standby $V_{CC}$ current		200	$\mu A$	$\overline{CE} = V_{CC} - .3$
$I_{CC2}$	Standby $V_{CC}$ current		5	mA	$\overline{CE} = V_{IH} \text{ min.}$
$I_{CC3}$	Active $V_{CC}$ current		80	mA	$\overline{CE} = V_{IL}$
$V_{IL}$	Input low voltage	-0.3	0.8	V	
$V_{IH}$	Input high voltage	2.0	$V_{CC} + .3$	V	
$V_{OL}$	Output low voltage		0.45	V	$I_{OL} = 2.1 \text{ mA}$
$V_{OH1}$	Output level (TTL)	2.4		V	$I_{OH} = -400 \mu A$
$V_{OH2}$	Output level (CMOS)	$V_{CC} - .4$		V	$I_{OH} = -100 \mu A$

### AC Test Conditions

Output load: 1 TTL gate and  $C(\text{load}) = 100 \text{ pf}$ .

Input rise and fall times:  $< 20 \text{ ns}$ .

Input pulse levels: 0.45 V to 2.4 V

Timing measurement reference level:

Inputs 1 V and 2 V

Outputs 0.8 V and 2 V

#### NOTE:

In A.C. characteristics all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a **minimum** time; the user must provide a valid state on that input or wait for the stated minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a **maximum** time, the device will perform the operation within the stated time.

Advance Data Sheets contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

## E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V <sub>ZAP</sub>	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note: Characterization data — not tested.

## Capacitance<sup>[1]</sup> T<sub>A</sub>=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C <sub>IN</sub>	Input capacitance	6 pf.	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	Output capacitance	12 pf.	V <sub>I/O</sub> = 0 V

Note 1: This parameter is only sampled and not 100% tested.

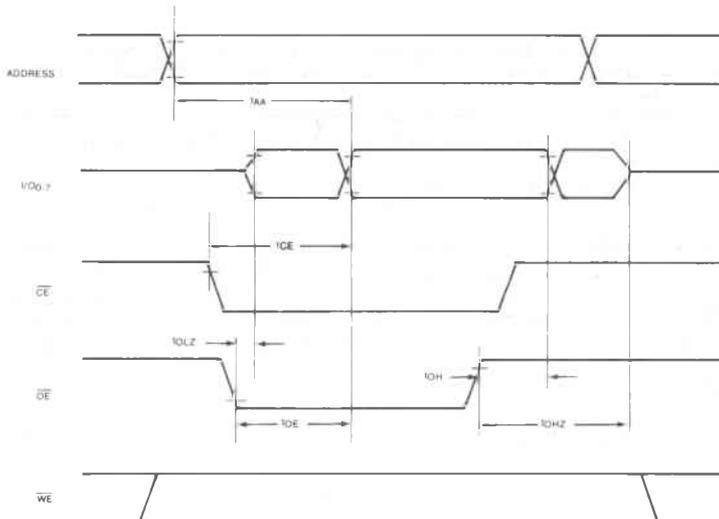
## AC Characteristics

(over the V<sub>CC</sub> and temperature range)

### READ

Symbol	Parameter	48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	
t <sub>RC</sub>	Read cycle time	250		300		ns
t <sub>AA</sub>	Address to data		250		300	ns
t <sub>CE</sub>	$\overline{CE}$ to data		250		300	ns
t <sub>OE</sub>	$\overline{OE}$ to data		100		150	ns
t <sub>DF</sub>	$\overline{OE}/\overline{CE}$ to data float		60		80	ns
t <sub>OH</sub>	Output hold time	0		0		ns

### Read Timing



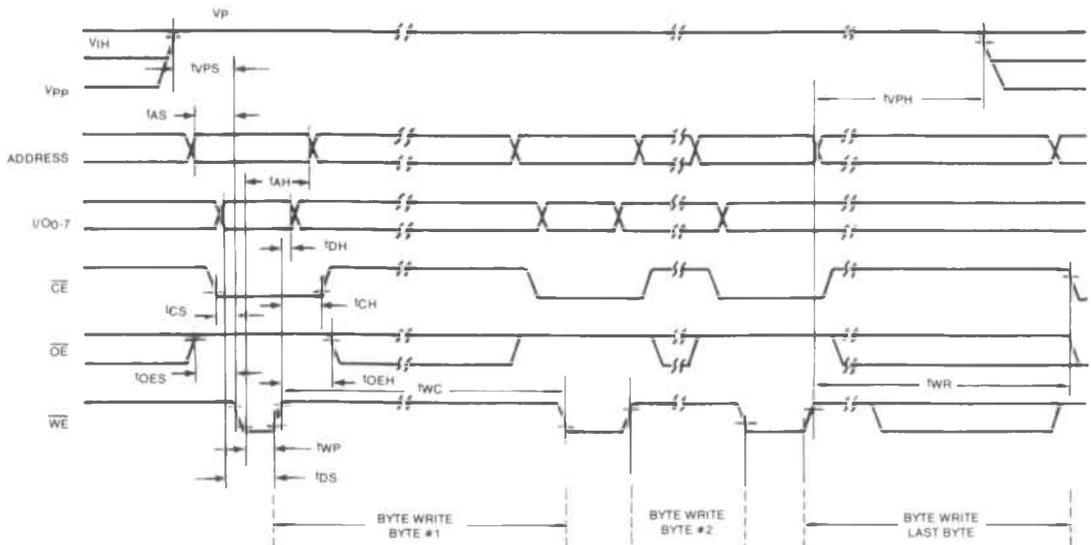
## AC Characteristics

(over the  $V_{CC}$  and temperature range)

## BYTE WRITE

Symbol	Parameter	48CXXX -250		48CXXX -300		Unit
		Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		$\mu S$
$t_{VPH}$	$V_{PP}$ hold time	250		250		$\mu S$
$t_{CS}$	$\overline{CE}$ setup time	0		0		ns
$t_{CH}$	$\overline{CE}$ hold time	0		0		ns
$t_{OES}$	$\overline{OE}$ setup time	10		10		ns
$t_{OEH}$	$\overline{OE}$ hold time	10		10		ns
$t_{AS}$	Address setup time	20		20		ns
$t_{AH}$	Address hold time	100		100		ns
$t_{DS}$	Data setup time	50		50		ns
$t_{DH}$	Data hold time	0		0		ns
$t_{WP}$	$\overline{WE}$ pulse width	100		100		ns
$t_{WC}$	Write cycle time	100	150	100	150	$\mu S$
$t_{WR}$	Write recovery time		1.5		1.5	ms

### Byte Write Timing



## AC Characteristics

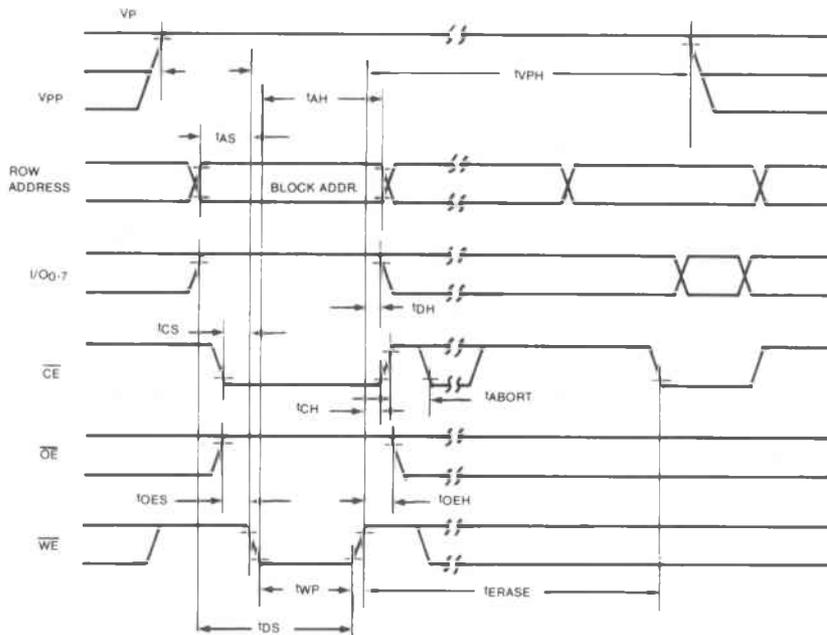
(over the  $V_{CC}$  and temperature range)

## BLOCK ERASE

Symbol	Parameter	48CXXX -250		48CXXX -300		Unit
		Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		$\mu s$
$t_{VPH}$	$V_{PP}$ hold time	500		500		ms
$t_{CS}$	$\overline{CE}$ setup time	0		0		ns
$t_{OES}$	$\overline{OE}$ setup time	0		0		ns
$t_{AS}$	Address setup time	20		20		ns
$t_{AH}$	Address hold time	100		100		ns
$t_{DS}$	Data setup time	50		50		ns
$t_{DH}$	Data hold time	0		0		ns
$t_{WP}$	$\overline{WE}$ pulse width	100		100		ns
$t_{CH}$	$\overline{CE}$ hold time	0		0		ns
$t_{OEH}$	$\overline{OE}$ hold time	0		0		ns
$t_{ERASE}$	Block erase time		500		500	ms
$t_{ABORT}$	Block erase delay		250		250	$\mu s$

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## Block Erase Timing



## AC Characteristics

(over the  $V_{CC}$  and temperature range)

## CHIP ERASE

Symbol	Parameter	48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	
$t_{VPS}$	$V_{PP}$ setup time	2		2		$\mu s$
$t_{VPH}$	$V_{PP}$ hold time	500		500		ms
$t_{CS}$	CE setup time	0		0		ns
$t_{OES}$	OE setup time	0		0		ns
$t_{DS}$	Data setup time	50		50		ns
$t_{DH}$	Data hold time	0		0		ns
$t_{WP}$	WE pulse width	100		100		ns
$t_{CH}$	CE hold time	0		0		ns
$t_{OEH}$	OE hold time	0		0		ns
$t_{ERASE}$	Chip erase time		500		500	ms

### Chip Erase Timing

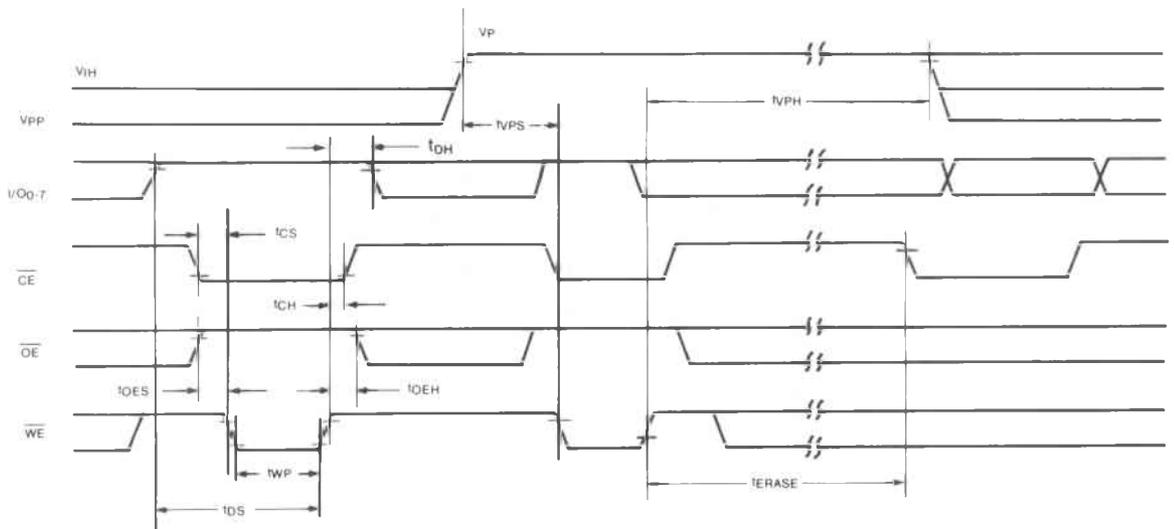
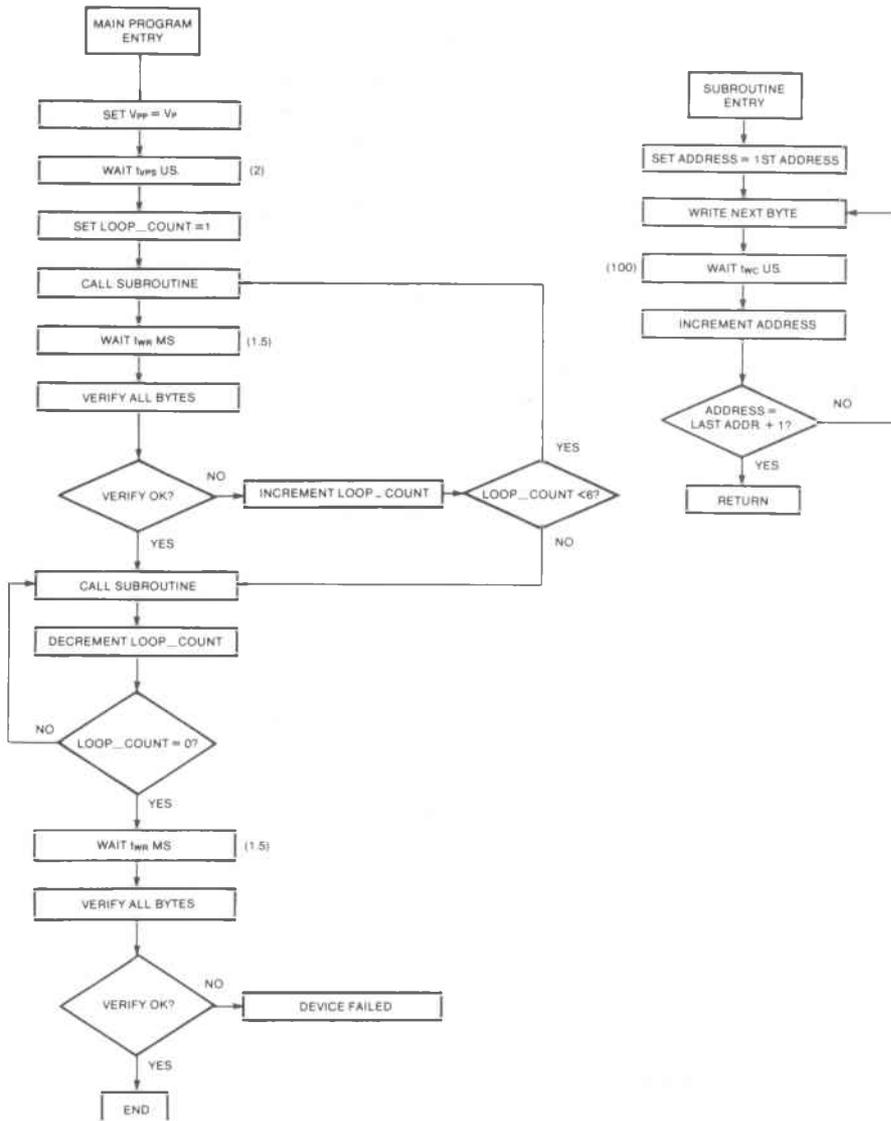
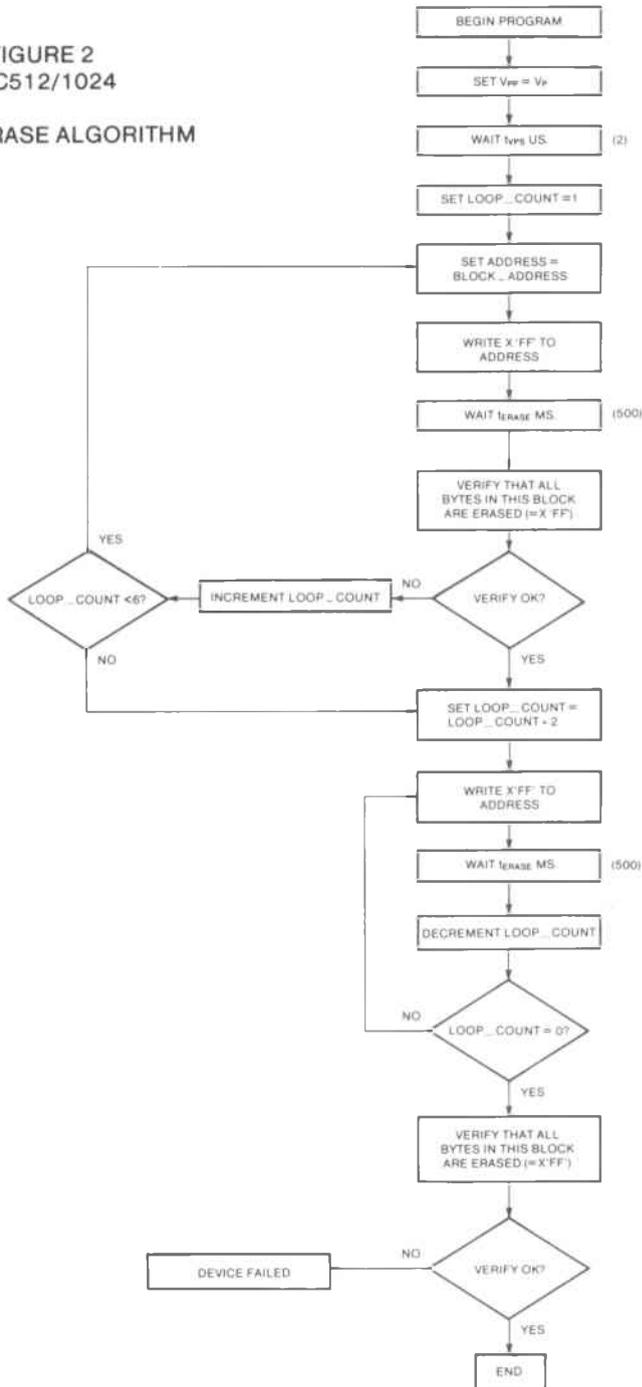


FIGURE 1  
48C512/1024 WRITE ALGORITHM

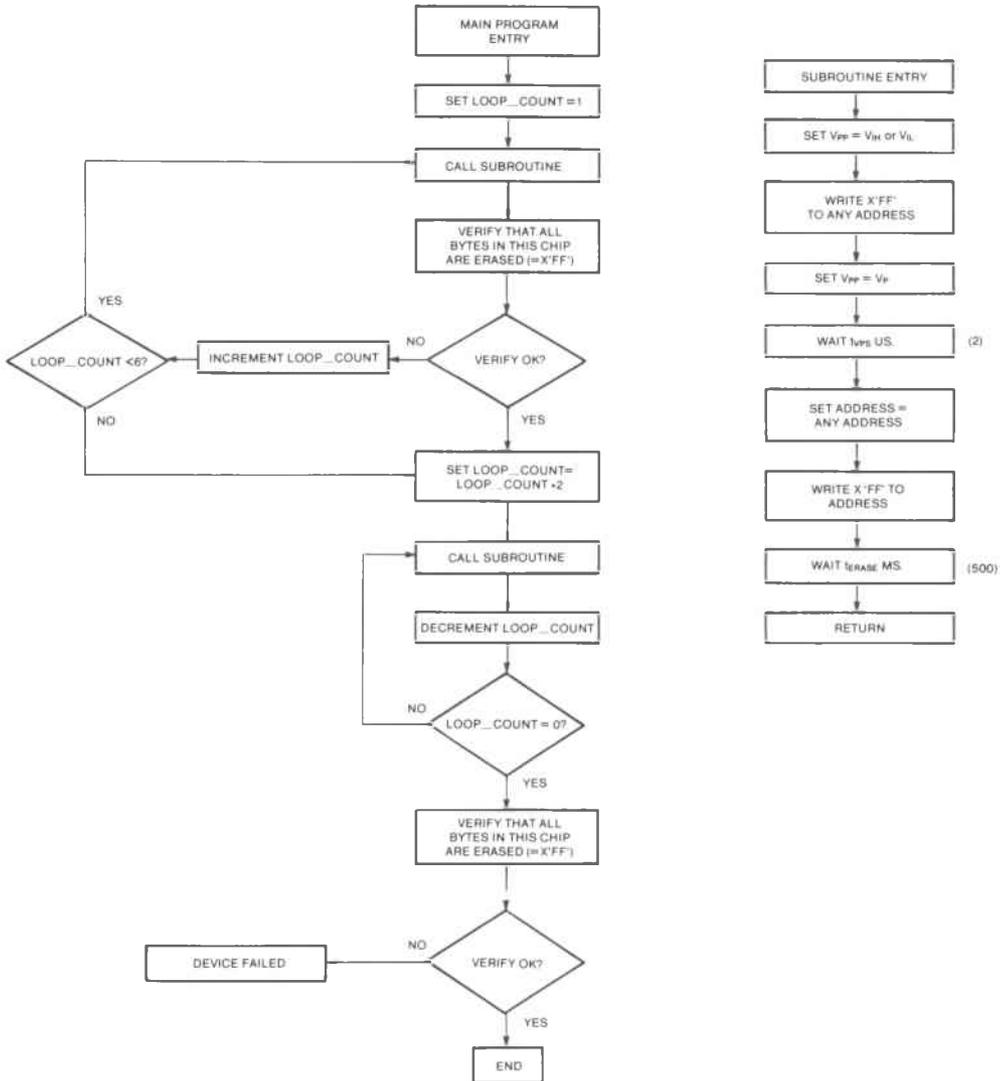


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**FIGURE 2**  
**48C512/1024**  
**BLOCK ERASE ALGORITHM**



**FIGURE 3**  
**48C512/1024**  
**CHIP ERASE ALGORITHM**



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### Features

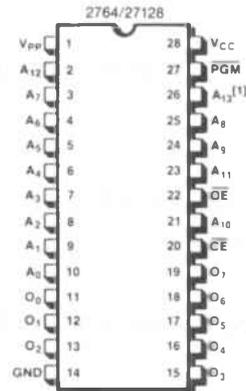
- **Military and Extended Temperature Range**
  - -55° to +125°C: M2764
  - -55° to +125°C: M27128
  - -40° to +85°C: E2764/E27128
- **200 ns Access Times at -55° to 125°C**
- **Programmed Using Intelligent Algorithm**
- **21 V V<sub>PP</sub> Programming Voltage**
- **JEDEC Approved Byte-wide Pin Configuration**
  - 2764 8K x 8 Organization
  - 27128 16K x 8 Organization
- **Low Power Dissipation**
  - 120 mA Active Current
  - 40 mA Standby Current
- **Silicon Signature™**

### Description

SEEQ's 2764 and 27128 are ultraviolet light erasable EPROMs which are organized 8K x 8 and 16K x 8 respectively. They are specified over the military and extended temperature range and have access times as fast as 200 ns over the V<sub>CC</sub> tolerance range. The access time is achieved without sacrificing power since the maximum active and standby currents are 120 mA and 40 mA respectively. The 200 ns allows higher system efficiency by eliminating the need for wait states in today's 8- or 16-bit microprocessors.

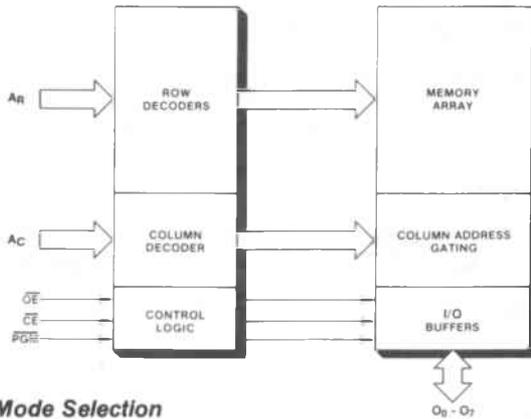
### Pin Configurations

DUAL-IN-LINE  
TOP VIEW



PIN 26 IS A NO CONNECT  
ON THE DIP 2764

### Block Diagram



### Mode Selection

MODE \ PINS	CE (20)	OE (22)	PGM (27)	V <sub>PP</sub> (1)	V <sub>CC</sub> (28)	Outputs (11-13, 15-19)
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>CC</sub>	V <sub>CC</sub>	DOUT
Output Disable	X	V <sub>IH</sub>	V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>	High Z
Standby	V <sub>IH</sub>	X	X	V <sub>CC</sub>	V <sub>CC</sub>	High Z
Program	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>PP</sub>	V <sub>CC</sub>	DIN
Program Verify	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>PP</sub>	V <sub>CC</sub>	DOUT
Program Inhibit	V <sub>IH</sub>	X	X	V <sub>PP</sub>	V <sub>CC</sub>	High Z
Silicon Signature**	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>CC</sub>	V <sub>CC</sub>	Encoded Data

X can be either V<sub>IL</sub> or V<sub>IH</sub>

\* For Silicon Signature™: A<sub>0</sub> is toggled, A<sub>6</sub> = 12V, and all other addresses are at TTL low.  
Silicon Signature™ is a registered trademark of SEEQ Technology.

### Pin Names

AC	ADDRESSES — COLUMN (LSB)
AR	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
O <sub>0</sub> - O <sub>7</sub>	OUTPUTS
PGM	PROGRAM

# M2764/M27128 E2764/E27128

Initially, and after erasure, all bits are in the "1" state. Data is programmed by applying 21 V to  $V_{PP}$  and a TTL "0" to pin 27 (program pin). They may be programmed with an intelligent algorithm that is now available on commercial programmers. This faster time improves manufacturing throughput time by hours over conventional 50 ms algorithms. Commercial programmers (e.g. Data I/O, Pro-log, Digelec, Kontron, and Stag) have implemented this fast algorithm for SEEQ's EPROMs. If desired, the 27128

and the 2764 may be programmed using the conventional 50 ms programming specification of older generation EPROMs.

Incorporated on the 27128 and 2764 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer, and programming information. This data is encoded in ROM to prevent erasure by ultraviolet light.

## Absolute Maximum Ratings

### Temperature

Storage ..... -65° C to +150° C

Under Bias ..... -65° C to +135° C

### All Inputs or Outputs with

Respect to Ground ..... +6V to -0.3V

### $V_{PP}$ During Programming with

Respect to Ground ..... +22V to -0.3V

### Voltage on $A_9$ with

Respect to Ground ..... +15.5V to -0.3V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	M2764 M27128	E2764 E27128
$V_{CC}$ Supply Voltage <sup>1)</sup>	5 V $\pm$ 10%	5 V $\pm$ 10%
Temperature Range (Read Mode)	(Case) -55° to 125° C	(Ambient) -40° to 85° C
$V_{PP}$ During Programming	21 $\pm$ 0.5 V	21 $\pm$ 0.5 V

## DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
$I_{IN}$	Input Leakage Current		10	$\mu$ A	$V_{IN} = V_{CC}$ Max.
$I_O$	Output Leakage Current		10	$\mu$ A	$V_{OUT} = V_{CC}$ Max.
$I_{PP}$ <sup>2)</sup>	$V_{PP}$ Current	Read Mode	5	mA	$V_{PP} = V_{CC}$ Max.
		Prog. Mode (25° C)	30	mA	$V_{PP} = 21.5V$
$I_{CC1}$ <sup>2)</sup>	$V_{CC}$ Standby Current		40	mA	$\overline{CE} = V_{IH}$
$I_{CC2}$ <sup>2)</sup>	$V_{CC}$ Active Current		120	mA	$\overline{CE} = \overline{OE} = V_{IL}$
$V_{IL}$	Input Low Voltage	-0.1	0.8	V	
$V_{IH}$	Input High Voltage	2	$V_{CC} + 1$	V	
$V_{OL}$	Output Low Voltage		0.45	V	$I_{OL} = 2.1$ mA
$V_{OH}$	Output High Voltage	2.4		V	$I_{OH} = -400$ $\mu$ A

### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- $V_{PP}$  may be connected directly to  $V_{CC}$  except during programming. The supply current is the sum of  $I_{CC}$  and  $I_{PP}$ .

# M2764/M27128 E2764/E27128

## AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)								Test Conditions
		E/M2764-20 E/M27128-20		E/M2764-25 E/M27128-25		E/M2764-35 E/M27128-35		M2764-45		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{AA}$	Address Access Time		200		250		350		450	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid		200		250		350		450	$\overline{OE} = V_{IL}$
$t_{OE}^{[2]}$	Output Enable to Data Valid		75		100		125		150	$\overline{CE} = V_{IL}$
$t_{DF}^{[3]}$	Output Enable to Output Float	0	60	0	85	0	105	0	130	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Chip Enable, Addresses, or Output Enable, whichever occurred first	0		0		0		0		$\overline{CE} = \overline{OE} = V_{IL}$

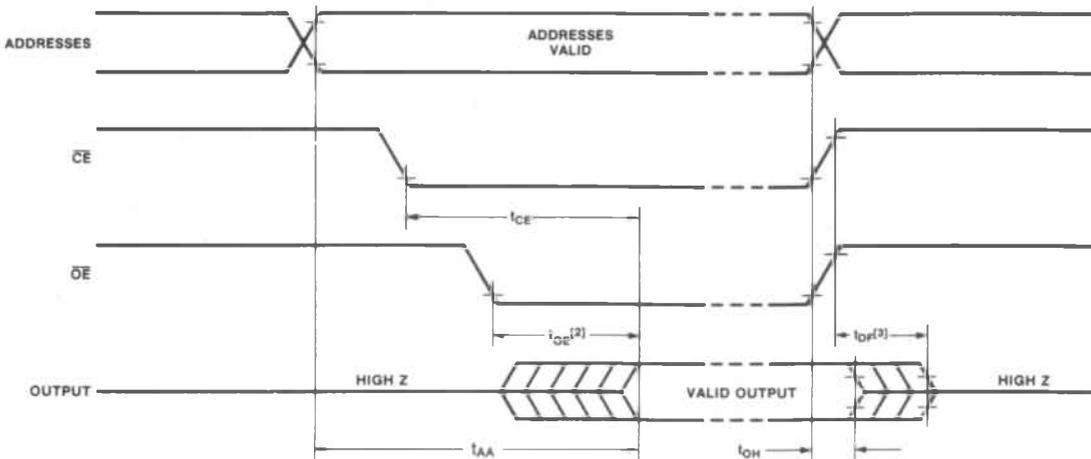
### Capacitance<sup>[1]</sup>

Symbol	Parameter	Typ.	Max.	Unit	Conditions
$C_{IN}$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

### Equivalent A.C. Test Conditions<sup>[4]</sup>

Output Load: 1 TTL gate and  $C_L = 100\text{ pF}$   
 Input Rise and Fall Times:  $\leq 20\text{ ns}$   
 Input Pulse Levels: 0.45V to 2.4V  
 Timing Measurement Reference Level:  
 Inputs 1V and 2V  
 Outputs 0.8V and 2V

### A.C. Waveforms



#### NOTES:

1. THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
2.  $\overline{OE}$  MAY BE DELAYED TO  $t_{AA} - t_{OE}$  AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON  $t_{AA}$ .
3.  $t_{DF}$  IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$ , WHICHEVER OCCURS FIRST.
4. THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

# M2764/M27128 E2764/E27128

## Erasure Characteristics

The 2764 and 27128 are erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm<sup>2</sup>. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm <sup>2</sup> )	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

## Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. Silicon Signature allows programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds programming.

Silicon Signature is activated by raising address A<sub>9</sub> to 12V ± 0.5V, bringing chip enable and output enable to a TTL low, having V<sub>CC</sub> at 5V, and having all addresses except A<sub>0</sub> at a TTL low. The Silicon Signature data is then accessed by toggling (using TTL) the column address A<sub>0</sub>. There are 2 bytes of data available. The data (see Table 2) appears on outputs O<sub>0</sub> to O<sub>6</sub>, with O<sub>7</sub> used as an odd parity bit. This mode is functional at 25° ± 5°C ambient temperature.

Table 2. Silicon Signature Bytes

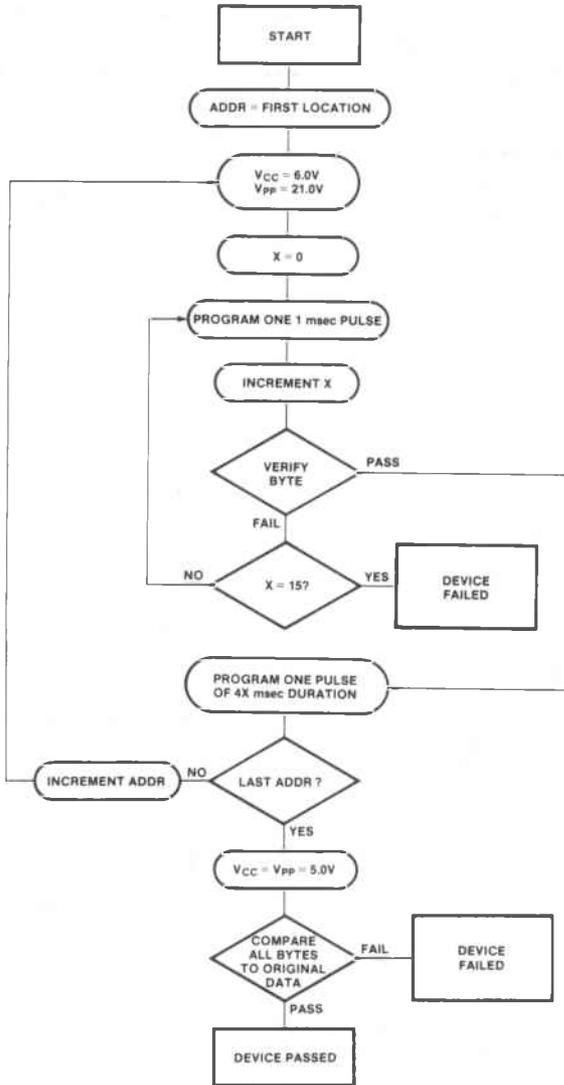
	A <sub>0</sub>	Data (Hex)
SEEQ Code (Byte 0)	V <sub>IL</sub>	94
Product Code (Byte 1)	V <sub>IH</sub>	40
	V <sub>IH</sub>	C1

## Programming

The EPROMs may be programmed using an intelligent algorithm or with a conventional 50 msec programming pulse. The intelligent algorithm improves the total programming time by approximately 10 times over the conventional 50 msec algorithm.

The intelligent algorithm requires V<sub>CC</sub> = 6V and V<sub>PP</sub> = 21V during byte programming. The initial program pulse width is one millisecond, followed by a sequence of one millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 4 times the number of one millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A maximum of 15 one millisecond pulses per byte should be applied to each address. When the intelligent algorithm cycle has been completed, all bytes must be read at V<sub>CC</sub> = V<sub>PP</sub> = 5V.

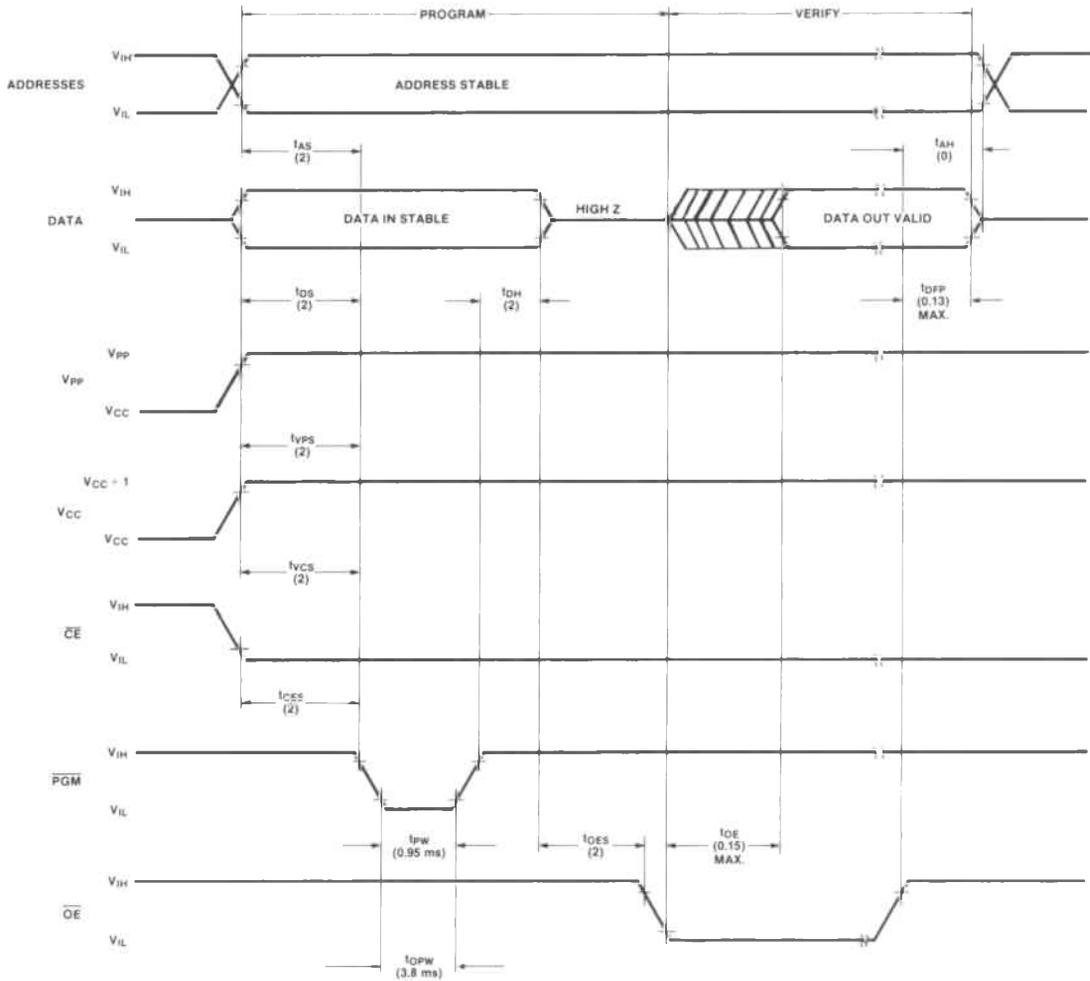
Intelligent Algorithm Flowchart



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# M2764/M27128 E2764/E27128

## Intelligent Algorithm



### NOTES:

1. ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN  $\mu$ SEC UNLESS OTHERWISE SPECIFIED.
2. THE INPUT TIMING REFERENCE LEVEL IS .8V FOR A  $V_{IL}$  AND 2V FOR A  $V_{IH}$ .
3.  $t_{OE}$  AND  $t_{DPP}$  ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.

# M2764/M27128 E2764/E27128

## Intelligent Algorithm

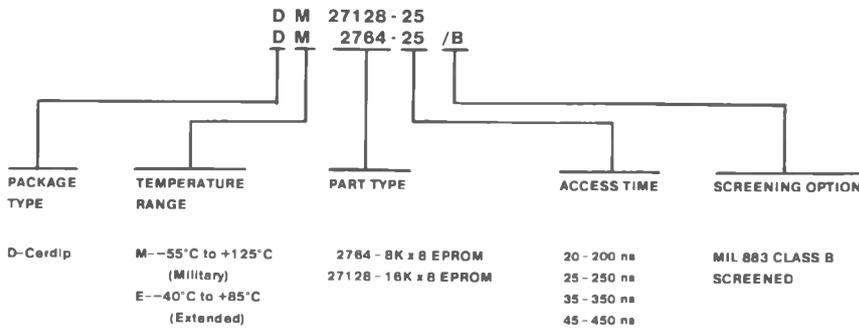
**AC Programming Characteristics**  $T_A = 25^\circ \pm 5^\circ\text{C}$ ,  $V_{CC}^{(1,4)} = 6.0\text{V} \pm 0.25\text{V}$ ,  $V_{PP} = 21\text{V} \pm 0.5\text{V}$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>AS</sub>	Address Setup Time	2			μs
t <sub>OES</sub>	OE Setup Time	2			μs
t <sub>DS</sub>	Data Setup Time	2			μs
t <sub>AH</sub>	Address Hold Time	0			μs
t <sub>DH</sub>	Data Hold Time	2			μs
t <sub>DFP</sub>	Output Enable to Output Float Delay	0		130	ns
t <sub>VPS</sub>	V <sub>PP</sub> Setup Time	2			μs
t <sub>VCS</sub>	V <sub>CC</sub> Setup Time	2			μs
t <sub>PW</sub> <sup>(2)</sup>	PGM Initial Program Pulse Width	0.95	1.0	1.05	ms
t <sub>OPW</sub> <sup>(3, 4)</sup>	PGM Overprogram Pulse Width	3.8		63	ms
t <sub>CES</sub>	CE Setup Time	2			μs
t <sub>OE</sub>	Data Valid from OE			150	ns

### NOTES:

- V<sub>CC</sub> must be applied simultaneously or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.
- Initial Program Pulse width tolerance is 1 msec ± 5%.
- The length of the overprogram pulse will vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
- For 50 ms programming, V<sub>CC</sub> = 5 V ± 5%, T<sub>PW</sub> = 50 ms ± 10%, and T<sub>OPW</sub> is not applicable.

## Ordering Information

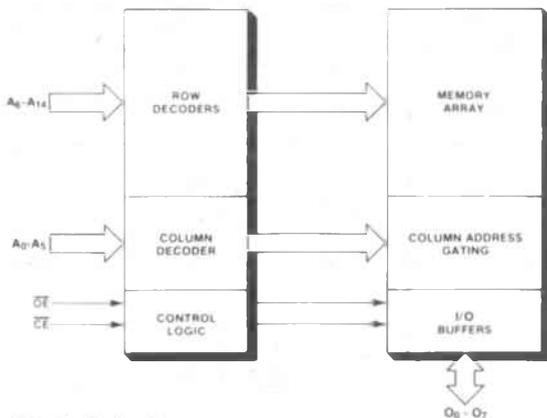




## Features

- 256K (32K x 8) CMOS EPROM
- Military and Extended Temperature Range
  - -55° to +125°C: M27C256
  - -40° to +85°C: E27C256
- Ultra Low Power
  - 150  $\mu$ A Max.  $V_{CC}$  Standby Current
  - 50 mA Max. Active Current
- Programmed Using Intelligent Algorithm
  - 12.5 V  $V_{pp}$
- 250 ns Access Times
- 5 V  $\pm$ 10%  $V_{CC}$
- JEDEC Approved Byte-wide Pin Configuration
- Silicon Signature™

## Block Diagram



## Mode Selection

MODE \ PINS	CE (20)	OE (22)	$V_{pp}$ (1)	$V_{CC}$ (28)	Outputs (11-13, 15-19)
Read	$V_{IL}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	DOUT
Output Disable	X	$V_{IH}$	$V_{CC}$	$V_{CC}$	High Z
Standby	$V_{IH}$	X	$V_{CC}$	$V_{CC}$	High Z
Program	$V_{IL}$	$V_{IH}$	$V_{pp}$	$V_{CC}$	DIN
Program Verify	$V_{IH}$	$V_{IL}$	$V_{pp}$	$V_{CC}$	DOUT
Program Inhibit	$V_{IH}$	$V_{IH}$	$V_{pp}$	$V_{CC}$	High Z
Silicon Signature™*	$V_{IL}$	$V_{IL}$	$V_{CC}$	$V_{CC}$	Encoded Data

X can be either  $V_{IL}$  or  $V_{IH}$ .

\* For Silicon Signature™  $A_0$  is toggled,  $A_9 = 12V$ , and all other addresses are at a TTL low.

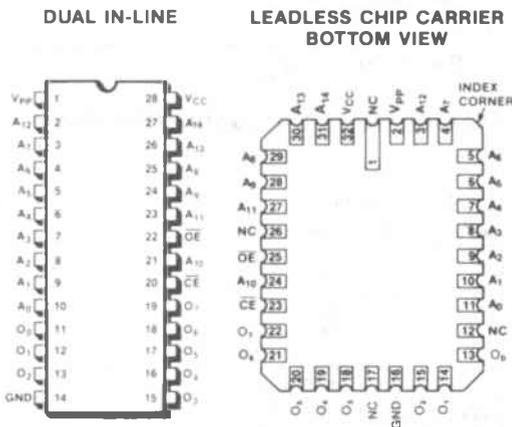
Silicon Signature™ is a registered trademark of SEEQ Technology.

## Description

SEEQ's 27C256 is the industry's first 256K CMOS EPROM. It has a 32K x 8 organization and has very low power dissipation. Its active current is less than one half the active power of n-channel EPROMs. In addition the standby current is orders of magnitude lower than those same EPROMs. Consequently, system memory sizes can be substantially increased at a very small increase in power. Low active and standby power is important in applications which require portability, low cooling cost, high memory bit density, and long term reliability.

The 27C256 is specified over both the extended and military temperature ranges at 5 V  $\pm$ 10%  $V_{CC}$ . The access time is specified at 250 ns, making the 27C256 compatible with most of today's microprocessors. Its inputs and outputs are completely TTL compatible.

## Pin Configuration



## Pin Names

$A_0 - A_5$	ADDRESSES — COLUMN LSB
$A_6 - A_{14}$	ADDRESSES — ROW
CE	CHIP ENABLE
OE	OUTPUT ENABLE
$O_0 - O_7$	OUTPUTS
NC	NO CONNECT

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# M27C256 E27C256

Initially, and after erasure, all bits are in the "1" state. An intelligent algorithm is used to program the 27C256 typically in four minutes. Data is programmed using a 12.5 V  $V_{PP}$  and an initial chip enable pulse of 1.0 ms.

Incorporated on the 27C256 is Silicon Signature™. Silicon Signature contains encoded data which identifies SEEQ as the EPROM manufacturer and gives the product code. This data is encoded in ROM to prevent erasure by ultraviolet light.

## Absolute Maximum Ratings

### Temperature

Storage ..... -65°C to +150°C

M27C256 Under Bias ..... -65°C to +135°C

E27C256 Under Bias ..... -50°C to +95°C

### All Inputs or Outputs with

Respect to Ground ..... +6 V to -0.3 V

$V_{PP}$  with Respect to Ground ..... +14.0 V to -0.3 V

Voltage on  $A_9$  with

Respect to Ground ..... +14.0 V to -0.3 V

\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Recommended Operating Conditions

	M27C256-25, M27C256-30	E27C256-25, E27C256-30
$V_{CC}$ Supply Voltage <sup>[1]</sup>	5 V ± 10%	5 V ± 10%
Temperature Range (Read Mode)	(Case) -55°C to +125°C	(Ambient) -40°C to 85°C
$V_{PP}$ During Read <sup>[2]</sup>	$V_{CC}$	$V_{CC}$
$V_{PP}$ During Programming <sup>[3]</sup>	12.5 ± 0.3 V	12.5 ± 0.3 V

## DC Operating Characteristics During Read or Programming

Symbol	Parameter	Limits		Unit	Test Condition
		Min.	Max.		
$I_{IN}^{[4]}$	Input leakage		1	$\mu A$	$V_{IN}=V_{CC}$ Max.
$I_{O}^{[5]}$	Output leakage		10	$\mu A$	$V_{OUT}=V_{CC}$ Max.
$I_{PP}$	$V_{PP}$ current:				
	Standby mode		150	$\mu A$	$\overline{CE}=V_{CC}-1$ v. min.
	Read Mode		1	mA	F=5 MHz, $\overline{CE}=V_{IL}$
	Programming mode		30	mA	$V_{PP}=12.5$ v.
$I_{CC1}$	$V_{CC}$ standby current		150	$\mu A$	$\overline{CE} \geq V_{CC}-1$ v.
$I_{CC2}$	$V_{CC}$ standby current		2	mA	$\overline{CE}=V_{IH}$
$I_{CC3}$	$V_{CC}$ active current		50	mA	$\overline{CE}=\overline{OE}=V_{IL}$ , $O_0-\gamma=0$ , F=5 MHz
$V_{IL}$	Input low voltage	-0.1	0.8	V	
$V_{IH}$	Input high voltage	2.0	$V_{CC} + 1$	V	
$V_{OL}$	Output low voltage		0.45	V	$I_{OL}=2.1$ ma.
$V_{OH}$	Output high voltage	2.4		V	$I_{OH}=-400$ $\mu A$ .

### NOTES:

1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
2.  $V_{PP}$  cannot be left floating and should be connected to  $V_{CC}$  during read.
3. 0.1  $\mu F$  ceramic capacitor on  $V_{PP}$  is required during programming only, to suppress voltage transients.
4. Inputs only. Does not include I/O.
5. For I/O only.

# M27C256 E27C256

## AC Operating Characteristics During Read

Symbol	Parameter	Limits (nsec)				Test Conditions
		M27C256-25 E27C256-25		M27C256-30 E27C256-30		
		Min.	Max.	Min.	Max.	
$t_{AA}$	Address Access Time		250		300	$\overline{CE} = \overline{OE} = V_{IL}$
$t_{CE}$	Chip Enable to Data Valid		250		300	$\overline{OE} = V_{IL}$
$t_{OE}^{[2]}$	Output Enable to Data Valid		100		120	$\overline{CE} = V_{IL}$
$t_{DF}^{[3]}$	Output Enable or Chip Enable to Output Float		60		105	$\overline{CE} = V_{IL}$
$t_{OH}$	Output Hold from Chip Enable, Addresses, or Output Enable whichever occurred first	0		0		$\overline{CE} = \overline{OE} = V_{IL}$

## Capacitance<sup>[1]</sup>

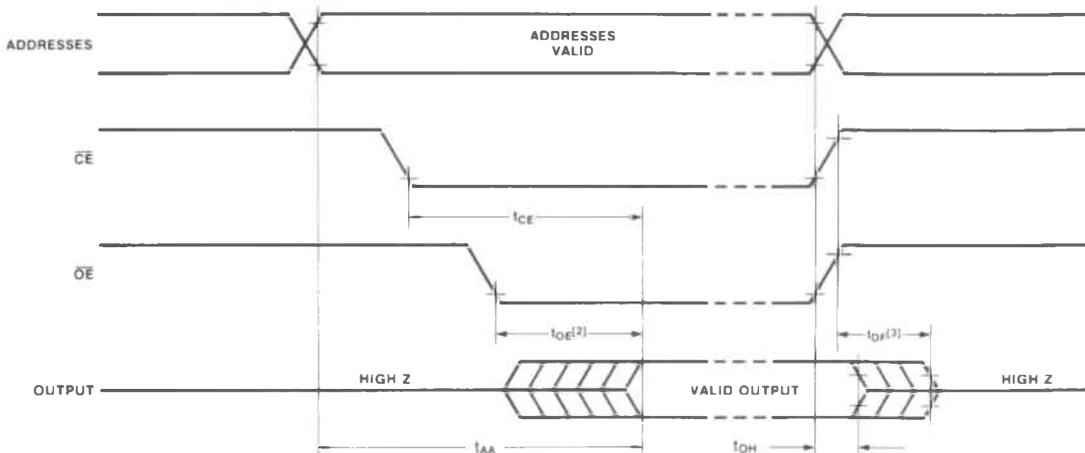
Symbol	Parameter	Typ.	Max.	Unit	Conditions
$C_{IN}$	Input Capacitance	4	6	pF	$V_{IN} = 0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT} = 0V$

## Equivalent A.C. Test Conditions<sup>[4]</sup>

Output Load: 1 TTL gate and  $C_L = 100$  pF  
 Input Rise and Fall Times:  $\leq 20$  ns  
 Input Pulse Levels: 0.45V to 2.4V  
 Timing Measurement Reference Level:  
 Inputs 1V and 2V  
 Outputs 0.8V and 2V

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## A.C. Waveforms



### NOTES:

- THIS PARAMETER IS SAMPLED AND IS NOT 100% TESTED.
- $\overline{OE}$  MAY BE DELAYED TO  $t_{AA} - t_{OE}$  AFTER THE FALLING EDGE OF  $\overline{CE}$  WITHOUT IMPACT ON  $t_{AA}$ .
- $t_{DF}$  IS SPECIFIED FROM  $\overline{OE}$  OR  $\overline{CE}$  WHICHEVER OCCURS FIRST.
- THESE ARE EQUIVALENT TEST CONDITIONS AND ACTUAL TEST CONDITIONS ARE DEPENDENT ON THE TESTER.

# M27C256 E27C256

## Erasure Characteristics

The 27C256 is erased using ultraviolet light which has a wavelength of 2537 Angstroms. The integrated dose, i.e., intensity x exposure time, for erasure is a minimum of 15 watt-second/cm<sup>2</sup>. The EPROM should be placed within one inch of the lamp tube during erasure. Table 1 shows the typical EPROM erasure time for various light intensities.

Table 1. Typical EPROM Erasure Time

Light Intensity (Micro-Watts/cm <sup>2</sup> )	Erasure Time (Minutes)
15,000	20
10,000	30
5,000	55

## Silicon Signature™

Incorporated in SEEQ's EPROMs is a row of mask programmed read only memory (ROM) cells which is outside of the normal memory cell array. The ROM contains the EPROM's Silicon Signature. Silicon Signature contains data which identifies SEEQ as the manufacturer and gives the product code. This data allow programmers to match the programming specification against the product which is to be programmed. If there is verification, then the programmer proceeds to program.

Silicon Signature is activated by raising address A<sub>9</sub> to

12V±0.5V, bringing chip enable and output enable to a TTL low, having V<sub>CC</sub> at 5V, and having all addresses except A<sub>0</sub> at a TTL low. The Silicon Signature data is then accessed by toggling A<sub>0</sub>. The data appears on outputs O<sub>0</sub> to O<sub>6</sub>, with O<sub>7</sub> used as an odd parity bit (see Table 2).

Table 2. Silicon Signature Bytes

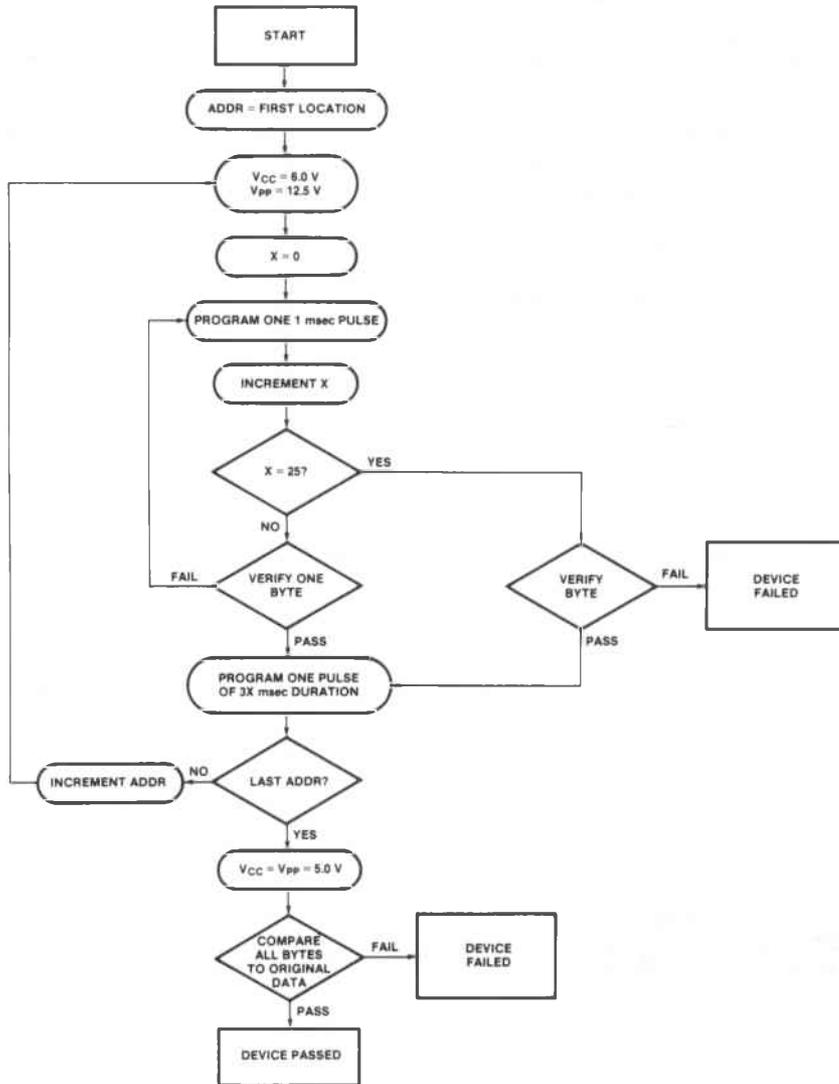
	A <sub>0</sub>	Data (Hex)
SEEQ Code (Byte 0)	V <sub>IL</sub>	94
Product Code (Byte 1)	V <sub>IL</sub>	C2

## Programming

The 27C256 is programmed using the industry standard intelligent algorithm.

The intelligent algorithm requires V<sub>CC</sub>=6 V and V<sub>PP</sub>=12.5 V during byte programming. The initial program pulse width is 1.0 millisecond, followed by a sequence of 1.0 millisecond pulses. A byte is verified after each pulse. A single program pulse, with a time duration equal to 3 times the number of 1.0 millisecond pulses applied, is additionally given to the address after it is verified as being correctly programmed. A minimum of one to a maximum of 25 1-ms pulses, plus one 3X over-pulse, may be applied to each byte. When the intelligent algorithm cycle has been completed, all bytes must be read at V<sub>CC</sub>=V<sub>PP</sub>=5 V.

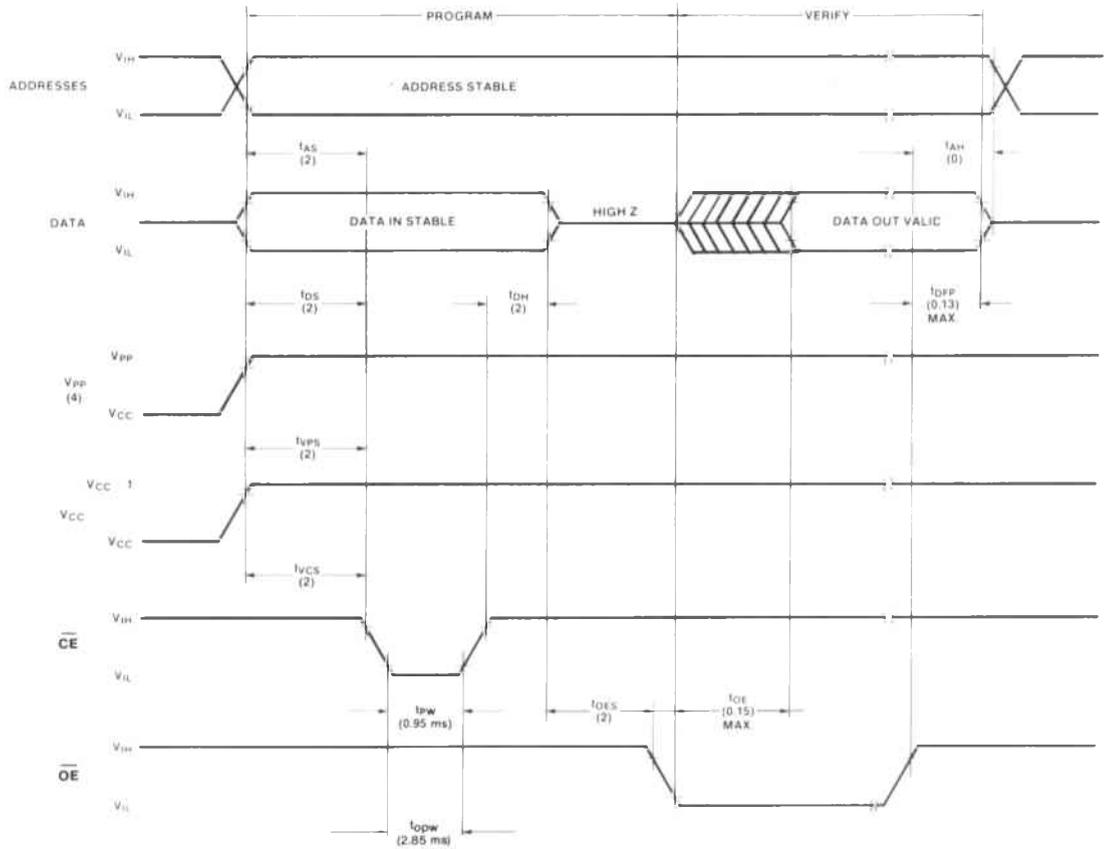
**Intelligent Algorithm Flowchart**



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# M27C256 E27C256

## Intelligent Algorithm



### NOTES:

- 1 ALL TIMES SHOWN IN ( ) ARE MINIMUM AND IN  $\mu\text{SEC}$  UNLESS OTHERWISE SPECIFIED.
- 2 THE INPUT TIMING REFERENCE LEVEL IS 0.8 V FOR A  $V_{IL}$  AND 2 V FOR A  $V_{IH}$ .
- 3  $t_{OE}$  AND  $t_{DPP}$  ARE CHARACTERISTICS OF THE DEVICE BUT MUST BE ACCOMMODATED BY THE PROGRAMMER.
- 4 0.1  $\mu\text{F}$  CERAMIC CAPACITOR ON  $V_{PP}$  IS REQUIRED DURING PROGRAMMING ONLY, TO SUPPRESS VOLTAGE TRANSIENTS.

# M27C256 E27C256

## Intelligent Algorithm

### AC Programming Characteristics $T_A = 25^\circ \pm 5^\circ\text{C}$ , $V_{CC}^{(1)} = 6.0\text{V} \pm 0.25\text{V}$ , $V_{PP} = 12.5\text{V}$

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{AS}$	Address Setup Time	2			$\mu\text{S}$
$t_{OES}$	$\overline{OE}$ Setup Time	2			$\mu\text{S}$
$t_{DS}$	Data Setup Time	2			$\mu\text{S}$
$t_{AH}$	Address Hold Time	0			$\mu\text{S}$
$t_{DH}$	Data Hold Time	2			$\mu\text{S}$
$t_{DFP}$	Output Enable to Output Float Delay	0		130	ns
$t_{VPS}$	$V_{PP}$ Setup Time	2			$\mu\text{S}$
$t_{VCS}$	$V_{CC}$ Setup Time	2			$\mu\text{S}$
$t_{PW}$	$\overline{CE}$ Initial Program Pulse Width	0.95	1.0	1.05	ms
$t_{OPW}^{(2)}$	$\overline{CE}$ Overprogram Pulse Width	2.85		78.75	ms
$t_{OE}$	Data Valid from $\overline{OE}$			150	ns

### AC Conditions of Test

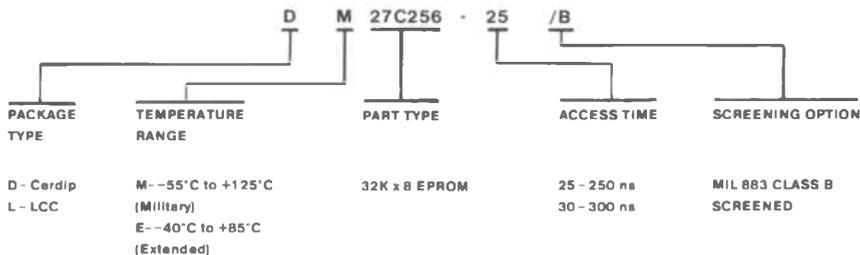
Input Rise and Fall Times (10% to 90%) . . . . . 20 ns  
 Input Pulse Levels . . . . . 0.45 V to 2.4 V  
 Input Timing Reference Level . . . . . 0.8 V and 2.0 V  
 Output Timing Reference Level . . . . . 0.8 V and 2.0 V

#### NOTES:

- $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
- The length of the overprogram pulse will vary from 2.85 msec to 78.75 msec as a function of the iteration counter value X.

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### Ordering Information





# 5

## ***RELIABILITY***

(Reliability Report)



# SEEQ EEPROM Reliability Report

## Introduction and Product Description

SEEQ offers a family of EEPROMs (Electrically Erasable Read Only Memories) which range in size from 4K to 256K bits in CMOS and NMOS technologies. They conform to the JEDEC configurations for byte wide memories. One family has internal input latches, a second family has internal input latches as well as a timer and a third with input latches, timer, and a page mode feature for fast write. New developments in process technology, circuit design techniques, and memory cell design combine to provide high performance from these EEPROMs that require only a single 5-volt power supply. SEEQ uses an innovative Q-Cell design on all its EEPROMs designed since 1983. The Q-Cell, combined with oxynitride in the tunnel dielectric, substantially improves the write/erase endurance of EEPROMs. This gives higher reliability to systems requiring infrequent writes (i.e., once a day for ten years) as well as to systems writing 5-10 times per day.

Programming the state of the memory cells (via the write and erase modes) is accomplished by charging and discharging a floating gate device via Fowler-Nordheim tunneling. This tunneling occurs through a proprietary oxynitride dielectric under the floating gate (see Figure 1). The use of oxynitride provides fast write/erase times at internal voltages that are 25% lower than those required for conventional oxide-only approaches due to a lower barrier height than thermal oxide. In addition, oxynitride provides lower charge trapping characteristics which gives improved write/erase endurance of each cell. The use of oxynitride in the dielectric area and SEEQ's proprietary Q-Cell design allows endurance to be specified up to 1,000,000 cycles/byte.

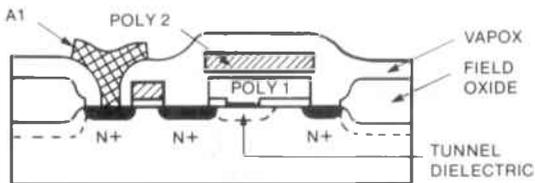


FIGURE 1. EEPROM N-MOS

## Memory Cell Operation

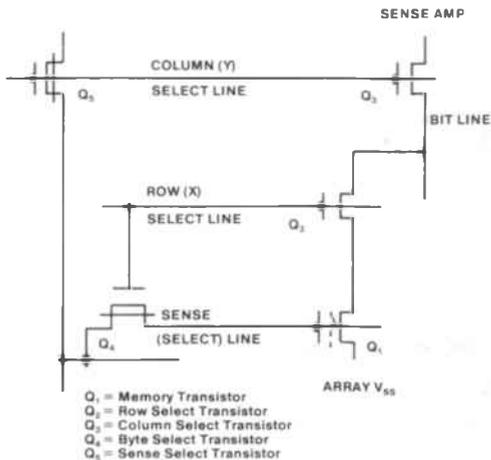
The SEEQ EEPROM Memory Cell consists of a MOS Floating Gate Memory Transistor and a Select Transistor. See the Device Cross Section in Figure 1 and schematic representation in Figure 2. The Memory Cell defines the Logic state, either a "1" or a "0", by storing negative or positive charge on the Floating Poly Silicon Gate (Poly 1 in Figure 1). When the reference voltage is applied to the top Poly Silicon Gate (Poly 2 in Figure 1), the Memory Cell will or will not conduct a current. This cell current is detected by the sense amplifier and transmitted to the output buffers as the appropriate Logic state.

Charge is transferred on and off the Floating Gate through the thin Oxynitride Tunnel Dielectric by Fowler-Nordheim Tunneling; (A Quantum Mechanical transmission mechanism of an electron penetrating through the energy bandgap for the thin oxide MOS structure). Fowler-Nordheim Tunneling occurs when a high voltage, typically 17-20 Volts, is placed across the Tunnel Dielectric region of the Memory Cell. This high voltage is generated internal to the device, the user need only to apply an external 5 Volt level.

For a Logic "1", electrons are stored on the Floating Gate; using the conditions defined For "erase." For a Logic "0", holes are stored on the Floating Gate; using the conditions defined for "write." The Memory Cells Thresholds for a Logic "1" and "0" are shown in Figure 3.

	Program	Erase	Read
Column	17V	5V	5V
Row	20V	20V	5V
Sense	0	20V	0
Bit	17V	0	2V
Array V <sub>SS</sub>	Floating	0	0
Floating Gate	-V <sub>p</sub>	+V <sub>E</sub>	
V <sub>T</sub>	<-5V	>+2V	
I Cell	40μA	0μA	

The select transistors are used to isolate the Memory Transistor in order to prevent data disturb. Memory cells and Peripheral Logic are combined to form the Q-Cell, which is a Memory Error Correction technique transparent to the user.



FLOATING GATE 85 ANGSTROMS OXY-NITRIDE

FIGURE 2. Generic EEPROM Memory Cell

Through the use of the proprietary Oxynitride process for the Tunnel Dielectric and use of the Q-Cell, SEEQ provides EEPROM's with typical data retention times of greater than 100 years, and Intrinsic Endurance Failure Rates of less than .03%/1000 cycles. Devices with a guaranteed Endurance of 1,000,000 cycles are possible.

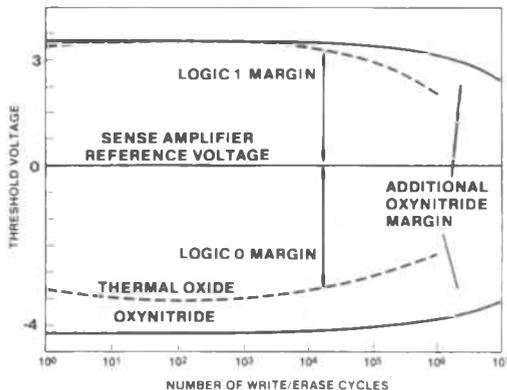


FIGURE 3. EEPROM Cell Margin Characteristics

## Static Life

"Static" refers to the D.C. bias of the cell periphery. Failure modes for static life include threshold shifts and leakages. The typical failure mechanisms are mobile ion contamination or trapped charges.

The "static" stress mode may be used either for screening or determining the long term reliability of the product

## Operating Life

The operating life of an EEPROM is limited by its general reliability which includes integrity of the peripheral circuitry as well as the memory cells. The operating life is characterized using a dynamic high temperature life stress.

Dynamic high temperature life stress is a standard approach used to evaluate the failure rate distribution of a product under accelerated conditions. The failure rate is statistically derived from the experimental results obtained at elevated temperatures, then extrapolated to typical operating temperature conditions. This extrapolation is accomplished using the Arrhenius relationship and an apparent activation energy consistent with the failure mechanisms observed. This acceleration technique works well for common causes of failure such as oxide defects, interconnect voids, and defective bonding.

For ease of calculation, the instantaneous failure rate is assumed to be constant throughout the lifetime of the product (i.e., the probability density function of the time to failure is assumed to be exponential).

Units to be stressed were drawn from finished goods inventory and written with a data pattern selected to program both logic states of "1" and "0" into locations in each row and each column of the array. Initial, intermediate, and final electrical testing of units was conducted at room temperature using a test program that checks parametrics, functionality and timing parameters.

The dynamic high temperature stress was applied in accordance with the conditions prescribed in MIL-STD-883, Method 1015, Condition D. Oven ambient temperature was maintained at 125 degrees C. The schematics are available upon request.

Table 1. Static Life Stress Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 125° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	324	324,000 hrs.	0	0.019%/1000 hrs.

The results are summarized in Table 2. The predictions use an assumed activation energy of  $E_a = 0.4$  eV for  $T_a = 55$  degrees C. The predicted charge gain failure rate is less than one-half the intrinsic failure rate of NMOS, as would be expected. This implies the field usage failure rate would be accurately predicted by dynamic life test.

### Data Retention Bake

Intrinsic data retention is defined as the ability to retain valid data over a prolonged period of time under storage conditions. At the cell level, data retention is a measure of the ability of the floating gate to retain charge in the absence of applied external gate bias. Data retention failures in a floating gate structure are commonly caused by dielectric defects and can be accelerated by high temperature bake stress. This characteristic provides a technique for both screening potentially defective product from the production flow as well as predicting expected retention lifetimes of outgoing product.

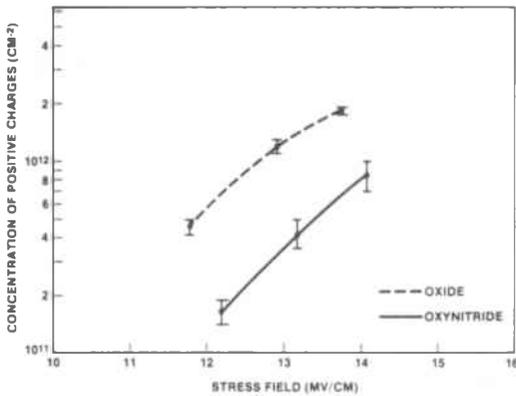


FIGURE 4. Comparison of Positive Charge Trapping at Tunneling-Dielectric/Si Interface.

In order to determine the data retention capability of SEEQ's products, unbiased devices are subjected to high temperature bake at 250 degrees C. The failure mode is a change in the state of the memory cell, and the typical failure mechanism is a dielectric defect resulting in "charge loss". Because dielectric defects can be induced by the electric fields generated during write/erase cycles, data retention and endurance are related topics. The effects of cycling on data retention are covered in the endurance section. In this section, the intrinsic data retention characteristics are evaluated and compared against the minimum data retention goal of ten years.

Units to be stressed are drawn from finished goods inventory and erased to an all 1's pattern (e.g., negative charge on floating gate). After erasing and initial testing, parts were temperature stressed at 250 degrees C. Voltage stress is not required for this evaluation; therefore, all leads are held at ground potential.

The results are summarized in Table 3. Using an activation energy of 0.6 eV, the data retention lifetime predicted by the data exceed 100 years at a 55 degrees C temperature. This period exceeds the industry 10 year standard for erasable memories.

### Endurance

Endurance is defined as the ability of an EEPROM to operate to data sheet specifications after repeated write/erase cycles to each byte. SEEQ specifies an endurance option of either 10,000 or 1,000,000 cycles/byte. The extraordinary high endurance is accomplished using SEEQ's proprietary oxynitride process and its innovative Q-Cell design. Products which are specified with 1,000,000 cycle endurance are designated with "55" series part numbers.

Endurance failures are characteristically caused by dielectric breakdown occurring in the tunnel dielectric itself. This breakdown is associated with charge trapping that occurs during repeated write/erase cycles. Because this behavior is central to the device physics of an EEPROM memory cell, endurance will be discussed in two parts; first, at the cell level, then, at the product level.

Table 2. High Temperature Dynamic Life Stress Results

Product	Total Devices Stressed	Total Device Stress Hours @ $T_a = 125^\circ \text{C}$	Number of Failures	Predicted Failure Rate @ 90% Confidence @ $T_a = 55^\circ \text{C}$ ( $E_a = 0.4$ eV)
52B13	684	684,000 hrs.	1	0.050%/1000 hrs.
52B33	603	658,000 hrs.	1	0.052%/1000 hrs.
5516A/2816A	603	772,000 hrs.	1	0.045%/1000 hrs.

During each write/erase operation of a floating-gate EEPROM cell, a miniscule amount of charge is trapped in the dielectric through which the programming charge tunnels (Ref. 1). The cumulative effect of this charge trapping has a strong impact on the effective threshold voltage that the cell exhibits at each write/erase cycle. The envelope of the "written" threshold voltage and the "erased" threshold voltage plotted over a number of cycles is referred to as the cell threshold "window" and is a key figure of merit for any EEPROM cell. Referring to the representative threshold window shown in Figure 3 the net effect of charge trapping results in an initial widening of the window (due to positive trapped charge). Ultimately, negative charge trapping sets the upper limit on endurance when the window becomes too narrow to be useful.

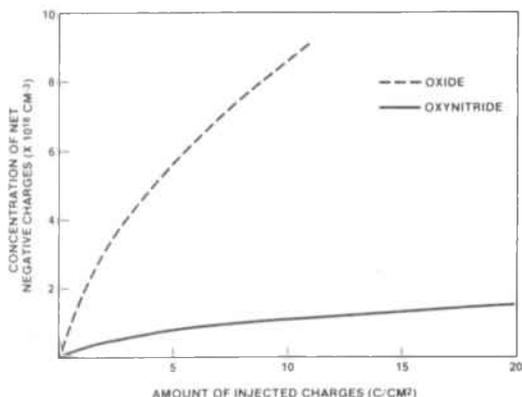


FIGURE 5. Comparison of Negative Charge Trapping

As seen from the endurance plot of Figure 3, the threshold window achieved using the SEEQ oxynitride dielectric represents an improvement over the traditional silicon dioxide case by at least a factor of ten. The oxynitride window demonstrates very little closing at  $10^6$  cycles, and provides a very useable window at  $10^7$  cycles.

The improved performance of oxynitride over oxide is directly related to the superior trapping characteristics of the oxynitride film, as shown in Figures 4 and 5. In Figure 4, the positive charge trapping characteristics of oxynitride and oxide are compared as a function of field strength (the principal independent variable). The positive charge trap density is consistently lower for oxynitride by approximately a factor of four. In Figure 5, the negative charge trapping characteristics of oxynitride and oxide are compared as a function of total injected charge (the principal independent variable in this case). Note the benefit of oxynitride in this case continues to increase with increasing charge, thus verifying the endurance improvement first observed in Figure 3.

Units were pulled from finished goods inventory and stressed by performing repeated write/erase cycles on every byte in the memory. Data retention, read/write functionality, AC performance, and parametrics were periodically tested against data sheet specs. Failures (typically caused by the selective failure of random bits) were analyzed and compiled for failure rate calculations.

A summary of the results is shown in Table 4. It shows that all of SEEQ's EEPROMs meet or exceed the intrinsic MOS failure rate of 0.05%/1000 hours if you write once per day. It should also be noted that the Q-Cell EEPROMs have higher endurance than the non Q-Cell 52B13. All of SEEQ's EEPROMs are Q-Cell except for the 52B13. For applications where writing occurs more frequently or where a failure rate of less than 0.03%/1000 hours is required, then a 1,000,000 cycle part such as the 16K 5516A should be considered.

## Reference

- (1) Ching S. Jeng et al, IEDM Technology Digest 1982, p. 811.

Table 3. High Temperature Bake Test Results

Product	Total Devices Stressed	Total Device Stress Hours @ Ta = 250° C	Number of Failures	Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.6 eV)
52B13	82	118,000 hrs.	2	0.0023%/1000 hrs.
2816A/ 2817/ 5516A	133	133,000 hrs.	0	0.000873%/1000 hrs.

**Table 4. Write/Erase Endurance Test Results**

<b>Product</b>	<b>Total Devices Stressed</b>	<b>Total Device Stress Cycles</b>	<b>Number of Failures</b>	<b>Predicted Failure Rate @ 90% Confidence @ Ta = 55° C (Ea = 0.125 eV)</b>	<b>Equivalent Failure</b>
52B13	189	4.4 m cycles	5	0.305%/1000 cycles	.013%/1000 hrs.
2816A/ 2817	2,196	1,057 m cycles	147	0.0225%/1000 cycles	0.0009%/1000 hrs.
5516A	1,427	1,427 m cycles	5	0.001%/1000 cycles	0.00004%/1000 hrs.
52B33	3,107	1,732.4 m cycles @ 25°C 8.5 m cycle @ 125°C	68 8	.0078%/1000 cycles	.00032/1000 hrs.

**Accelerated stress is updated quarterly and is available from SEEQ Technology.**

**RELIABILITY**



# Radiation and MOS Non-Volatile Memories

## Introduction

The effect of radiation on non-volatile memories is of concern when the devices may be exposed to radiation and are expected to continue functioning. Such environments include space, non-hardened battlefield conditions or commercial radiation applications. SEEQ EEPROM's have demonstrated similar performance as other NMOS or CMOS memories and can be successfully used in the above listed environments, as well as other applications requiring functionality during and after radiation exposure. SEEQ EEPROM's have proven particularly resistant to single event upsets.

## Concerns

### A. Permanent damage is a function of:

1. Total dosage of ionizing radiation;
2. Neutron flux;
3. Gamma dose rate.

### B. Transient errors (single event upset) are a function of:

1. Cosmic rays;
2. Gamma dose rate.

## Failure Mechanisms

### A. Permanent Damage:

1. Build up of trapped charge in dielectrics, primarily gate oxides; caused by net positive charge generated by the radiation flux congregating at defects in the oxide. This results in threshold shifts and subsequent non-functionality.
2. Build up of interface states caused by net positive charge generated by the radiation flux accumulating at layer boundaries. This results in degradation in transconductance and threshold shifts and subsequent non-functionality.
3. Formation of interstitials and vacancies in the crystal lattice structure caused by neutron flux. This results in changes in the electrical characteristics of the bulk silicon and subsequent non-functionality.

### B. Transient Errors:

1. Generation of false electrical signals from photo-currents in semi-conductor junctions caused by high energy particles or gamma rays. These result in data upset during read.

## Models

**A. Total dose ionizing radiation:** Simulated by exposure to gamma rays, usually from a Co 60 source. Expect MOS devices to withstand  $10^3$  to  $10^4$  rad(Si) of total dose before permanent damage. Variables include:

1. Thinner gate oxides are less likely to trap charge.
2. Bias applied during irradiation aggravates charge trapping.

**B. Dose rate:** Simulated by exposure to gamma rays usually generated by a linear accelerator. Expect MOS parts to withstand  $10^6$  to  $10^7$  rad(Si)/sec before transient damage and  $10^9$  to  $10^{10}$  rad(Si)/sec before permanent damage.

**C. Neutron flux:** Simulated by exposure to neutrons, usually generated by a nuclear reactor. Expect MOS parts to withstand greater than  $10^{14}$  neutrons/cm<sup>2</sup>.

**D. Cosmic rays:** Simulated by exposure to high energy, heavy ions, usually generated by a particle accelerator. Baseline standards are not well established for MOS parts.

1. Smaller channel lengths appear to aggravate upsets.

## Data for SEEQ MOS parts (attached)

**A.** Total dose is as expected for a thin oxide, MOS part.

**B.** Dose rate for both transient and permanent damage is better than typical for MOS parts.

**C.** No data for neutron flux, but expect to be similar to other MOS parts, e.g. greater than  $10^{14}$ /cm<sup>2</sup>.

**D.** Data for single event upset (SEU) is using various models to simulate worse case cosmic rays. The parts appear to perform better than expected.

## Definitions

**A. Curie**— A quantity of radioactive material undergoing 3.7 times  $10^{10}$  disintegrations per second.

**B. Rad**— Radiation Absorbed Dose — The absorption of 100 ergs of radiation energy per gram of absorbing material.

**C. Roentgen**— The amount of gamma rays required to produce ions carrying 1 electro-static unit of charge in 1 cubic centimeter of dry air.

# Radiation and MOS Non-Volatile Memories

**D. REM** — Radiation Equivalent (in) Man — The measure of the biological effect of radiation exposure and is obtained by multiplying the absorbed dose (in rads) by a "quality factor" for the particular radiation.

**E. Radioactivity** — The spontaneous emission of radiation, e.g. particles and/or electro magnetic waves (photons), from the nuclei of an unstable isotope, which eventually decays to a stable non-radioactive isotope.

## Radiation Test Results

**16K EEPROM**      **64K EEPROM**  
**(5516A/2816A,**      **(52B33,**  
**5517A/2817A,**      **2864)**  
**52B13)**

Stress	Conditions	Failure Mode	Failure Range	Failure Range
Unbiased total dose	Alternating data patterns, (e.g. 1st exposure all 0's, next exposure all 1's) Co 60 gamma ray source (10 RAD/SEC)	Device will read but some locations fail to write	9000 ± 2000 RAD (Si)	6500 ± 500 RAD (Si)
Biased total dose	Alternating data patterns, (e.g. 1st exposure all 0's, next exposure all 1's) Co 60 gamma ray source (10 RAD/SEC)	Device will read but some locations fail to write  Read only	3000 ± 1500 RAD (Si)	3000 ± 500 RAD (Si)  11,000 (±) 2500 RAD (Si)
Biased dose rate upset	Erased (1's state), linear accelerator gamma ray source	Upset during read; not permanent	$3 \pm .75 \times 10^7$ RAD (Si)/SEC	$1.6 \pm .02 \times 10^7$ RAD (Si)/SEC
Biased dose rate survival	Erased (1's state), linear accelerator gamma ray source (200 RAD/20 ns PULSE)	Device will read, all locations fail to write	$> 10^{10}$ RAD (Si)/SEC	$\sim 10^{10}$ RAD (Si)/SEC

**256K EPROM**  
**(27C256)**

Stress	Conditions	Failure Mode	Failure Range	
Biased total dose	Memory Programmed to all 0's, Exposed to Co60 source (1 to 35 RAD/SEC)	Device Fails to Read, Multiple bits read 1's	15,000 (±) 2,000 RAD (Si)	

**256K EEPROM**  
**(28C256)**

Dose Rate Upset	Byte Checkerboard Data Pattern; 54 ns to 1.5 us Pulse Widths; Linear Accelerator	Single Bits Change State	$1.1 \times 10^9$ to $6.6 \times 10^{10}$ RAD (Si)/SEC	
Biased Dose Rate Latch-Up	Byte Checkerboard Data Pattern; 54 ns to 1.5 us Pulse Widths; linear Accelerator	Parts Fail to Read, Recover After Power Down	$5 \times 10^7$ to $1 \times 10^8$ RAD (Si)/SEC	

RELIABILITY

## Single Event Upset 64K EEPROM (52B33)

Samples were programmed and subjected to different levels of radiation to simulate a cosmic flux.

The devices are read after irradiating for upsets

RUN #	IONS	LET	FACILITY	ENERGY	RAD H2O	TIME	UPSETS
1	Fe	8	BEVATRON		144	30 SEC	NONE
2	Fe	6	BEVATRON		144	30 SEC	NONE
3	Fe	4	BEVATRON		288	2 MIN	NONE
4	Fe	3.8	BEVATRON		288	2 MIN	NONE
5	Kr	41	CYCLOTRON	200 MeV			NONE
	Ar	15.4	CYCLOTRON	160 MeV			NONE
	Ne	5.7	CYCLOTRON	88 MeV			NONE
	O	1.8	CYCLOTRON	217 MeV			NONE
	N	2.9	CYCLOTRON	68 MeV			NONE
6	P	.004	CYCLOTRON	148 MeV			NONE
7	CF-252	42		105 MeV			NONE

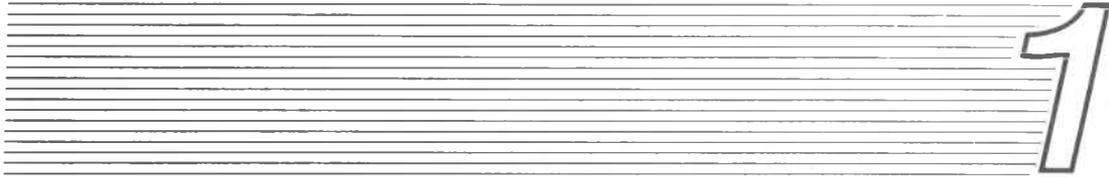
# 6

## ***APPLICATIONS***

(Application Notes)



**Memory Products  
Application Note**



**48128 FLASH™ EEPROM  
OFFERS IN-CIRCUIT  
REPROGRAMMABILITY**

*April 1987*

APP. NOTES

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**seeq**  
*Technology, Incorporated*

# MICROPROCESSOR INTERFACING WITH SEEQ'S FLASH™ EEPROMS

## INTRODUCTION

This application note describes the interfacing of SEEQ's FLASH™ Electrically Erasable Programmable Read Only Memory—'FLASH'™ EEPROMs to a microprocessor bus. The 48128 FLASH™ EEPROM is the first member of a new generation of memory devices from SEEQ. The 48128 FLASH™ EEPROM is a 128 K-bit (16Kx8) memory device combining EPROM and EEPROM technologies to give a high density, low cost memory ideal for applications with infrequent in-system updates such as program store. The FLASH™ EEPROM can be easily bulk-erased electrically and programmed in-circuit. Only a single high voltage supply (21 v) is needed for chip erase or byte write. The fast read access time (170 ns) meets the requirements of many of today's popular microprocessors.

### FLASH™ EEPROM Advantages:

The in-circuit erasability and programming feature of the FLASH™ EEPROM brings several system advantages:

- Reduction of system development time—the FLASH™ EEPROMs erase in 20 seconds and program fully in 32 seconds. In contrast a 128K UV EPROM takes 20 to 30 minutes under ultra-violet light to erase and programming time is over 2 minutes. Also the UV EPROMs have to be removed from their sockets for each erasure.
- Elimination of unreliable socket connections—the FLASH™ EEPROMs can be soldered directly on to the circuit board thus improving contact reliability.

- Elimination of excessive device handling during software changes occurring during user development/testing/ production.
- Elimination of glass-epoxy circuit board degradation due to ultra-violet radiation—the FLASH™ EEPROM can be erased electrically in-circuit unlike UV EPROMs.
- Elimination of UV radiation health hazard by using the FLASH™ EEPROM.

### FLASH™ INTERFACE CONCEPTS:

The FLASH™ EEPROMs interface concepts are similar to EEPROMs. SEEQ memory products application notes 2A and 8A describe microprocessor interface techniques for SEEQ's EEPROM devices. In this application note FLASH™ EEPROM interface techniques are presented. The 48128 FLASH™ EEPROM data sheet provides detailed information on device characteristics. The unique part of the FLASH™ EEPROM interface to the microprocessor is the chip erase and write concept. The FLASH™ EEPROM has to be chip erased before a write. The chip erase time is 20 seconds. A write operation can also be performed without first erasing the chip if the previously written (non-FF Hex) data will not be changed. As is the case with UV EPROMs, if a location is to be changed from a non-erased state, 48128 FLASH™ EEPROM must be chip erased first. The write time per byte is 2 ms. Hence, there is an intrinsic timing difference between the 48128 memory and the microprocessor. Therefore additional hardware is necessary to accommodate these timing differences. The read operation is similar to EEPROMs and UV EPROMs.

FLASH™ is a registered trademark of SEEQ Technology, Inc.

There are different approaches to microprocessor interfacing:

- The microprocessor performs a write (or erase) operation as usual. As soon as the command is initiated, a control interface takes over and continues the command operation independent of the CPU. Command termination is indicated to the CPU by the control interface through interrupt service or I/O polling schemes. Thus, the microprocessor can run independently of the FLASH™ EEPROM controller during chip erase or write time.
- In the second approach the microprocessor is dedicated to the FLASH™ EEPROM chip erase/write operation. The disadvantage is that the microprocessor is inhibited from doing any other function during the chip erase and/or the write time.

The second approach is acceptable in many applications where erase/write is infrequent. This technique is very easy to implement and does not require any software overhead in terms of I/O polling or interrupt servicing. In terms of hardware the scheme can be implemented by controlling the microprocessor's ready line. In this case wait states are inserted in the microprocessor's cycle as long as necessary to complete the chip erase or write operation.

The two distinct interface approaches dictate the amount of hardware and software required to interface the FLASH™ EEPROM to the microprocessor. The efficiency of information transfer is also dependent on the type interface approach taken. This application note discusses the second approach, since the FLASH™ EEPROM is an ideal device for systems with infrequent system updates, requiring low cost,

high density memory with in-circuit erase/write feature. An overview of the 48128 FLASH™ EEPROM chip erase and write operation is given prior to the interface discussion.

## FLASH™ EEPROM CHIP ERASE/WRITE

Chip erase is done by raising  $V_{PP}$  to high voltage (21 V) with  $\overline{OE}$  held at a TTL high level. Address pins  $A_1$ ,  $A_2$ ,  $A_6$  must also be brought to a high voltage level. The erase cycle is then started by  $\overline{PGM}$  and  $\overline{CE}$ . During the erase cycle it is necessary to control address  $A_3$ . Wait states are inserted in the processor's write cycle to stretch  $\overline{PGM}$  active width to 100  $\mu$ s. For complete erasure the effective  $\overline{PGM}$  width should sum up to or equal 10 seconds each with  $A_3$  'high' and 'low' alternatively. This can be achieved by repeating the 100  $\mu$ s writes 100,000 times twice; first with address  $A_3$  high and then low. See 48128 data sheet for chip erase details.

Once the chip is erased fully, the FLASH™ EEPROM can be written by applying a high voltage to the  $V_{PP}$  pin (21 V).  $\overline{OE}$  should held high.  $\overline{CE}$  then selects the device and pulsing  $\overline{PGM}$  after presenting valid data at the inputs starts the write cycle. The  $\overline{PGM}$  low pulse width(s) should equal 2 ms for a successful byte write. Processor time can be saved by only writing to those address locations in which data will change from the erased state (FF Hex).

The control signal specifications for read, chip erase and write operations of the 48128 FLASH™ EEPROM are shown in the mode selection Table (table 1). For timing specifications refer to the data sheet.

Function Mode (Pin)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	$V_{PP}$ (1)	$A_1, A_2, A_6$ (9, 8, 4)	$A_3$ (7)	$V_{CC}$ (28)	$D_0 - D_7$ (11-13, 15-19)
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	Address	$A_3$	$V_{CC}$	$D_{OUT}$
Standby	$V_{IH}$	X	X	X	X	X	$V_{CC}$	HI Z
Write	$V_{IL}$	$V_{IH}$	TTL Pulse	$V_{PP}^{[1]}$	Address	$A_3$	$V_{CC}$	$D_{IN}$
Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	Address	$A_3$	$V_{CC}$	$D_{OUT}$
Chip Erase	$V_{IL}$	$V_{IH}$	TTL Pulse	$V_{PP}^{[1]}$	$V_{EA}^{[2]}$	TTL Pulse	$V_{CC}$	HI Z

Table 1. Mode Selection

Notes:

1.  $V_{PP}$  - 21V
2.  $V_{EA}$  - 15V min 21V max
3. X - Don't Care

## V<sub>PP</sub> AND CHIP ERASE SWITCHING

For in-circuit erase/write V<sub>PP</sub>, A<sub>1</sub>, A<sub>2</sub> and A<sub>6</sub> switching is key to the microprocessor interface. This necessitates that high voltage signals be actively present in the microprocessing environment. The high voltage signals are dynamic and need to be controlled over a wide temperature range. V<sub>PP</sub> can be at 21V for all modes of operation for the 48128 (table 1). Hence V<sub>PP</sub> can be connected directly to 21V eliminating the need for a V<sub>PP</sub> switch. The high voltage circuit drivers for chip erase (i.e) A<sub>1</sub>, A<sub>2</sub>, A<sub>6</sub> are shown in Figure 1. The high voltage power supply should take into account the saturation voltage drop across the switching transistors. It is important to note that the chip erase driver does not have to source large currents. The high voltage levels on A<sub>1</sub>, A<sub>2</sub>, A<sub>6</sub> are needed to trigger the internal level detectors on 48128 during Chip Erase Mode and the maximum current would be 10μA on these inputs. See 48128 datasheet for specs. The high voltage rise times for V<sub>PP</sub> and chip erase (A<sub>1</sub>, A<sub>2</sub>, A<sub>6</sub>) should be long to minimize overshoots. The 0.1 μF capacitor placed between V<sub>PP</sub> and ground provides additional protection against overshoots during erase/write operations. The capacitor should be high frequency ceramic disc type in order to handle transient noise

spikes. Another important point to be considered is the effect of pin to pin coupling between input signal lines. Because of the 21 V high voltage pulses, the voltage coupled between input signals can be quite large and may damage other devices on the signal line whose input specifications demand that V<sub>IN</sub> does not exceed V<sub>CC</sub>+1 V. Due to the high input impedance of MOS memories, driver characteristics, signal shielding, device package and board layout parameters have to be considered to minimize the effects of pin to pin coupling between input signal lines.

Microprocessor system environments demand the capability to connect multiple devices together. The 48128 FLASH™ EEPROM mode table shows that the device can be deselected using CE during erase/write. Hence, from a system perspective, Chip Erase (A<sub>1</sub>, A<sub>2</sub>, A<sub>6</sub>) can be bussed to multiple devices in the system. Using TTL level control of only CE, any FLASH™ EEPROM device can be selectively erased or written. This allows for simple and straightforward control of multiple FLASH™ EEPROMs in the system. The result is a highly compact, cost effective design with only one Chip Erase switch for the entire FLASH™ EEPROM memory array.

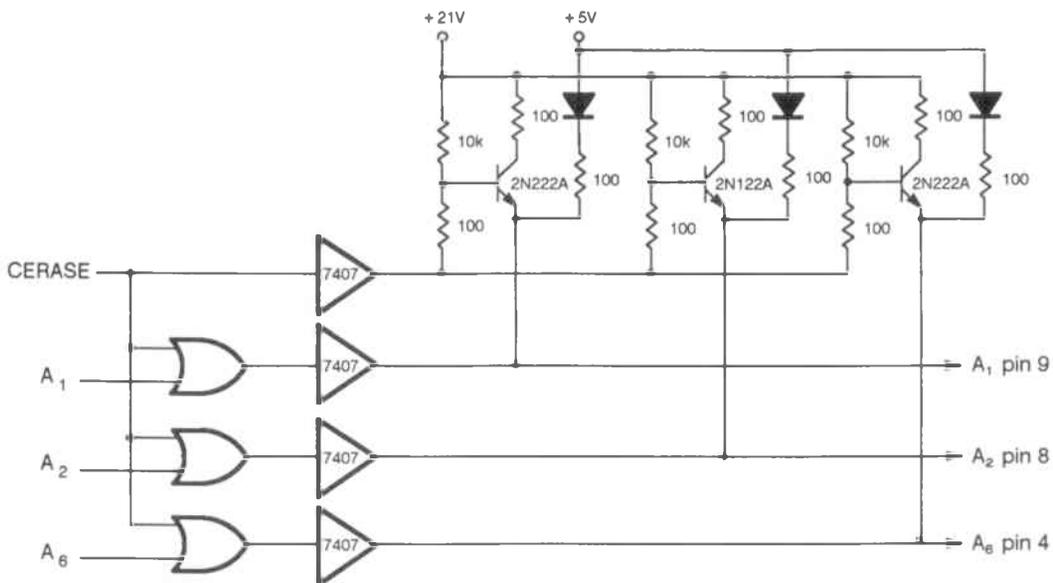


Figure 1. High Voltage Drivers for Chip Erase

## Switching Regulator

In order to generate the high voltage pulses required for  $V_{PP}$ ,  $A_1$ ,  $A_2$  and  $A_6$ , a power supply with the capacity to supply output voltages up to +24 V is needed. In a system environment where this voltage is not available a D.C to D.C switching regulator can be used to convert +5 V to +21 V.

A switching regulator worth considering is the LT1070 from Linear Technology. The LT1070 is a monolithic high power switching regulator capable of delivering load power up to 100 watts without external power devices. The switch duty cycle in the device is controlled by switch current.

The LT1070 is operated in the boost mode. Design procedure for the 5V to 21V boost regulator is fairly simple and straightforward. Figure 2 shows the boost regulator. The  $V_{CC}$  pin is used for frequency compensation, current limiting, soft start and shut down. Empirical techniques have to be used to select component values for frequency compensation, soft start and shut down. It is recommended that LT1070 data sheets and design manual AN-19 from Linear Technology be used to develop individual designs.

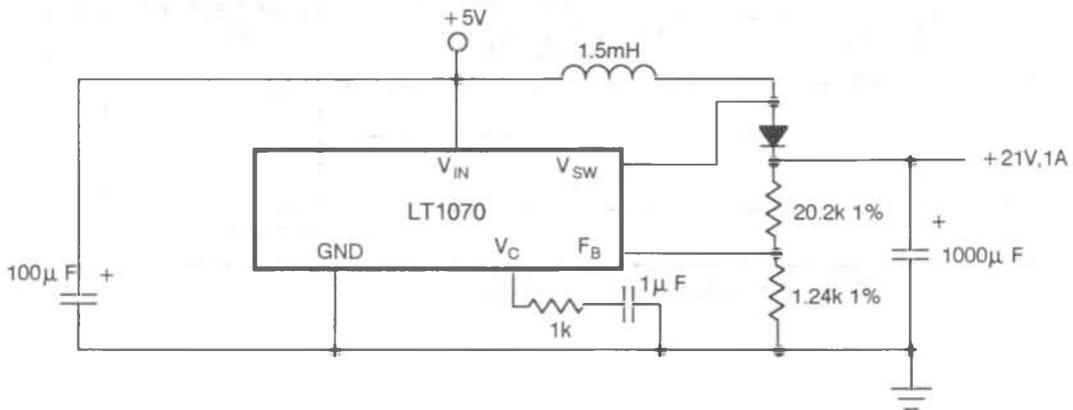


Figure 2. +5V to +21V Boost Regulator

## MICROPROCESSOR INTERFACE OVERVIEW

In the FLASH™ EEPROM interface to a microprocessor bus, both bus timing and software timing are used to gate the control signals. Figure 3 shows the block diagram of the control interface. It is assumed that the microprocessor is dedicated to the task of erasing/writing the FLASH™ EEPROM. The  $V_{PP}$  and Chip Erase switches can be turned on/off through dedicated I/O ports of the processor. The other option would be to use logic gates along with latches and assign dedicated memory ad-

resses for the switches. Then, the  $V_{PP}$  and Chip erase switches can be turned on or off by performing dummy writes to the addresses. The memory write control line of the processor should be connected to the FLASH™ EEPROM PGM pin. The wait state generator uses the microprocessor's ready line to insert wait states in the memory write cycle to extend the write cycle time to 100  $\mu$ s. ' $\overline{V_{PPON}}$ ' is used to qualify wait state generation.



## Write cycle extension

Different techniques can be used to insert wait states into a microprocessor's write cycle. A convenient approach would be to use a one-shot like the 74HC123A, Figure 4.  $\overline{V_{ppON}}$  and the start of a write cycle should trigger the 100  $\mu\text{s}$  timer. The one-shot's 100  $\mu\text{s}$  pulse output is used to negate the processor's READY line thus inserting wait states in to the write cycle. It is important to ensure that the RC time constant used to time the 100  $\mu\text{s}$  pulse is temperature compensated. The FLASH™ EEPROM 48128 specifies a minimum pulse width of 90  $\mu\text{s}$  and a maximum pulse width of 120  $\mu\text{s}$  for the

$\overline{\text{PGM}}$  signal during write. Hence the one-shot design should ensure that the write cycle duration does not violate device specs.

An alternative to the one-shot is a programmable digital timer like the 74LS294, Figure 5. The count module can be digitally controlled using the inputs provided. For example, using a 5 MHz clock, programming for  $2^9$  will give a period of 102.4  $\mu\text{s}$ . Using this signal as the 'NOT READY' to the processor, the write cycle time or PGM width can be extended to a minimum of 102.4  $\mu\text{s}$  satisfying the 48128 write specifications for PGM width.

Write Cycle Extension Using Ready Input of Microprocessor

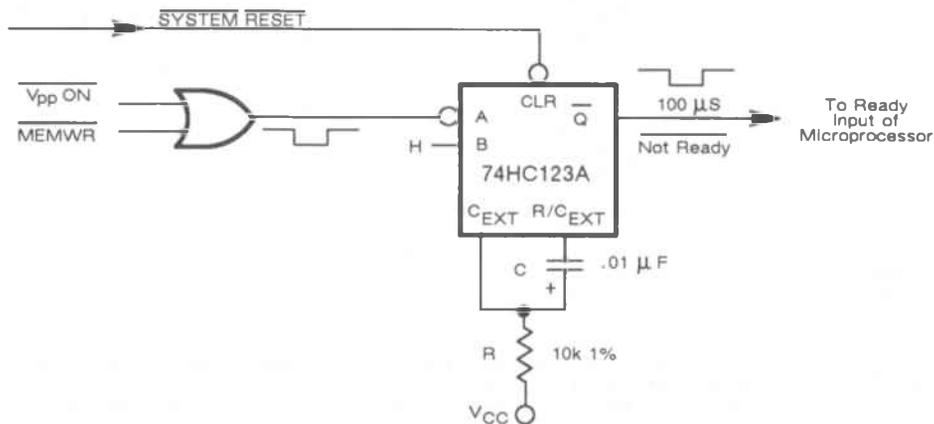


Figure 4. One-Shot Approach

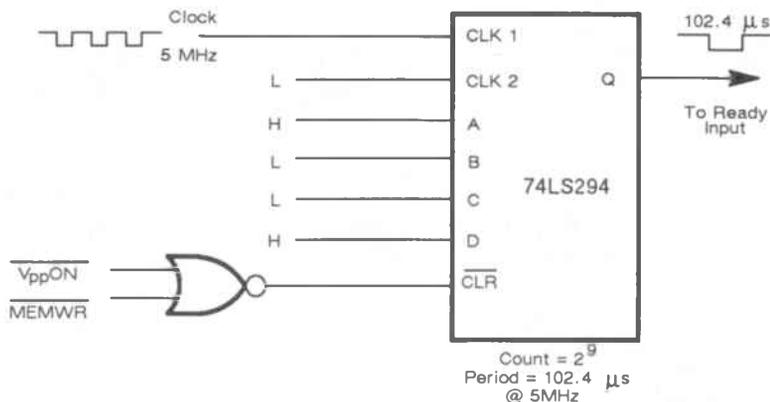


Figure 5. Programmable Digital Timer Approach

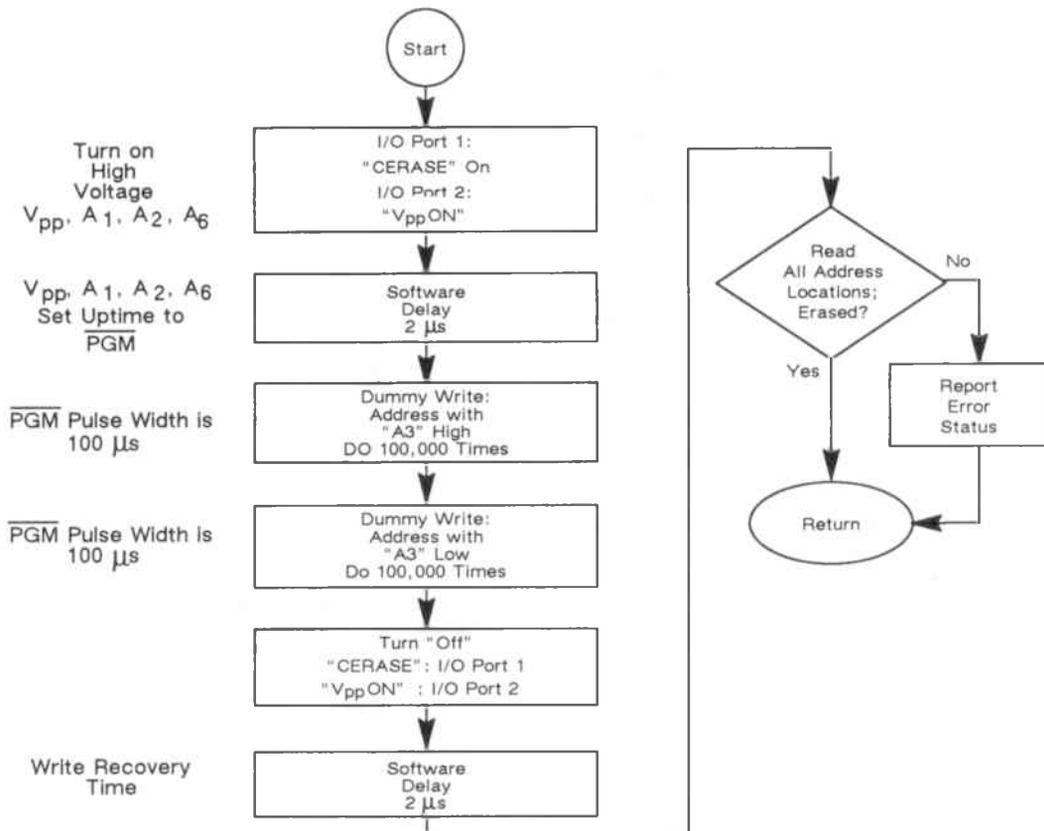


Figure 6. Flash™ EEPROM Chip Erase Flowchart

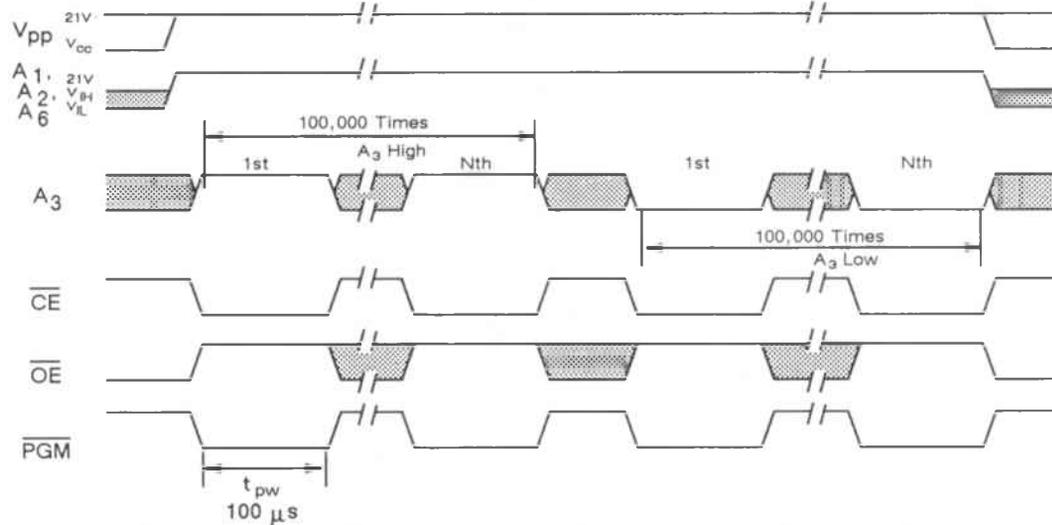


Figure 7. Flash™ Chip Erase Timing

## Chip Erase

During Chip erase, it is necessary to control the address line  $A_3$ . In the high voltage drivers shown in Figure 1 for chip erase, the OR gates ensure that addresses  $A_1$ ,  $A_2$  and  $A_6$  remain 'high' during chip erase. Dummy writes to any two address locations can be performed in order to toggle  $A_3$  for chip erase; one with address bit  $A_3$  high and a second with  $A_3$  low. For example the addresses can be 00FF hex and 00F7 hex. The order of toggling  $A_3$ , i.e. the addressing order is immaterial. The software flowchart to control the FLASH™ EEPROM chip erase and programming is shown in Figures 6 and 8. The write cycle time or the PGM width is assumed to be 100  $\mu$ s. To do a chip erase the processor does dummy writes to the selected FLASH™ EEPROM 100,000 times twice; first with  $A_3$  address line at '0' and subsequently with  $A_3$  at '1' or vice versa. With this technique, the effective PGM width during  $A_3$  'high' and 'low' times, add up to 10 seconds each to total 20 seconds thus satisfying the 48128 datasheet specifications for chip erase.

Using the digital timer approach with a 5 MHz clock, would give a PGM width of 102.4  $\mu$ s. The number of writes then should be 97655 times instead of the 100,000 times to achieve the 10 seconds effective time.

## Writing to FLASH™ EEPROM

While programming the FLASH™ EEPROM, it should be ensured that Chip Erase is 'OFF' before starting the programming cycle. A 100  $\mu$ s write cycle is performed with the data and address for each memory location to be programmed. The process is repeated 20 times. The effective write cycle time thus adds up to 2 ms satisfying the PGM pulse width requirement for programming. With the digital timer approach the effective write time will be 2.048 ms. Processor write time can be saved by only writing to those locations in which the data will change from the erased state. The 2  $\mu$ s delays shown in the software flowchart are needed to satisfy the  $V_{PP}$ , Chip Erase ( $A_1$ ,  $A_2$  and  $A_6$ ) setup times and write/erase recovery time of the 48128 FLASH™ EEPROM. Other timing requirements of the FLASH™ EEPROM like the address, data,  $\overline{CE}$  and  $\overline{OE}$  setup times are satisfied using hardware techniques. The techniques outlined in this application note use general control signals to permit

adaptation to any microprocessor system's bus. Examples of interfacing to specific processors are now presented.

## Intel 8086/88

The Intel 8086 and 8088 are microprocessors with time multiplexed address and data lines. Both the processors have 20-bit address bus and differ essentially from one another by their respective data bus widths. The 8086 uses 16-bit data bus while the 8088 uses 8-bit data bus. The interface example discussed here uses the 8086 and the technique can be extended to the 8088 easily. The 8086 system discussed here is assumed to be in MAX mode with demultiplexed, buffered address and data lines. 8282 address latches, 8286 transceivers and 8205 decoders are assumed to be used. In addition it is assumed that the 8288 bus controller is used to control access to the FLASH™ EEPROM devices on the demultiplexed buffered system bus. The 48128-200 FLASH™ EEPROM with 200 ns read access time easily meets the read requirements of the 8 MHz 8086-2 microprocessor without the need for wait states. The 48128-300 with 300 ns read access time can be used with the 5 MHz 8086 processor without any wait states for the read operation. While the read interface is straightforward, the write/chip erase timing requirements of the 48128 FLASH™ EEPROM require a few accommodations to be made in hardware and software, to ensure 8086 and 48128 timing compatibility. The 5 MHz and the 8MHz 8086 timings during write operation meet the  $\overline{OE}$  setup time requirement of the 48128. The  $\overline{CE}$  and data setup times are '0' for the 48128. The next timing requirement is the PGM or the write command pulse width. Wait states have to be introduced in the processor write cycle to meet the 100  $\mu$ s PGM pulse width requirement for the 48128 chip erase/write operation. The Ready input for the 8086 should be disabled by the end of T2 processor state to guarantee the insertion of wait states. In order to meet the setup and hold requirements for the Ready input, the advanced write command (from the 8288 bus controller) along with the chip select signal can be used to generate the 100  $\mu$ s 'Not Ready' signal.

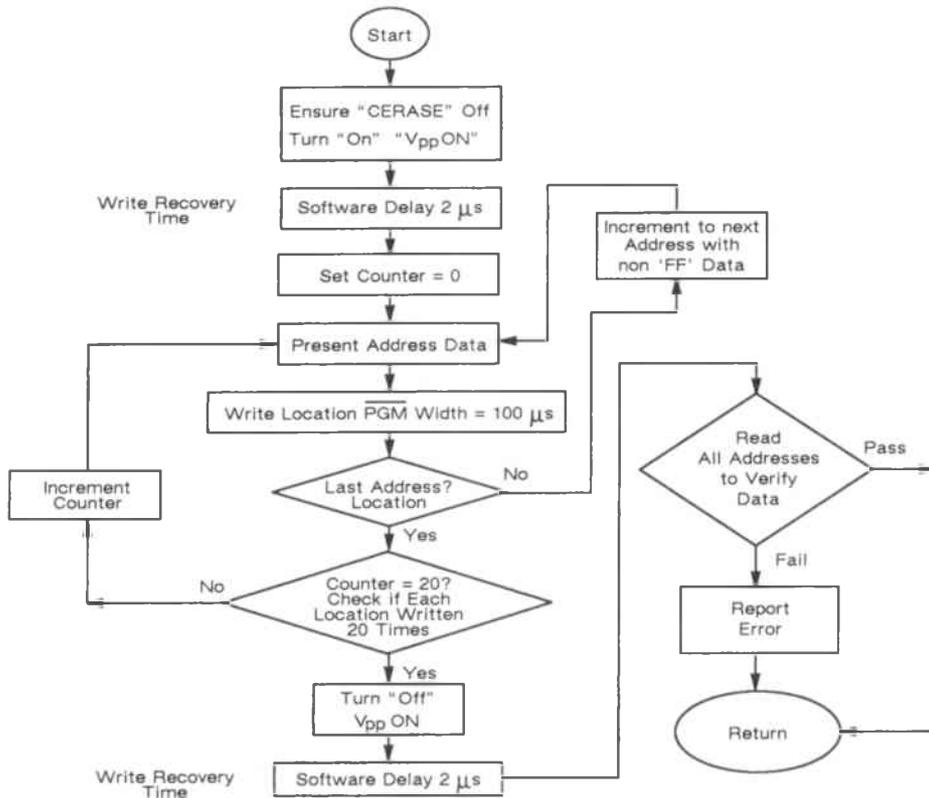


Figure 8. Flash™ Write Flow Chart

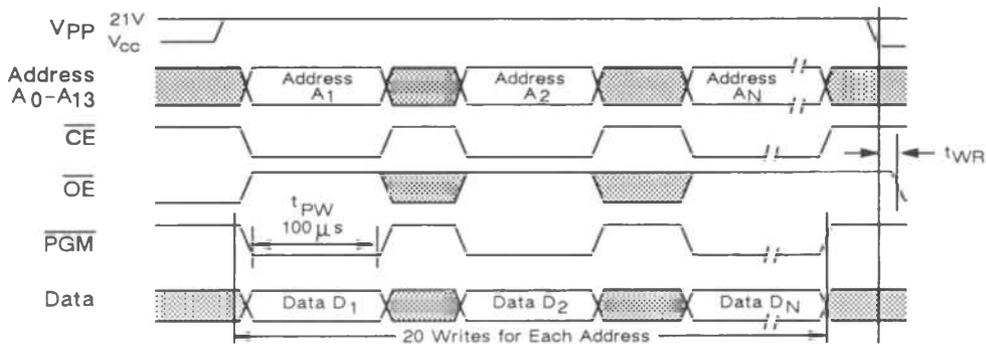


Figure 9. Flash™ Write Timing





## National NS32C016

The NS32C016 is a CMOS microprocessor with 32-bit architecture and implementation. It has a multiplexed address/data bus with 24-bits of address and 16-bits of data. It is assumed that the NS32C201 timing control unit (TCU) is used to provide system clock, system control logic and microprocessor cycle extension logic. 48128-200 with the 200 ns read access time can interfaced to the 10 MHz NS32C016-10 without wait states. In order to provide the 100  $\mu$ s PGM for the 48128 write operation it is necessary to extend the processor write cycle by inserting wait states. The NS32C016 CPU checks the RDY input at the end of T2 state on

the falling edge of PH2 clock, to see if wait states are needed. The CWAIT (continuous wait) pin on the NS32C201 TCU can be used to generate the wait states. The 100  $\mu$ s NOT READY signal should be gated with the TSO signal from the TCU to generate the CWAIT. TSO is activated at the beginning of state T2 of the CPU cycle and is de-activated at the beginning of state T4. The TCU drives the RDY pin to the CPU causing wait states to be inserted in the CPU cycle as requested by the CWAIT. The write cycle timing and interface are shown in Figures 14 and 15.

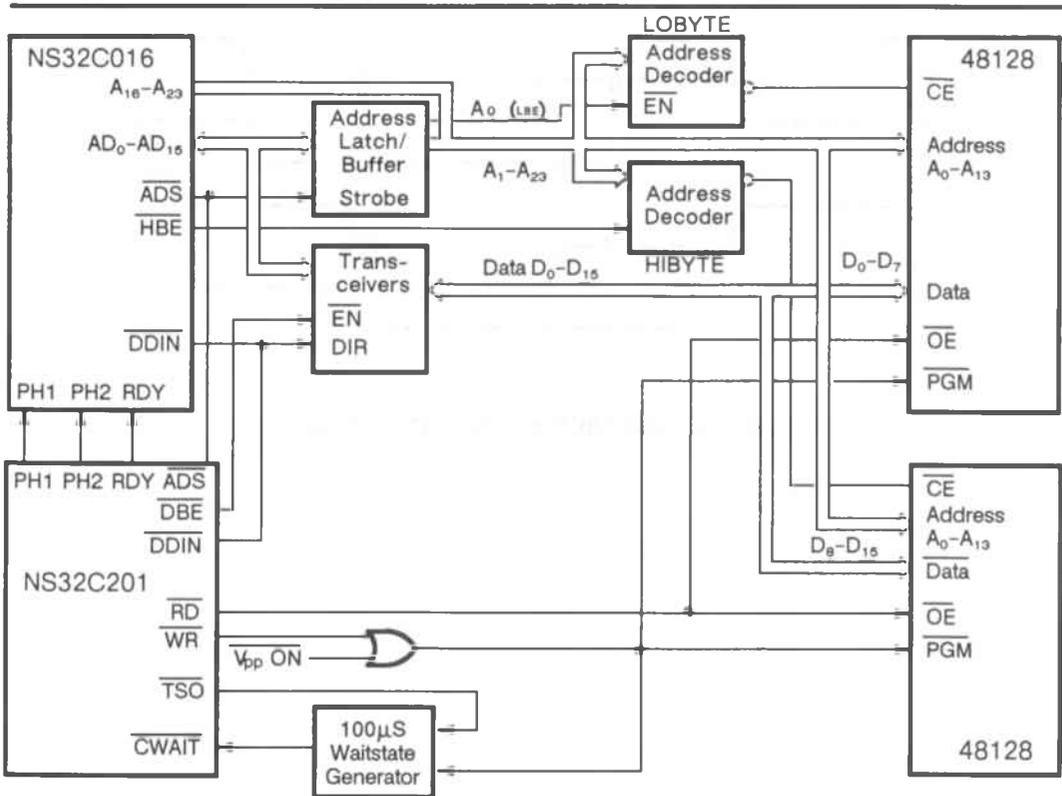


Figure 14. NS32C016 Interface to Flash™ EEPROM

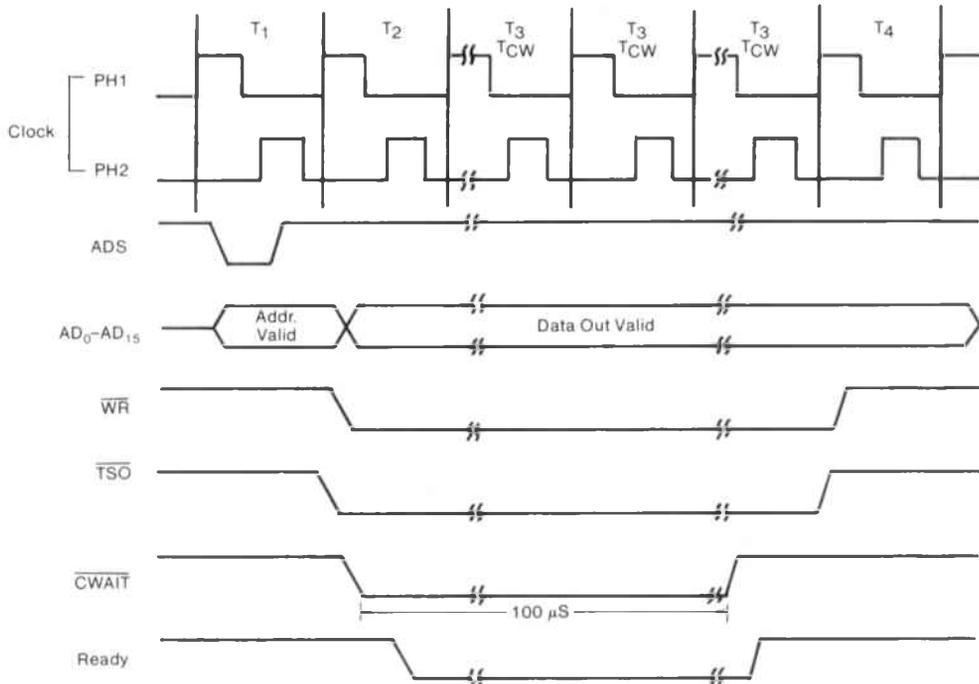


Figure 15. NS32C016 WRITE CYCLE TIMING

## CONCLUSION:

This application note has provided an example of a simplified approach for interfacing FLASH™ EEPROMs with microprocessors. The FLASH™ EEPROM interface described has utilized both hardware and software timing for chip erase and programming. An important point to keep in mind is that the tradeoffs between hardware and software timing is system dependent. It is obvious that FLASH™ EEPROMs

provide benefits to the system designer. In-circuit changes to non-volatile program and data storage can be implemented in systems at low cost. Also at the same time, costs associated with software changes, maintenance and service can be reduced significantly. System functionality and performance can be extended to higher levels.



**Memory Products  
Application Note**

**2**

**MICROPROCESSOR  
INTERFACING  
WITH SEEQ's  
LATCHED EEPROM**

*March 1985*

APP. NOTES

**seeq**  
*Technology, Incorporated*

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# Microprocessor Interfacing with SEEQ's Latched EEPROM

## Introduction

This application note describes the interfacing of SEEQ's "latched" Electrically Erasable Read Only Memory (E<sup>2</sup>ROM or E<sup>2</sup>) to a microprocessor bus. The latched E<sup>2</sup>ROM family is comprised of a 16K 52B13 and 64K 52B33. On each of these devices there are internal latches on all inputs except write enable. A byte must first be erased before it can be written. In addition to the latched E<sup>2</sup>ROM family, SEEQ has a timer E<sup>2</sup>ROM family. This family is comprised of a 16K 2816A (24 pins), a 16K 2817A (ready/busy) and a 64K 2864 (ready/busy). The timer family has internal latches on all inputs and has an internal timer which automatically performs a byte erase before write. In this application note, the E<sup>2</sup> used is SEEQ's 52B13, a 2K x 8 memory. Since the timing of the higher-density members of the family is compatible, the circuits given can be extended to interface equally well with the 52B33 (8K x 8). Both bus timing and software timing are used to gate the control signals. The case presented here uses general control signals to permit adaptation to any system's bus structure. In addition, modifications are given for interfacing to specific processors.

## Interface Signals

The solution presented here (see Figure 1) uses an  $\overline{S}$ - $\overline{R}$  flip-flop (74LS00) with TTL gates (74LS32) to latch  $\overline{WE}$  for the 52B13. This flip-flop causes valid data to be latched correctly, satisfies device setup and hold times, and allows easy latch/unlatch of the  $\overline{WE}$  signal.

The system-dependent direct bus interface components form the second part of the interface circuit. These components will generate  $\overline{CHIP\ SELECT}$  and  $\overline{E^2ROM\ SELECT}$  to enable this part of memory.

$\overline{CHIP\ SELECT}$  is usually generated separately for each word-wide group of devices. In this way, it chooses the actual devices to be written.  $\overline{E^2ROM\ SELECT}$  would be an "OR" function of the  $\overline{CHIP\ SELECT}$  signals for all the devices for which this latch gates  $\overline{WE}$ . With  $\overline{WE}$  wired in common, only one gated latch is required for the E<sup>2</sup>ROM array. Of course, fanout must be considered, with a high-current driver used if necessary. In the example bus interfaces shown in this application note, gating for one device is assumed, and  $\overline{E^2ROM\ SELECT}$  is tied directly to  $\overline{CHIP\ SELECT}$ .

The bus interface components perform other tasks common to a memory/bus interface. For a multiplexed data bus, the bus interface components must demultiplex the data and addresses. In addition, this bus interface circuitry may generate  $\overline{MEMORY\ READ}$  and  $\overline{MEMORY\ WRITE}$ , if required. Details of this bus interface are given in the section "Considerations for Special Applications," beginning on page 5.

## Details of Operation

### Byte Write or Erase

The timing diagram in Figure 2 shows the details of a byte write or erase operation for SEEQ's latched E<sup>2</sup>ROM family. The two modes are the same, except that hex "FF" is presented to the I/O lines for erasure. Due to this similarity, only the write mode will be discussed.

The first step is initiation of a write cycle. First, the processor issues addresses, and the system's decoding circuitry brings  $\overline{CHIP\ SELECT}$  valid. Although the chip is enabled at this point, a write to the chip has not yet begun, because  $\overline{MEMORY\ WRITE}$  has

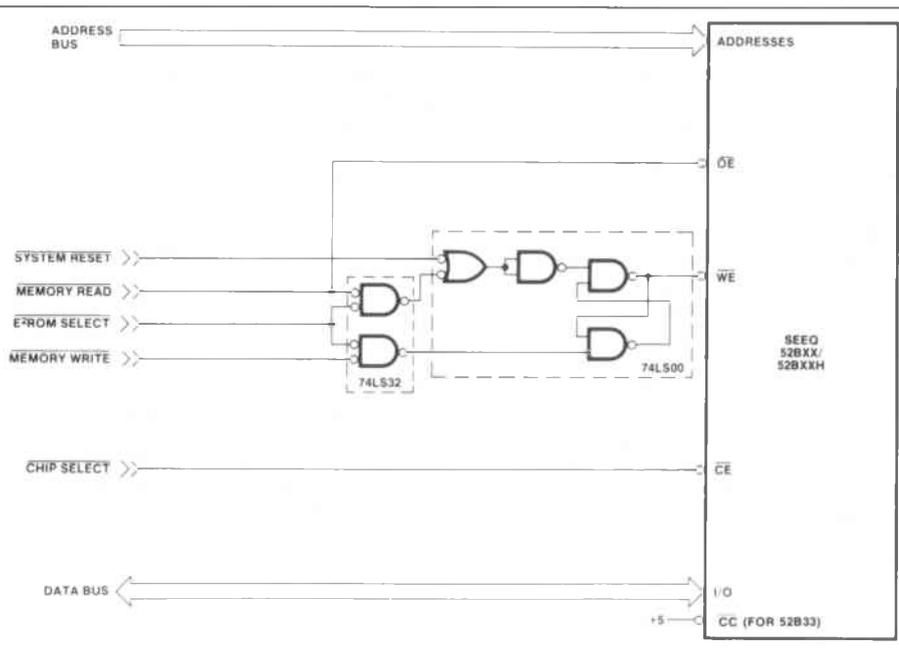


Figure 1. E2ROM Interface Circuit

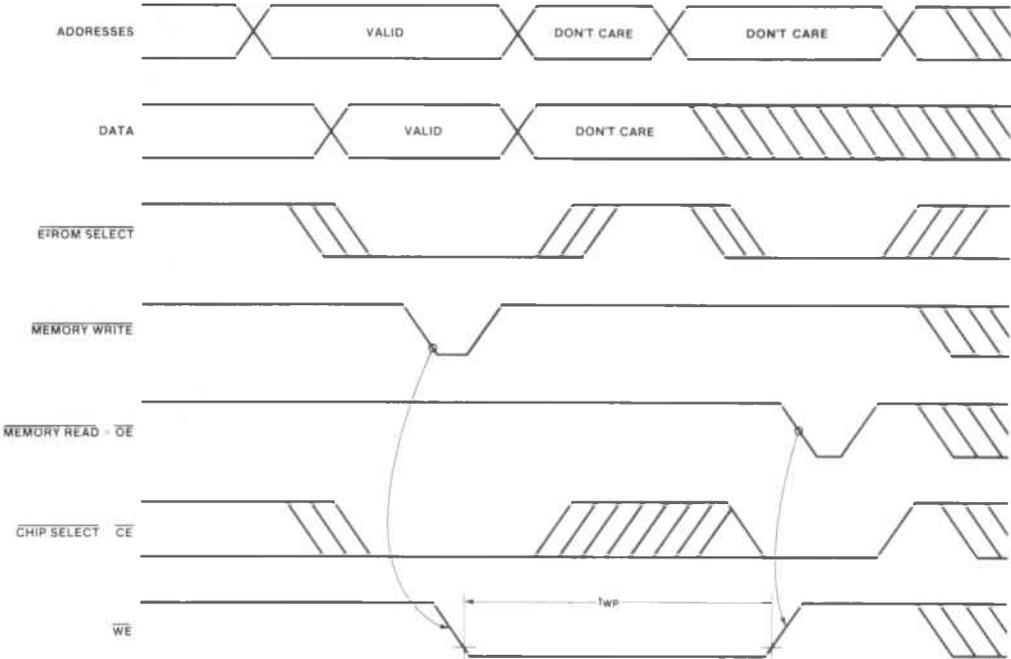


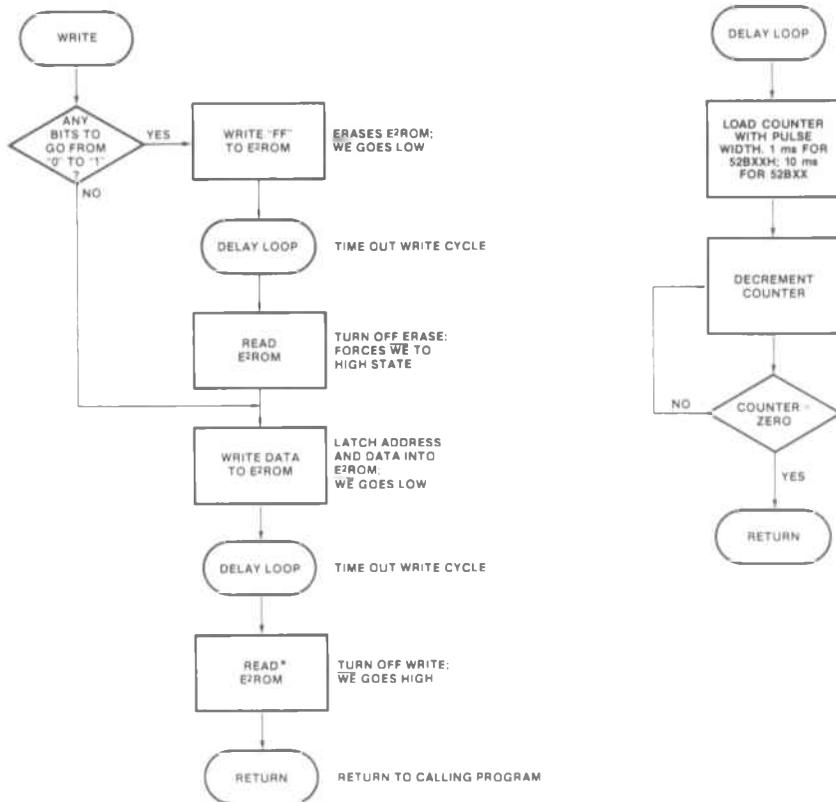
Figure 2. Write-Cycle Timing Diagram Latched E2ROM Interface Application

not yet been issued. This prevents inadvertently writing to an incorrect address as the address lines are allowed to settle out before a write is initiated. Following the timing events above, the active level of MEMORY WRITE sets the flip-flop, bringing  $\overline{WE}$  low to the E<sup>2</sup>. Data, Addresses,  $\overline{CE}$ , and  $\overline{OE}$  are latched at this point.

In the second part of a write,  $\overline{WE}$  continues to be active low for the entire write cycle. This requires a timeout, which can be effected in any of several ways. The designer can use a timing loop in software, or trigger a timer which interrupts the processor after the correct time. The software timeout may require less hardware on-board. The hardware timeout, on the other hand, allows the CPU to perform other tasks. Obviously, a good compromise is a software architecture with regular (perhaps one-millisecond) timing interrupts, for system real-time synchronization. Division of the task between hardware and software is best left to the individual systems engineer.

Regardless of the method used in the timeout, the write pulse is terminated by  $\overline{WE}$  being brought high. This is effected by a read to any location in the device, which resets the flip-flop to bring  $\overline{WE}$  high. A second read cycle is required for byte verify. System designers should allow extra time between the two reads to meet write recovery time ( $t_{WR}$ ) requirement. This method of write-cycle termination provides another form of protection against inadvertent writing to the chip. Even if a statistically unlikely succession of glitches were to trigger both flip-flops, enable the gates, and bring  $\overline{WE}$  low, a subsequent read to the device could terminate the write before data would be written.

For the case of a fully software-timed write, a flowchart is given for the sequence of operations (see Figure 3). This processor-independent flowchart handles all the erasure and writing for storing data in the E<sup>2</sup>ROM, using the circuit from Figure 1. In addition, a segment of example code (written for the Z8) is shown (see Figure 4).



\*Data is not valid during this cycle.

Figure 3. Flowchart for 52BXX Erase/Write — Software Timing

```

186 //-----
187 // The following is a general routine for writing
188 // data contained in the working register
189 // DataReg to an EEROM in
190 // the location pointed to by the working register
191 // pair AdReg, This EEPROM is assumed to be in the
192 // external data memory of Z8.
193 // Write FF to erase byte.
P 0060 7C FF 194 EEWR: LD OutReg, #%FF
P 0062 92 70 195 LDE @AdReg, OutReg
P 0064 D6 0071 196 CALL WaitWP // Wait for Twp
P 0067 82 80 197 LDE NowReg, @AdReg // Turn off WE
198 // Now, write the data to the part.
P 0069 92 90 199 LDE @AdReg, DataReg
P 006B D6 0071 200 CALL WaitWP // Wait for Twp
P 006E 82 80 201 LDE NowReg, @AdReg // turn off WE
202
P 0070 AF 203 FinWr: RET //return from routine
204 // End of EEPROM Write Routine
205 //-----
206
207 // Timing routines
P 0071 EC 0A 208 WaitWP: LD RLoop2, #Twp // # of ms to wait
209 // 10-> wait 10 mS.
210 // 1 -> Wait 1 mS.
211
P 0073 D6 007E 212 WPLoop: CALL WaitTms
P 0076 00 EE 213 DEC RLoop2
P 0078 6D 007D 214 JP Z, DunWP
P 007B 8B F6 215 JR WPLoop
P 007D AF 216 DunWP: RET // Done with Twp.
217
218 // Basic 1 msec timing routine-
219 // adjust for microprocessor crystal freq.
220 // The value of Hex5B (Dec88) works with
221 // a Z8 with a 6.144 MHz xtal.
222 // Use %6A for 7.3728 MHz xtal. Elimination
223 // of NOP, or xtal substitution, will
224 // require recalibration.
P 007E FC 6A 225 WaitTms: LD RLoop3, #%6A
226
P 0080 FF 227 Timp: NOP
P 0081 00 EF 228 DEC RLoop3
P 0083 6D 008B 229 JP Z, DunTms
P 0086 8B F8 230 JR Timp
231
P 0088 AF 232 DunTms: RET // Done with wait
233
234 //End of EEPROM Timing Routines
235 //-----

```

Figure 4. Sample Z8 Code for 52BXX Write

## Read Operation

The timing for a read (see Figure 5) is simpler than for a write. In the read mode, the on-chip latches are transparent. The leading (falling) edge of  $\overline{\text{CHIP SELECT}}$  brings  $\overline{\text{CE}}$  low, and the falling edge of  $\overline{\text{MEMORY READ}}$  brings  $\overline{\text{OE}}$  low. Data is available from the 52BXX E<sup>2</sup>ROM after a delay of  $T_{\text{OE}}$  (from  $\overline{\text{OE}}$ ) or  $T_{\text{CE}}$  (from  $\overline{\text{CE}}$ ). Table 1 shows the  $T_{\text{ACC}}$  required for operation with sample microprocessors, using no wait states. Memory devices currently available from SEEQ feature  $T_{\text{CE}}$  as fast as 200 nanoseconds. For certain new microprocessors (for example, the 68000 or 8085A-1) which may require faster access, SEEQ is currently developing memories with access times of 150 nanoseconds or less.

To terminate the read, the rising edge of  $\overline{\text{MEMORY READ}}$  brings  $\overline{\text{OE}}$  high.  $\overline{\text{CE}}$ , however, is dependent only on  $\overline{\text{CHIP SELECT}}$ , and remains active low for the entire microprocessor cycle.

## Considerations for Special Applications

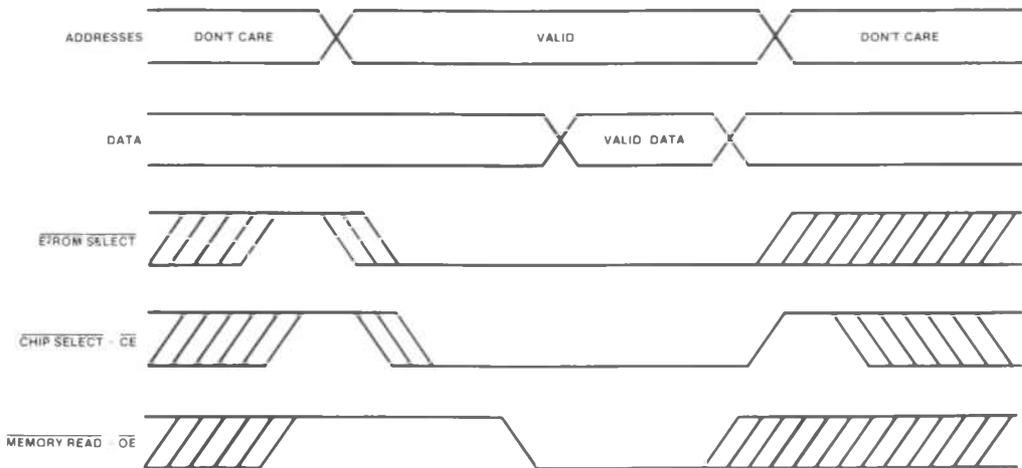
### Use with Z8, Z8000 Systems

The implementation of the circuit shown in Figure 1 in a Z-Bus application allows simple generation of

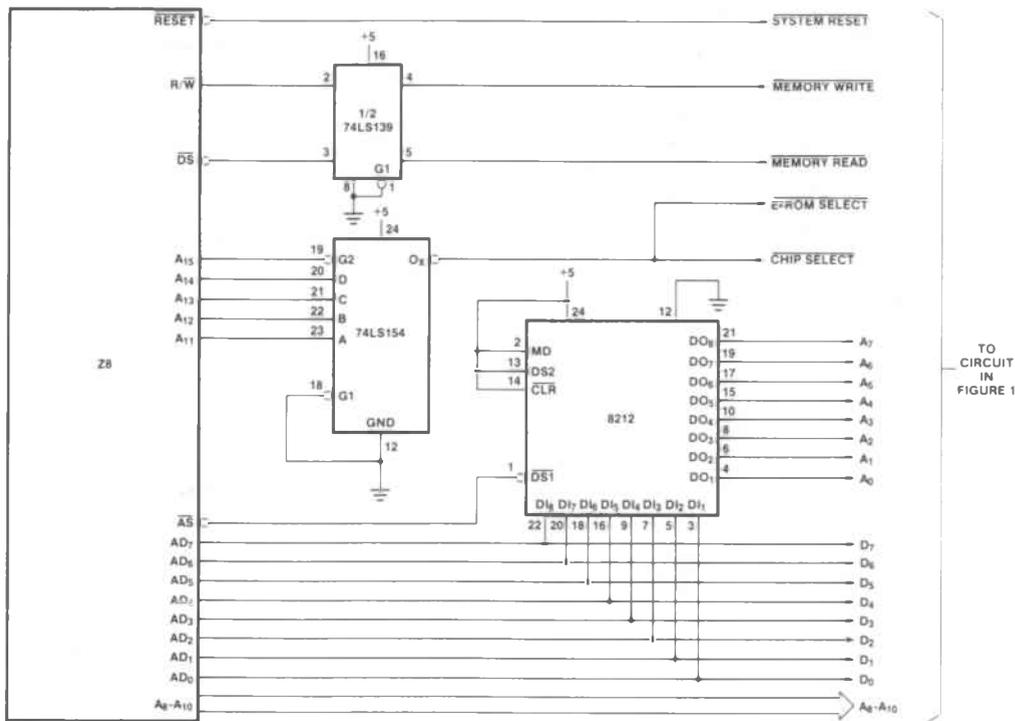
**Table 1. Zero-Wait State Required Minimum  $T_{\text{ACC}}$   
(Assuming zero delay for buffers and drivers)**

Microprocessor	Clock Freq. (MHz)	Required $T_{\text{ACC}}$ (nanoseconds)
72720	10	350
8085A/8085AH	3	460
8085A-2/8085AH-2	5	270
8085A-1/8085AH-1	6	175
8086/8088	5	402
8086-2/8088-2	8	267
8086-1	10	227
Z8	8	310
Z80	2	575
Z80A	2.5	325
Z80B	6	190
6800	1	605

the control signals. First, the control signals  $\overline{\text{MEMORY READ}}$  and  $\overline{\text{MEMORY WRITE}}$  can be generated by one half of a 74LS139 decoder, as in Figure 6. In addition, for the Z8, the lower byte of addresses must be latched, due to the multiplexing of address and data. This can be easily accom-



**Figure 5. Read-Cycle Timing Diagram**



TO  
CIRCUIT  
IN  
FIGURE 1

**Figure 6. Interfacing to a Z8**

plished with an 8212 octal latch, as in Figure 6. Interfacing to a Z8000 (or 16-bit Z-Bus) requires an additional 8212 latch, to demultiplex AD<sub>8</sub>-AD<sub>15</sub>.  $\overline{AS}$ , the Z-Bus address strobe, is active low, and must be connected to the active low input in order to clock these latches.

**Use with Z80 Systems**

The circuit shown in Figure 7 provides a bus interface to a Z80, Z80A, or Z80B processor. In Figure 7, MEMORY READ and MEMORY WRITE are generated from combining MREQ with the Z80  $\overline{RD}$  and  $\overline{WR}$ , respectively. Since address and data are issued by the Z80 processor on separate lines, the 8212 latch is not needed.

**Use with 8085 Systems**

The implementation of the E<sup>2</sup>ROM interface circuit in an 8085 system is extremely simple. Figure 8 shows the bus interfacing necessary. MEMORY READ and MEMORY WRITE are issued by the processor directly. However, MEMORY WRITE must be delayed, as shown in Figure 8, to ensure latching of valid data. CHIP SELECT is generated from the top

5 address bits and IO/ $\overline{M}$ , using a 74LS154 decoder. The RESET to the 8085 processor also supplies RESET for the E<sup>2</sup>ROM interface. Finally, the demultiplexing of address and data lines is accomplished by a 74LS373 latch triggered by ALE. Alternatively, an 8212 latch can be used but requires more board space.

**Interfacing to 8088/8086 (Minimum Mode) Systems**

The above considerations for implementation of this solution in an 8085 system also apply to an 8088/8086 system operation in minimum mode, with two additions. As above, the processor issues ALE,  $\overline{RD}$ ,  $\overline{WR}$ , and multiplexed address/data. However, an inverter is required in order to produce IO/ $\overline{M}$  from M/ $\overline{IO}$ . In addition (for an 8086), another octal latch must be added, in order to demultiplex AD<sub>8</sub>-AD<sub>15</sub>.

The time delay indicated in Figure 8 depends on the type of processor used and its clock frequency. For a 5 MHz 8088/8086, this time delay should be 100 nanoseconds; for an 8088-2/8086-2 at 8 MHz, it should be 60 nanoseconds. For a 10 MHz 8086-1, the time delay should be 50 nanoseconds.

APP. NOTES

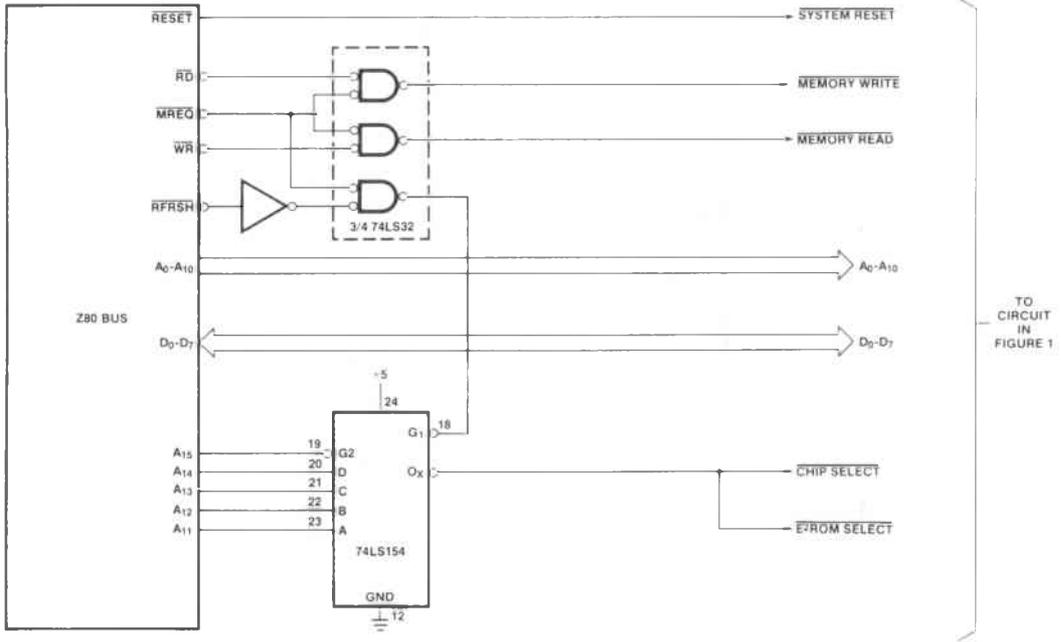


Figure 7. Bus Interface — Z80

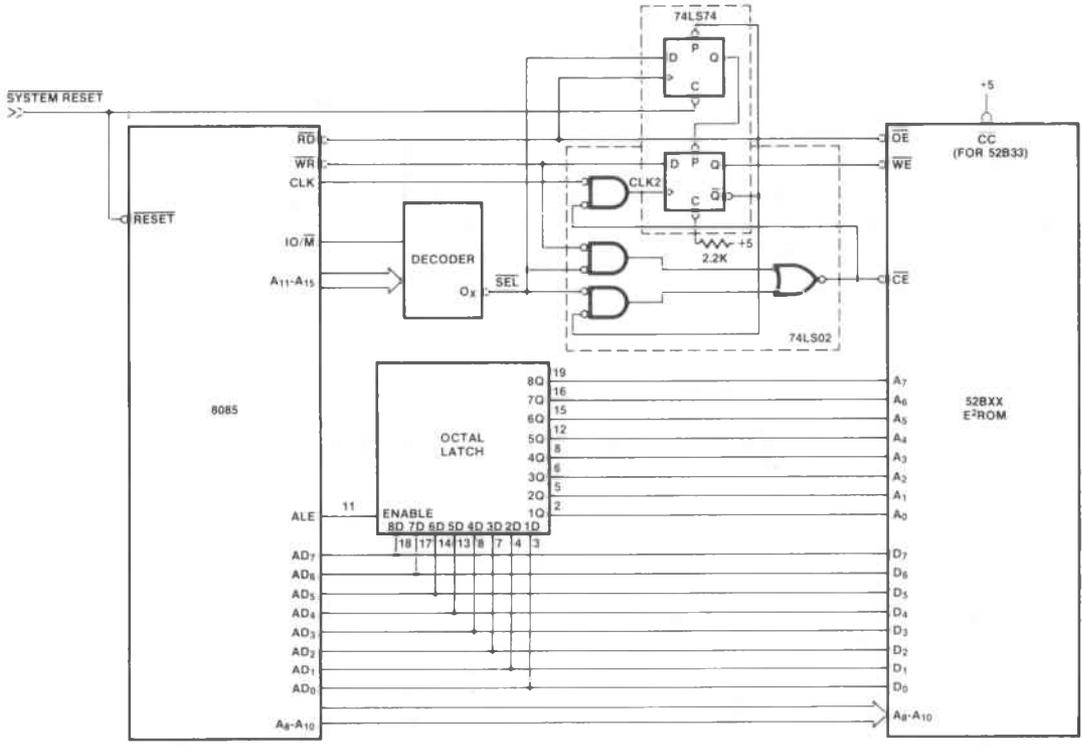


Figure 8. Bus Interface Circuitry — 8085 System

## Interfacing with 72720 Systems

The 52BXX E<sup>2</sup>ROM can be interfaced to SEEQ's new 72720 microcomputer (with 2K x 8 on-board E<sup>2</sup>ROM) more easily than to any other processor. The 72720 PRG instruction operates off-board, to program an external E<sup>2</sup>ROM. This instruction initiates latching and timing of  $\overline{WE}$ , as well as presentation of valid data. These tasks are handled automatically within the 72720. As a result, the write enable latch circuit of Figure 1 is not required. Total 52BXX interface hardware, shown in Figure 9, is very simple, even including a 74LS373 latch to demultiplex the lower eight bits of address. The software required for programming is shown in Figure 10. This example subroutine erases and writes one byte.

## Interfacing with the 6800

One example of a complete interface between a 6800 processor and a 52BXX is shown in Figure 11. The DBE signal from the 6800 is delayed for a time between 250 and 350 nanoseconds, in order to provide a strobe for valid data. This data strobe clocks

R/ $\overline{W}$  into the flip-flop at the correct time, so that the falling edge of  $\overline{WE}$  can satisfy timing requirements with respect to valid address, data, and control signals.

## Conclusion

This application note has been prepared to assist the designer in implementing the technology of latched E<sup>2</sup>ROMs in systems requiring adaptability. The designer is encouraged to create new designs based on these ideas. E<sup>2</sup>ROM technology, while still in its infancy, holds the promise of being the memory breakthrough for the eighties. With a reliably non-volatile approach to alterable program memory, systems for control of avionics, manufacturing, and data acquisition can be enhanced in usefulness. With the timing to use the advanced technology of E<sup>2</sup>ROMs, the system designer can incorporate more features now, while allowing still more flexibility for the future.

Z-Bus, Z8, Z8000, Z80A, Z80, and Z80B are trademarks of Zilog.

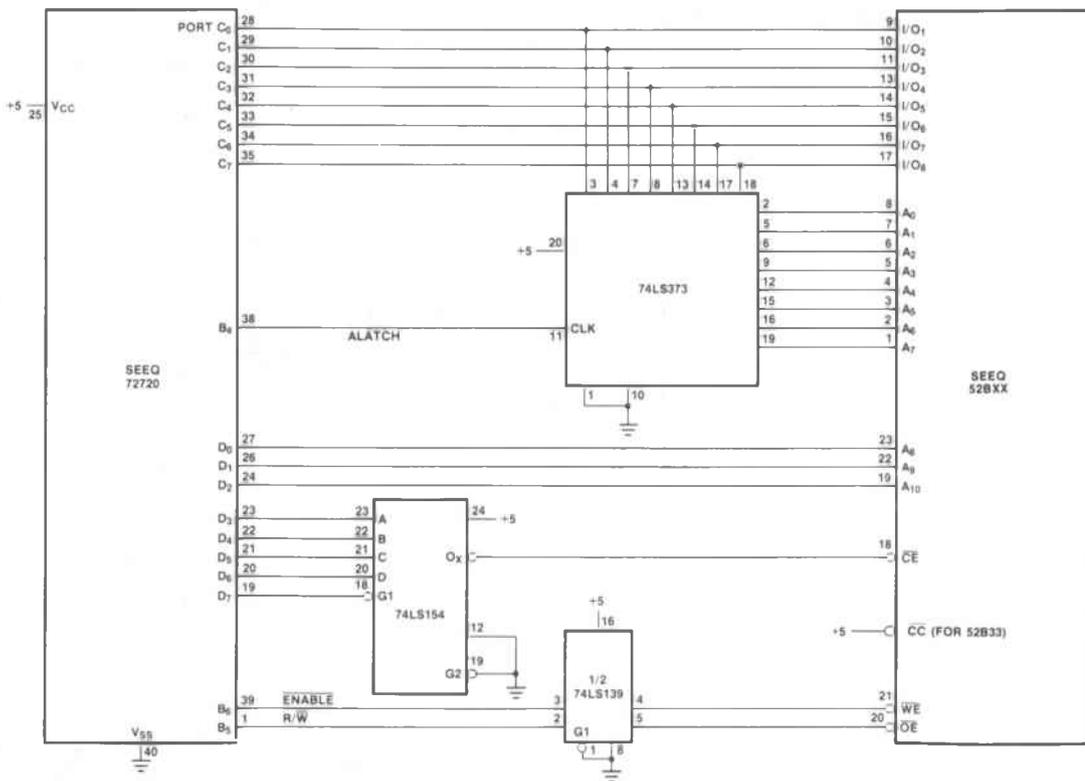


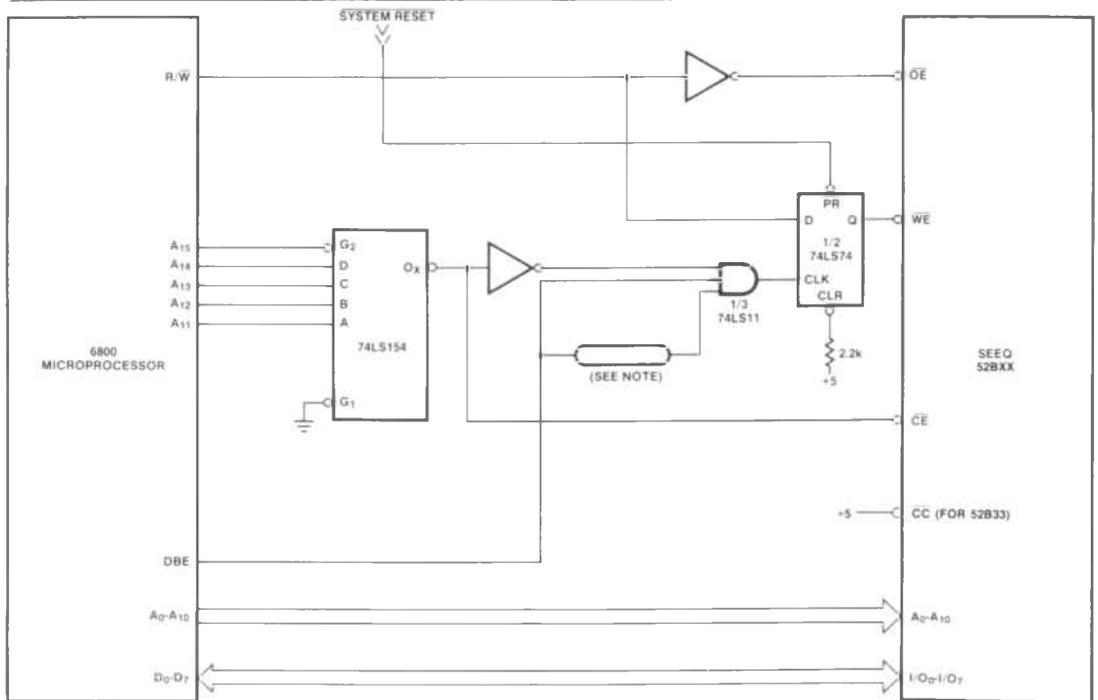
Figure 9. 72720 Interface

```

0 ERRORS
7000 ASSEMBLER REV 1.3
>
0001 9000 *****
0002 9000 *
0003 9000 *          EEROM AUTO ERASE BEFORE WRITE ROUTINE
0004 9000 *
0005 9000 *          DATA TO BE PROGRAMMED IN REGISTER 102
0006 9000 *          LOCATION TO BE PROGRAMMED IN REGISTERS 100/101
0007 9000 *
0008 9000 *****
0010 9000 *
0020 9000 0066 EEDAT EQU R102      DATA TO BE PROGRAMMED
0030 9000 0065 EEADR EQU P101     POINTER TO LOCATION
0040 9000 B8   EEWR  PUSH A       SAVE ACCUMULATOR
0050 9001 22   MOV  %>FF,A      IS LOCATION ALREADY ERASED?
      9002 FF
0060 9003 9D   CMPA *EEADR
      9004 65
0070 9005 E2   JEQ  PROG
      9006 00
0080 9007 04   PRG  *EEADR      IF NOT PROGRAM WITH FF HEX
      9008 65
0090 9009 12   PROG MOV EEDAT,A  IF ERASED PROGRAM DATA
      900A 66
0100 900B 04   PRG  *EEADR
      900C 65
0110 900D B9   POP  A          RESTORE ACCUMULATOR
0120 900E 0A   RETS          RETURN
0130 900F     END
<

```

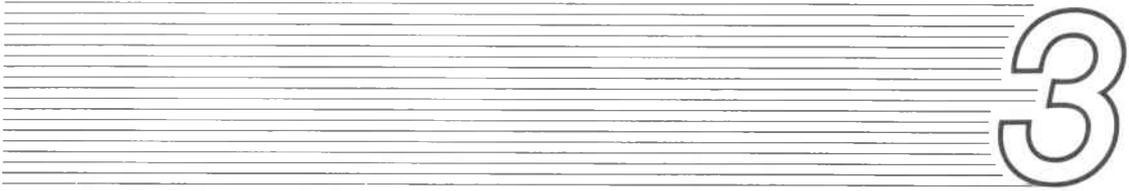
Figure 10. 72720 Code for Programming 52B13/33



NOTE: THIS ELEMENT OF THE CIRCUIT SHOULD DELAY A RISING EDGE (A TTL LOW-TO-HIGH TRANSITION) BY 250 (MIN) TO 350 (MAX) NANoseconds.

Figure 11. 6800/52BXX Interface

**Micro Products  
Application Note**



**3**

**72720 DESIGN BOARD  
APPLICATION NOTE**

*April 1987*

APP. NOTES

**seeq**  
*Technology, Incorporated*

# 72720 E<sup>2</sup> ADAPTABLE SINGLE BOARD COMPUTER

There is a new generation of microprocessors now in the marketplace that have the capability to learn and alter their own program. Many of us have learned that dynamically changing code is not good programming practice, but in some cases it can be very useful. For example, a microprocessor controlling a mechanical device can alter its program to compensate for the mechanical wear that occurs over time. One part that has this ability is the SEEQ 72720 E<sup>2</sup> microprocessor. To help in evaluation of this new technology, SEEQ has developed a board that can program slave devices or can be used as a stand alone controller.

## GENERAL DESCRIPTION

The 72720 Design Board demonstrates the capabilities of the SEEQ 72720 Self-adaptive EEPROM Microcomputer. The board functions as a stand alone computer or controller and it can be used to program EEPROM's or other 72720's. It can communicate with a terminal or a host computer through two RS-232 ports and it has two 25 pin I/O connectors for controlling other external applications. Information and programs can be transferred to and from a host computer by using commands from the Design Board Monitor. Use of E<sup>2</sup> non-volatile memory allows incremental debugging and development without continuous uploading and downloading.

### 72720 Controller

At the heart of the Design Board is the SEEQ 72720 Microcomputer. It is based on the TMS 7000 family of microprogrammed computers. The 72720 has 2K bytes of EEPROM on chip that can be self programmed or slave programmed by a system such as the design board. The processor has 256 bytes of RAM, a 13 bit Timer, 4 levels of interrupts and a Security Lock feature that prevents unwanted access to internal programs.

### Processor Instructions

The 72720 shares the standard instruction set of the TMS 7000 series with an additional instruction to program internal or external EEPROMs. There are 61 instructions including Binary and BCD arithmetic, an 8 \* 8 multiply, logical instructions, bit tests of memory or I/O, load/move instructions and I/O instructions. Address modes include Register file addressing, Peripheral file Addressing, Immediate, PC relative, Direct, Indirect and Indexed.

### Design Board Hardware

The complete Design Board Hardware consists of the CPU, 6 memory chips, 2 port chips and 8 TTL glue chips. Only a subset of these chips are needed for a minimal system. To run BASIC, the parts needed are: the program ROM, a RAM, the CPU and the glue chips. To use the Slave programming utilities, an 8155 and a socket for the slave need to be added. The additional memories are for non-volatile program storage and the 8255 expands the I/O capabilities. Depending on the choice of memory and glue chip technology, the board can be set up to run on low power or high speed operation (16 MHz clock rate).

Two sockets are set up to be low insertion force sockets for programming Slave 72720's and 64k EEPROMs. All memories can be write protected by use of jumpers.

### Design Board Monitor

The Design Board Monitor is a collection of utilities to aid in developing programs for loading into the 72720. On power up the Baud rate is determined from a Carriage Return from the terminal. A command can then be entered and executed. From the monitor you can call up routines to download assembly language programs from a host computer in several different

formats. These programs can be modified or moved to different EEPROMS. By entering the slave programming mode, a slave 72720 can be cleared, programmed or read. Also resident in the monitor is a special version of Tiny Basic. For controller applications, programs can be written quickly in the Higher level language and can then be tuned by replacing sections with assembly language code that can be executed from within Basic. There are special Basic commands that allow storage and retrieval of Basic programs from non-volatile memory.

#### Applications

The Design Board can be a platform for many applications that demonstrate the utility of EEPROMs and EEPROM microprocessors. It can be used to implement an Adaptable Controller whose program can be altered depending on environmental stimulus. The system can be used as a stand alone computer when connected to a terminal or it can be a remote slave controller communicating with a master or host computer over the RS-232 link. Finally it provides a means to slave program 72720's for use in other

systems or program any EEPROM in a 28 pin package.

#### 72720 DESIGN BOARD

The 72720 Design Board can be used to program other 72720 chips and it also functions as a stand alone computer or controller. It can communicate with a terminal or a host computer through two RS-232 ports and it has two 25 pin I/O connectors for controlling other external applications. Information and programs can be transferred to and from a host computer by using commands from the Design Board Monitor.

The complete Design Board Hardware consists of the CPU, 6 memory chips, 2 port chips and 8 TTL glue chips. Only a subset of these chips are needed for a minimal system. To run BASIC, the parts needed are: the program ROM, a RAM, the CPU and the glue chips. To use the Slave programming utilities, an 8155 and a socket for the slave need to be added. The additional memories are for non-volatile program storage and the 8255 expands the I/O capabilities. (See board layout and schematics for additional information).

#### DESIGN BOARD MEMORY MAP

0000-00FF	72720 RAM (256 BYTES)	
0180-0185	8155 REGISTERS	†
0200-02FF	8155 RAM (256 BYTES)	
0800-0803	8255 REGISTERS	
1000-1FFF	2 * 2K X 8 EEPROM	
2000-3FFF	8K X 8 RAM	*, †
4000-5FFF	8K X 8 EEPROM (SPACE ON PC BOARD FOR ZIF SOCKET) (REMOVABLE FOR STORING BASIC PROGRAMS)	
6000-7FFF	8K X 8 EEPROM	
8000-FFFF	SYSTEM EPROM (72720 EEPROM NOT ACCESSIBLE)	*, †

IC sockets at locations A6 and A20 should be low insertion force sockets. A20 is where a slave 72720 can be programmed for use in another system. This part can also execute a program in Single Chip mode while in this socket and can communicate with the Main processor through the 8155 port chip. The EEPROM at A6 is used to save BASIC programs and it can be removed if it becomes filled (up to 255 programs) or if a program needs to be copied into

several memories. A program stored in RAM will not be destroyed if this part is changed while holding the reset button.

There are a number of jumpers for options on the board and to Write Protect the E<sup>2</sup> memories. JP 4-7 and JP15 are used to enable RAMs or E<sup>2</sup> memories. When they are removed, the chips' Write Enable line is pulled high through a resistor.

\* PARTS NEEDED FOR BASIC

† PARTS NEEDED FOR SLAVE PROGRAMMING

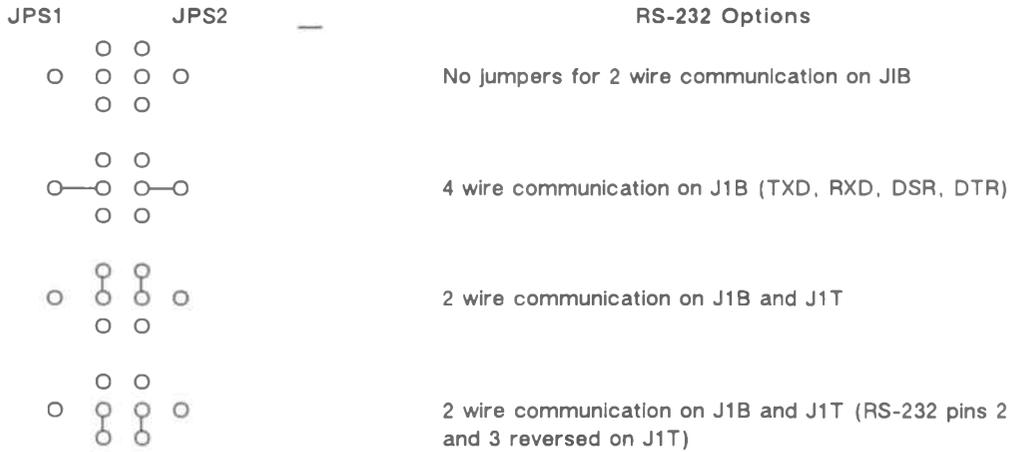
Below is a list of the Jumpers:

JP4	Write Enable	A4	
JP5	Write Enable	A5	
JP6	Write Enable	A6	
JP7	Write Enable	A7	
JP15	Write Enable	A15, A16	
JP4A	O---->	A6 pin 1	Jump top posts for 256K EEPROM
	O---->	Addr. 14	
	O---->	A6 pin 27	Jump bottom posts for 256K EPROM

Neither jumper need be on for 64K parts

JP13 is reserved for future use and is presently a Don't Care.

J2 and J6 can be used for connecting to the 72720 APORT and BPORT lines or can be jumped to ground for signalling other options to the 72720. (APORT lines have internal pull ups.)



There are two LED's on board to indicate Power On and Slave programming in progress. If the proper program is on board, then a terminal is not needed to program slaves. The Slave Program LED will come on when a Slave is being programmed and will go out when it is OK to remove the part.

### 72720 DESIGN BOARD MONITOR

The Design Board Monitor is a collection of utilities to aid in developing programs for loading into the 72720. On power up the Baud rate is determined from a Carriage Return from the terminal. A command can then be entered and executed.

#### COMMANDS:

BA	Start Basic. See SEEQ E <sup>2</sup> BASIC Document for more information.
SP	Slave mode Programming. See Design Board Programmer document for more information.
DT	Download (TI format). Accepts a .MPO file from host system and loads it into RAM. The data can then be block moved somewhere else (using MV) or it can be moved into a Slave 72720 using SP.
DH	Download (Cybernetic format). Accepts a .HEX file from host system and loads it into RAM. The data can then be block moved somewhere else (using MV) or it can be moved into a Slave 72720 using SP.

(Continued on next page)

**COMMANDS:**

BT	Download (TI format). Accepts a .MPO file from host system and loads it into RAM or E <sup>2</sup> starting at the AORG address.
BH	Download (Cybernetic format). Accepts a .HEX file from host system and loads it into RAM or E <sup>2</sup> starting at the AORG address.
UT <SRC_STRT> <SRC_END>	Upload (TI format). Uploads data to host system for storage.
UH <SRC_STRT> <SRC_END>	Upload (Cybernetic format). Uploads data to host system for storage.
DM <STRT> <STOP>	Display data from start to stop in hex.
MM <ADDR>	Display/Modify Memory at ADDR. Space or + will step to next location, - will decrement address to be displayed. <CR> to terminate.
MV <SRC_STRT> <SRC_END> <DEST_STRT>	Move data block between SRC_STRT and SRC_END to DEST_STRT.
EX <ADDR>	Execute assembly language program at ADDR. Program should end with RETS to get back to Monitor.
U0-7	8 commands are available for User definable routines.

A scrolling display can be frozen by using ^S and started again using ^Q. Most routines in progress can be terminated by ^C.

**SEEQ E<sup>2</sup> BASIC**

SEEQ E<sup>2</sup> BASIC is based on Palo Alto Tiny Basic with extensions to read and write EEPROM for program/data storage. There are also extensions to PEEK any memory location and POKE

RAM or EEPROM and to run assembly language subroutines. Below is a list of commands and their formats. This is followed by a more detailed description of each command and the BASIC structure.

**Direct Commands:**

```

NEW
LIST [<start line #>] [, <# of lines>]
RUN [<line #>]
EECLR

Direct/Program Commands:
[LET] <variable> = <expression>
PRINT [<expression or string>] [, ... ]
INPUT ['<string>'] <variable> [, ... ]
IF <expression> ...
GOTO <expression>
GOSUB <expression>
RETURN
GOASM <address>
FOR <variable> = <start expr> TO
<stop expr> [ STEP <expr> ]
NEXT <variable>
STOP
REM ...
POKE <address>, <data>

```

**Direct/Program Commands: (Con't)**

```

SAVE <index #> [, <start line #>]
[, <# of lines>]
LOAD <index #> [, ... ]
DELETE <index #>
INDEX
EXIT

Arithmetic/Compare:
+, -, /, *, ( ), =, #, <, >, <=, >=.
```

**Functions:**

```

ABS (<expression>)
RND (<expression>)
SIZE
PEEK <address>
```

**Notes:**

[ ] denotes optional field  
All commands can be abbreviated as shown in Table 1

## BASIC Basics

SEEQ BASIC will signal it is ready by the prompt 'OK' and '>'. Direct commands or a program can then be entered in from the keyboard. A Basic program consists of statements which are made up of a line number followed by one or more commands. Line numbers can be between 1 and 32767. Commands in the same line are separated by a semi-colon. The commands GOTO, STOP and RETURN cannot be followed by another command. Commands entered without a line number will be executed immediately and the semi-colon will concatenate commands together in this mode also. The commands NEW, LIST, RUN, and EECLR can only be used directly; they can't appear in a program.

## Numbers, Variables and Arithmetic

All numbers are integers between 32767 and -32767. There are 26 variables denoted by the letters A through Z and an array variable @(idx) where the range of the index is set to make use of all memory space that is left unused by the program (i.e. 0 through SIZE/2, see SIZE function later). Variables are not initialized automatically so they should be initialized within the program.

Expressions are formed with numbers, variables and functions with arithmetic and/or compare operators between them. The expression is evaluated from left to right with \* and / done

first, + and - next and compare operators done last. Parentheses can be used to alter the order of evaluation. The result from a comparison will be 1 if true or 0 if not true. The division result will be truncated to an integer.

Hexadecimal numbers can be mixed in with integers in expressions. A Hex number is preceded by % sign (e.g. %FC00 or %9A). The Hex numbers range from %0 to %7FFF (decimal 0 to +32767) and %8001 to %FFFF (decimal -32767 to -1). The value %8000 is illegal in expressions but it can be used as an address in PEEK, POKE and GOASM. If there are more than four hex digits, then only the last four are used.

## Error Messages

There are 3 main error conditions in SEEQ BASIC. The statement that contains an error is printed out with a question mark inserted at the point where the error is detected. WHAT? means it doesn't understand you. For example, if a command is misspelled or a parenthesis is missing. HOW? means it understands you but it does not know how to do it. For example if there is arithmetic overflow or if you GOTO a line number that doesn't exist. SORRY means there is not enough room in memory to store something. There are other error messages when using the E<sup>2</sup> commands and these will be explained later.

## COMMAND DESCRIPTIONS

### Direct Commands:

#### NEW

Will clear any previous program from memory.

#### LIST [<start line #>] [, <# of lines>]

Will print out the program listing. The first parameter will give the starting line number (default = 0). The second parameter is the number of lines listed (default = 32767). With no parameters the whole program will be listed.

#### RUN [<line #>]

Starts execution at the specified line number or the next one found if <line #> doesn't exist (default = lowest line #).

#### EECLR

This will initialize an EEPROM for program/data storage. It will first prompt SURE? (Y/N). If you type Y it will continue, anything else will abort the command. If there is not an EEPROM or a RAM in the socket it will return the error message: NOT FOUND.

### Direct/Program Commands:

[LET] <variable> = <expression> [, <variable> = <expr.> ...]

Will assign the evaluated expression to a variable. The word 'LET' can be omitted, e.g. LET A=2 is the same as A=2. Multiple assignments can be made by separating with ','.

PRINT [<expression or string>] [, ...]

Will output a number or a string to the terminal. Multiple items can be separated by commas and extra spaces can be generated by commas. A number is printed with leading blanks so they take 8 spaces each. This field width can be changed by '#' followed by a number indicating a new width. The new width is effective until the end of the PRINT command unless another # is found. Strings are delimited by matching pairs of '"' or '''. For example PRINT 3/2-4, 5, 'STRING EG "#!", #3, B

*(Continued on next page)*

## COMMAND DESCRIPTIONS (Con't)

will result in the output:

```
-3      5STRING EG "#! <the value of B in 3
spaces> In this example, B could take more
spaces if it was > 999 or < -99. The PRINT
statement will end with a carriage return
unless the list ended with a ', ' in which case
the next PRINT statement will resume
printing where the last left off.
```

**INPUT** ['<string>'] <variable> [, ...]

Will input an expression from the keyboard and assign it to a variable. Basic will prompt with '<string>' or the variable if no string is specified. Other variables can be input by using commas. For example: INPUT 'ENTER VOLUME' V will prompt: ENTER VOLUME . The statement: INPUT V will prompt: V<space> If you type: 3\*8\*4 <return> it will assign the value 96 to V.

**IF** <expression> ...

If the expression is evaluated to be zero, the rest of the line will be skipped. Otherwise, the rest of the commands in the line will be executed. The result of a comparison using =, #, <, >, <=, >=, will be 1 if true, 0 if false. These operators are not always needed. For example the statement: "IF A ..." is the same as: "IF A # 0 ..." (# means not equal). The "..." stands for the commands following the IF statement. Note that the word THEN is not used.

**GOTO** <expression>

Will number evaluated in expression. This line number must exist and GOTO can not be followed by more commands.

**GOSUB** <expression>

This will also jump to <expression> line number but when the called routine encounters a RETURN, execution continues from the command following GOSUB.

**RETURN**

The program will jump back to the command following the most recent GOSUB. This command cannot be followed by others in the same line. Subroutines can be nested with the depth limited by the external Stack Space.

**GOASM** <address>

This command is like GOSUB except that it will call a 72720 Assembly language routine anywhere in the processors' memory

space. This can be used to do special functions or to increase the speed of a particular operation or calculation. Assembly language subroutines, PUSHes and POPs are limited by the Internal Stack space of about 150 locations. To transfer control back to Basic, the assembly language routine should end with a RETS opcode. The Address can be an expression or it can be a Hex value, e.g. GOASM %FC0A.

**FOR** <variable> = <start expr> TO <stop expr> [ STEP <expr> ]

This initializes a loop that is terminated by a NEXT statement. When a FOR is first encountered, the specified variable is set to the evaluated start expression. When NEXT is encountered, the optional STEP value (default = + 1) is added to the variable and the program jumps back to the command following the FOR. This repeats until the variable equals or exceeds the stop expression. The loop is always executed at least once. There can only be one NEXT for each FOR. FOR loops can be nested with the depth limited by the external Stack space.

**NEXT** <variable>

Terminates the FOR loop

**STOP**

Will stop execution of Basic program and return to the Direct mode.

**REM**

This command is ignored by Basic. It is used to comment the program or insert data.

**POKE** <address>,<data> [ <data> ... ]

Will write the specified data into a RAM or EEPROM at the specified address. Both the address and data can be an expression or a Hex constant. Multiple bytes of data can be POKEd into sequential locations starting at <address>.

**EXIT**

Stop BASIC and return Monitor

**EEPROM Commands**

**SAVE** <index #> [, <start line #>] [, <# of lines>]

Will save all or a portion of the present program. The format is similar to LIST except an index number needs to be specified for future access to the entry. The index number must be between 0 and 255 and

*(Continued on next page)*

## COMMAND DESCRIPTIONS (Con't)

If there is not enough room in EEPROM for the data being saved an error message is returned saying: E<sup>2</sup> OVERFLOW. If the data just fits or if you are using the 255th entry, a warning message is sent saying: E<sup>2</sup> FULL . If the SAVE command was being used in a program, execution will continue in this case. If no Index is specified an error message is returned saying: WHERE? The saved statements must have line numbers, but they do not have to be executable commands. If they appear in the program after a STOP or a GOTO loop then these lines can be text or data that can be LOAded, modified and SAVEd under program control.

LOAD <Index #> [, ... ]

Will load the specified entry (or entries) from EEPROM and place in the present program. Statements with line numbers that match line numbers in the loaded program will be lost as the loaded program overwrites them. If an Index is specified that doesn't exist in the EEPROM then an error message will be returned saying: NOT FOUND.

DELETE <Index #>

Will delete an entry from the EEPROM. If an Index is specified that doesn't exist in the EEPROM then an error message will be returned saying: NOT FOUND. This command modifies all data saved in the EEPROM. In the worst case (deleting an entry from the bottom of a full EEPROM) it can take up to 4 minutes to execute.

### INDEX

Will print the Index number followed by the first line of the saved entry for every item in the EEPROM. The first line SAVEd should be a REM statement describing the entry.

### Functions

ABS (<expression>)

Gives the Absolute value of the expression

RND (<expression>)

Gives a random number between 1 and <expression> inclusive

SIZE

Gives the number of bytes of RAM left unused by the program.

PEEK (<address>)

Returns the contents (in decimal) of the specified memory location. Address can be an expression or Hex constant.

### Command Abbreviations

All commands can be abbreviated with a period. The minimum required abbreviations are shown in Table 1 along with the recommended minimum to uniquely distinguish each command. Basic

recognizes the command containing the minimum required letters up to the full spelling. For example; P., PR., PRI. and PRIN. all stand for PRINT. The command LET can be omitted entirely.

TABLE 1. COMMAND ABBREVIATIONS

COMMAND	MINIMUM REQUIRED	MINIMUM RECOMMENDED
NEW	N.	N.
LIST	.	.
RUN	R.	R.
EECLR	E.	E.
LET	LE. (or omit)	(omit)
PRINT	P.	PR.
INPUT	IN.	IN.
IF	I.	IF
GOTO	G.	GOTO
GOSUB	GOS.	GOS.
RETURN	R.	RET.
GOASM	GOA.	GOA.
FOR	F.	FOR

(Continued on next page)

**TABLE 1. COMMAND ABBREVIATIONS (Con't)**

COMMAND	MINIMUM REQUIRED	MINIMUM RECOMMENDED
NEXT	.	NEXT
STOPS	.	ST.
REM	REM	REM
POKE	PO.	PO.
SAVE	SA.	SA.
LOAD	LO.	LO.
DELETE	D.	DEL.
INDEX	IND.	IND.
EXIT	EX.	EX.
ABS	A.	ABS
RND	.	RND
SIZES	.	SI.
PEEK	P.	PE.

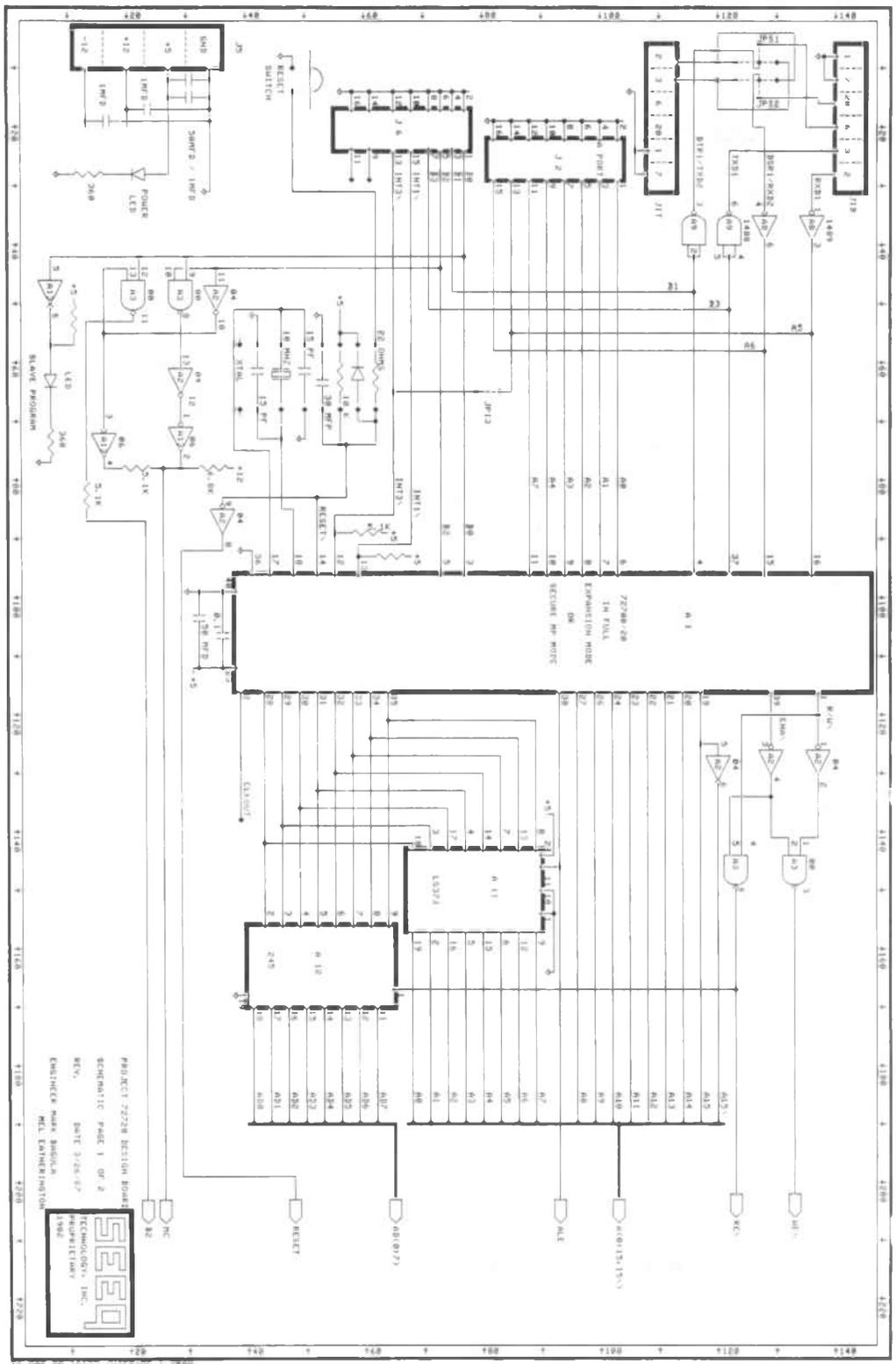
**72720 DESIGN BOARD PROGRAMMER**

Program can be entered from the monitor with the command "SP" (Slave Programming) or a basic call; GOASM %F200. Before each test is executed, a routine will determine what part is in the programming socket; 72710 or 7272X.

After test is complete, typing carriage return will bring up a short menu of commands available (TYPE B V F C W H Z OR S). Typing any other key will repeat the same test again. (Parameter for the V test must be reentered in case a different section is wanted). Any input sequence can be aborted with ^C. This will bring up the menu again.

COMMANDS:	
B SSSS XXX DDDD	Block move XXX bytes of data from SSSS in main memory into E <sup>2</sup> at DDDD (all values HEX).
V X	Read (verify) a 256 byte section of E <sup>2</sup> . X range: from 0 to 7 and determines which section to display (e.g. V 7 will display from FF00 to FFFF).
F XX	Fill E <sup>2</sup> with XX (HEX)
C	Block Clear then verify all one's.
W	Block Write then verify all zero's.
Z	Verify all zero's. Reads E <sup>2</sup> and prints the address of any bad location if any.
H	Verify all one's. Reads E <sup>2</sup> and prints the address of any bad location if any.
T	Trace Write. Accepts 16 characters for input into Traceability E <sup>2</sup> . If test is repeated, only last four digits need to be entered.
R	Trace Read. Prints Trace information.
S	Stop exerciser and return to Monitor.

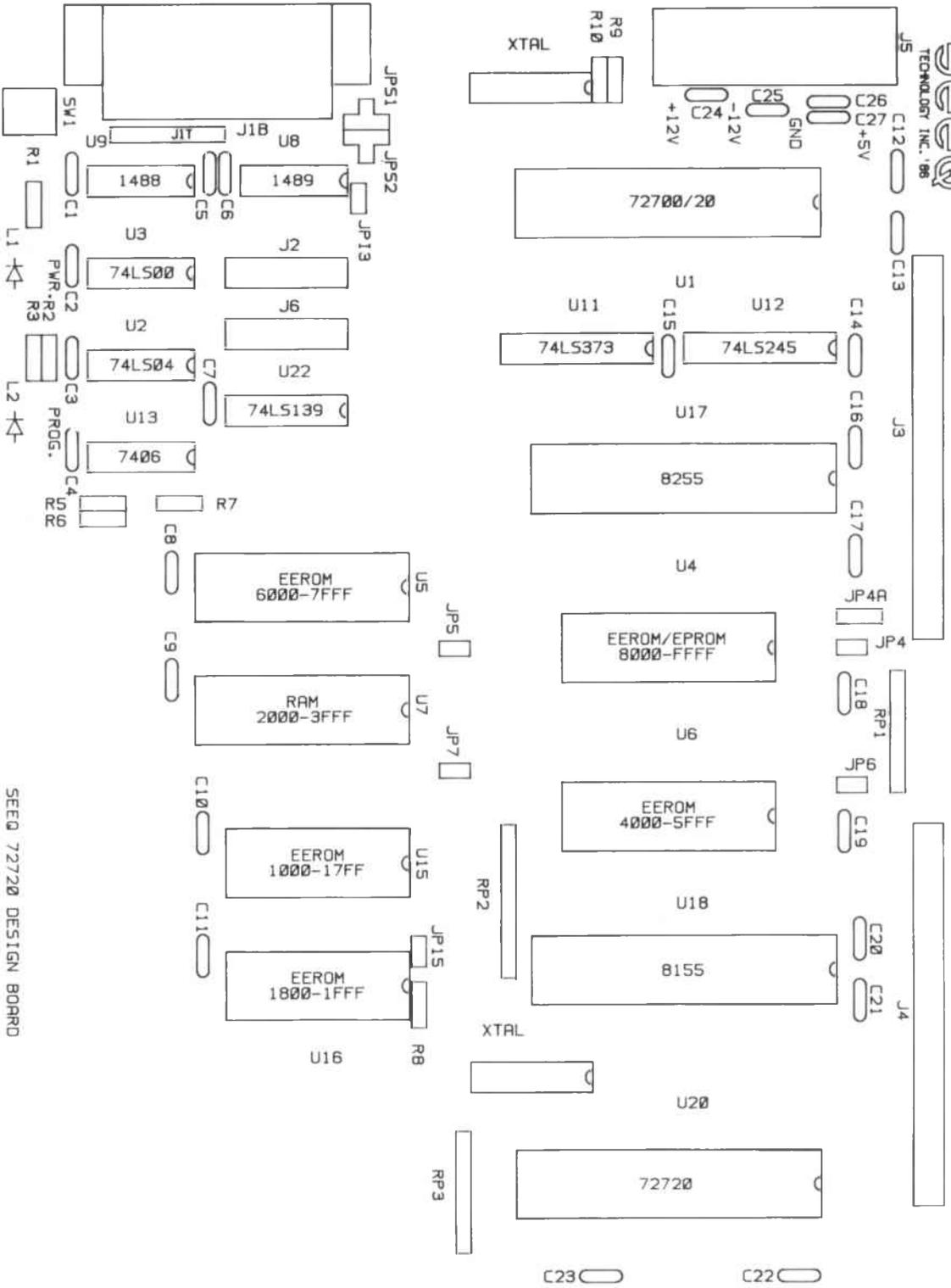
APP. NOTES



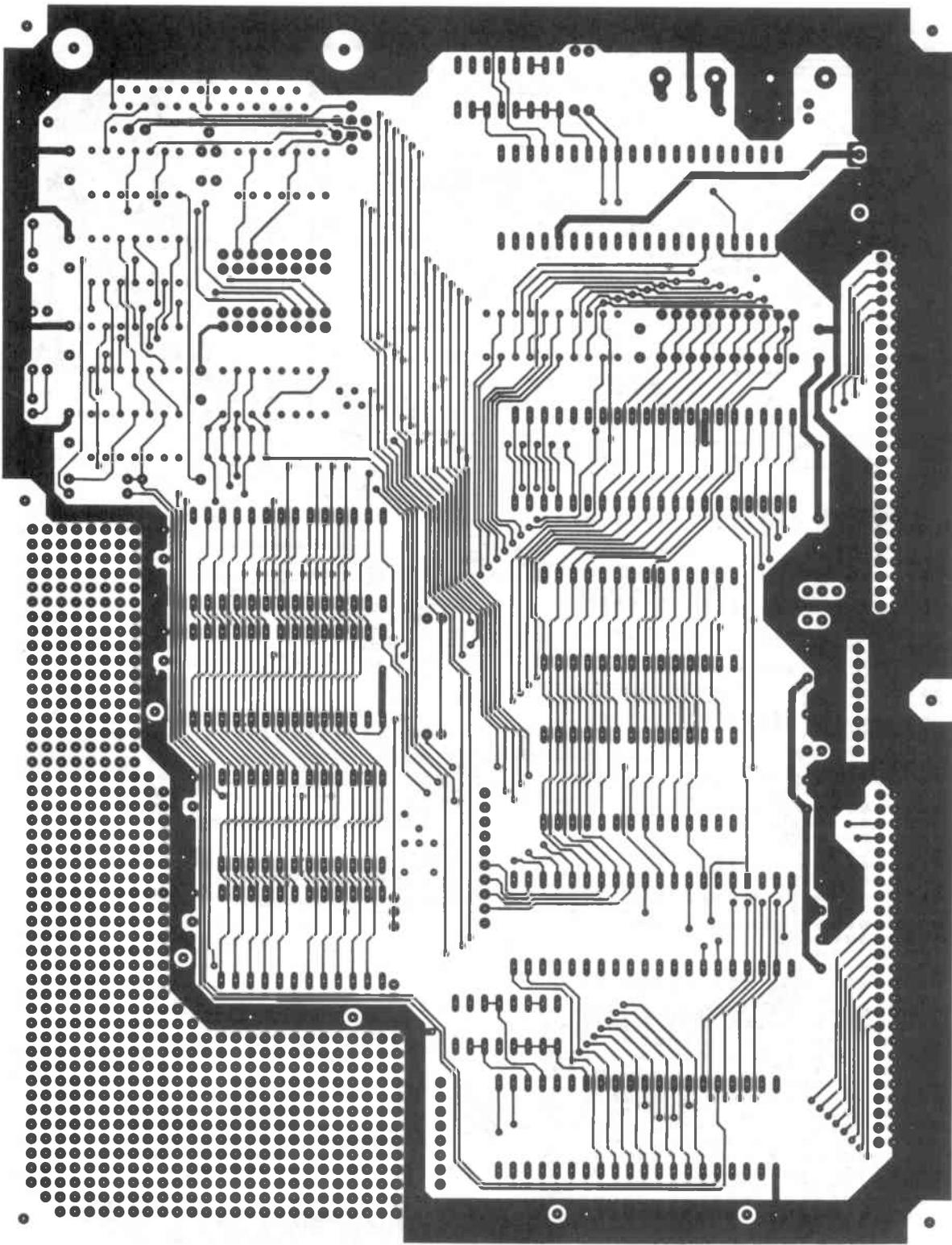
PROJECT 7228 DESIGN BOARD  
 SCHEMATIC PAGE 1 OF 2  
 REV. DATE 3/28/87  
 ENGINEER MARK BISSON  
 MCL ENGINEERING  
 1982



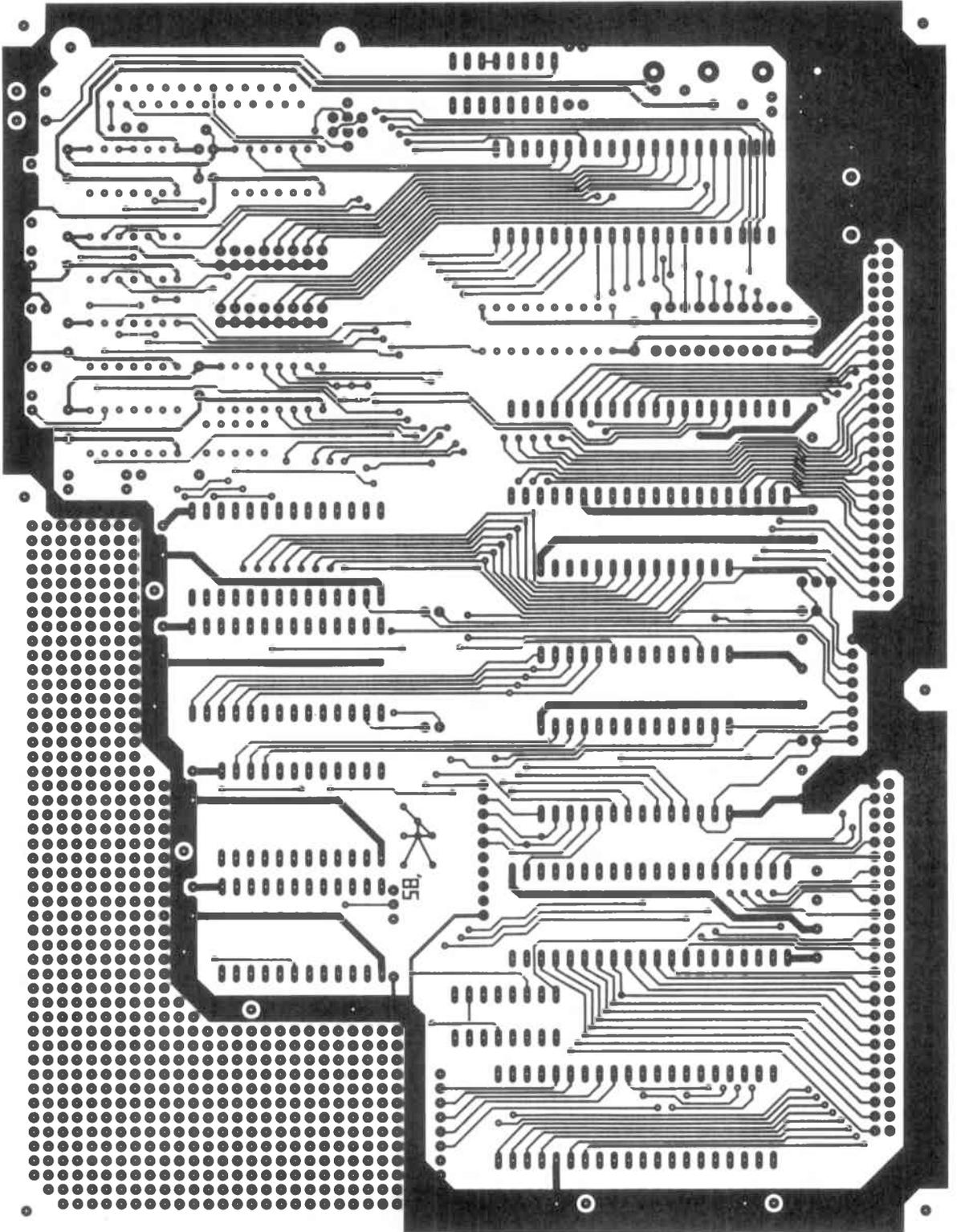




SEEQ 72720 DESIGN BOARD



APP. NOTES



ICs:	RESISTORS:
MOS:	360 1K 5.1K 6.8K 10K 22
72700 72720 8255 8155 27C256 2864 2816A 6264	SIP RESISTORS: 1K 8 pin 10K 8 pin 10K 10 pin
LOGIC:	CONNECTORS:
74LS245 74LS273 74LS139 74LS139 74LS04 7406 74LS00 1488 1489	RS-232 Female Right Angle IDC Cable Shorting Blocks "Snapable" Headers 24xP40 Straight Leadp
CAPACITORS:	MISCELLANEOUS:
1uf 35v 20% Tantalum electrolytic 10uf 20v 20% 47uf 35v 20% .1uf 50v 20% 15pf MICA	XTAL: 10MHZ DIODE: IN4148 LEDS: MINI RED, Led Holders MEMORY: RAM, HITACHI, HM6264-12 SWITCH: Pushbutton

TABLE 2. 72720 DESIGN BOARD PARTS LIST



**Communications Products  
Application Brief**



**5**

**INTERFACING  
THE 8003 EDLC™  
TO A 16-BIT BUS**

*March 1985*

APP. NOTES

**seeq**

*Technology, Incorporated*

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# Interfacing the 8003 EDLC™ to a 16-Bit Bus

## Introduction

The SEEQ 8003 Ethernet Data Link Controller (EDLC™) chip together with the SEEQ 8023A Manchester Code Converter (MCC™) chip provide an economical two-chip solution for the Data Link Layer and Physical Layer of the Ethernet protocol. These chips are fully Ethernet compatible and suitable for use in terminals, personal computers, workstations, printers, disk drives and host computers.

The 8003 is a VLSI data link controller chip in a 40-pin package. It replaces approximately 60 MSI and SSI components in a typical Ethernet node configuration. The choice of which one to use is governed by the system interface requirements for the design. The 8003 provides protocol functions like frame formatting, link access control and error control. The part is optimized for Direct Memory Access techniques for frame storage.

The 8023A MCC™ Manchester Code Converter performs the signal encoding and decoding in Manchester Code at 10 million bits per second. It also monitors the channel for "carrier" and "collisions" (two nodes transmit simultaneously). Low-power CMOS technology is used in the 8023A, which is in the 0.3 inch 20-pin package.

## Ethernet Node Configuration

A typical Ethernet node is shown in Figure 1. The System Interface on the left connects the host system bus to the network. This interface varies depending on processor and system requirements.

The station-resident hardware, consisting of the System Interface, the 8003 EDLC™ chip and the 8023A

MCC™ chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists of 78Ω balanced, shielded twisted-pair connections, DC biased at the station end and transformer-coupled at the Transceiver end.

Besides a passive tap to the Trunk Coax, the transceiver provides signal amplification, preconditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.

## Host-Dependent System Interface

There are three basic methods for interfacing the CSMA/CD channel to the system bus. The first one employs First-In, First-Out (FIFO) buffer memory to temporarily hold the transmit and receive frames. On the system-bus side of the FIFOs, data is transferred serially a byte at a time by the processor. The second method uses Direct Memory Access to transfer data directly between the Ethernet Data Link Controller and the system memory. In the third method, Direct Memory Access is also used, this time with a temporary buffer memory intervening between the system memory and the EDLC™ chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. (For more information on DMA-type interfaces, see SEEQ's Application Brief 6).

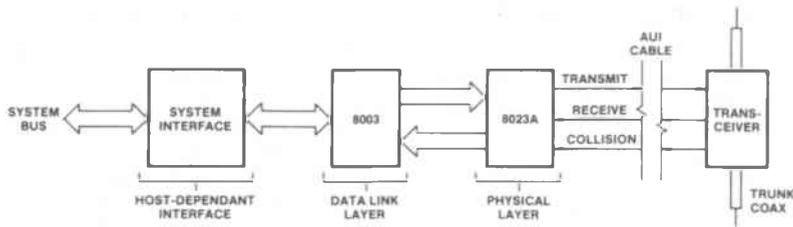


Figure 1. Ethernet Node Configuration

### IEEE 802.3 CSMA/CD Standard Protocol for Local Area Networks (Alias Ethernet)

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corporation. Since then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be reliable and efficient in a wide variety of network applications. As a result, it has become the first industry-standard protocol for local area networks, supported internationally by computer manufacturers in the U.S. and Europe.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry standard. After three years of review and refinement, this specification is about to be published by IEEE Press under the title *IEEE 802.3 CSMA/CD Local Area Network Standard Protocol*, ("CSMA/CD" describes the medium access method, **Carrier Sense**, **Multiple Access** with **Collision Detection**). The IEEE 802.3 document supersedes all previously published Ethernet specifications.

#### CSMA/CD — Carrier Sense, Multiple Access with Collision Detection

**CSMA/CD:** This expression describes the medium access method used in Ethernet alias IEEE 802.3 CSMA/CD. **Carrier Sense** means all

nodes on the network can detect all signals transmitted on the network from any source.

**Multiple Access** means all nodes can have equal access to the network without need for centralized control. A node is permitted to transmit if the network is not already busy. If, however, two or more nodes start to transmit simultaneously, it is called a collision. **Collision Detection** means that all nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes resolve which will retransmit first by differential backoff timing.

Data is transmitted in "packets" or "frames" which begin with a preamble for synchronization and end with a CRC field for error detection. In between, the frame has source and destination addresses, a byte-count field and an information field. Total frame length is 72 to 1526 bytes.

The physical signaling format used in Ethernet is baseband Manchester Code transmitted at a rate of 10 million bits per second. In Manchester Code, each bit is encoded by a transition. A "one" is encoded as a low-to-high transition and a "zero" as a high-to-low. In this way there is a continuous supply of bit-framing information for the receiver, since the transmitted signal is never stationary for more than one bit time.

## Interface Techniques for 16-Bit Busses

Ethernet is a byte-oriented protocol. That is to say, the smallest unit of data which can be transmitted is a byte. Hence, the 8003 EDLC™ chip has byte-wide data bus. Whether the System Interface is the FIFO-buffer type or the DMA type, the data transfers to and from the 8003 are byte-wide. This application brief describes some techniques for interfacing this byte-wide communication channel to a 16-bit wide bus.

In designing an Ethernet node, trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance may be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you strike the right balance for your design, several interface techniques will be given in the following sections. They are covered in order of increasing cost/complexity/performance.

In an 8-bit system, the 8003 can be interfaced directly to the data bus as shown in Figure 2. The RxTxD0-7 bus is the bus for transferring frame data. It connects to the internal 16-byte transmit and receive FIFOs. The CdSt0-7 bus is a separate input/output port for control and status. It interfaces to the system bus so that the processor has direct access to all command and status bits. In a 16-bit system, CdSt0-7 would connect either to the upper or lower data byte.

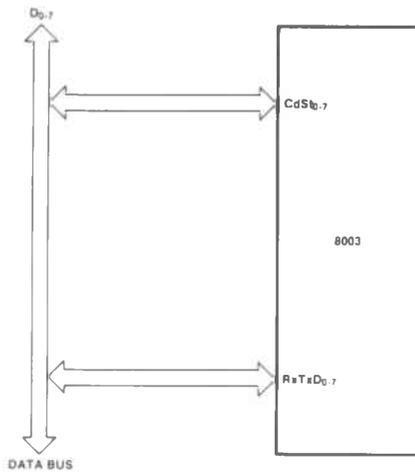


Figure 2. 8-Bit DMA Data Interface

## Split-Word 16-Bit Data Interface

Refer to Figure 3 for a circuit diagram of this technique. The split-word method splits the 16-bit word into two halves, using one half for transmit data and the other for receive data. In Figure 3, the upper byte of the system data bus is used for the transmit memory buffer and the lower half for receive. Two 74LS244 tristate buffers isolate the system bus lines from the RxTxD0-7 bus of the 8003. The upper 74LS244 is enabled by TxACK from the DMA Controller. TxACK is the DMA Acknowledge signal for the transmit channel. When enabled, this buffer transfers a byte of data from the upper byte of system memory to the 8003's Transmit FIFO. Similarly, the lower 74LS244 transfers data from the 8003's Receive FIFO to the lower byte of system memory. Configured in this way, the transmit and receive buffers in system memory can occupy the same word-address space.

## Full-Word 16-Bit Interface Using Byte-Wide Memory Transfers

Another type of 16-bit interface is one that assembles and disassembles words by transferring the upper byte and the lower byte separately. For example, suppose the convention is chosen that the upper byte is to be the first of the two bytes to be transmitted and the lower byte the second. Then the first byte of a frame and all odd-numbered bytes are always transferred to/from the upper byte of memory, and the second and all even-numbered bytes to/from the lower.

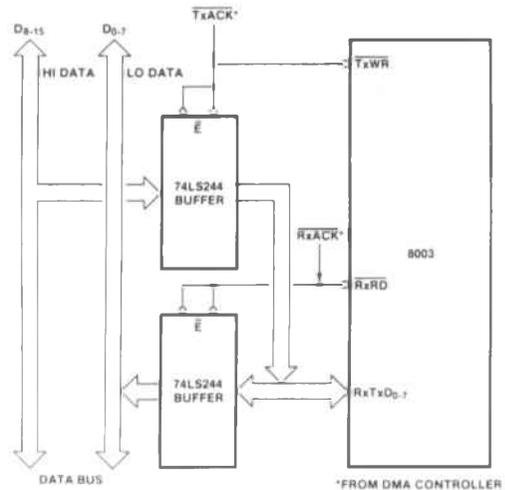


Figure 3. Split-Word 16-Bit DMA Data Interface

The data interface for this approach is a variation of the one shown in Figure 3. Two tristate buffers are replaced by two bi-directional transceivers. A0, the least-significant bit of the DMA Controller's address is decoded with  $\overline{\text{TxAck}}$  and  $\overline{\text{RxAck}}$  to enable the transceivers. The more significant address bits from the DMA Controller, A1 through A<sub>N</sub>, are used as the memory address. Upper and lower memory strobes are also controlled by A0. Refer to Table 1 for the truth table.

This is the simpler and more economical of two "Full-Word" data interfaces described in this application brief. The other one, shown in Figure 5, assembles and disassembles words in registers, and transfers 16 bits at a time. The advantage of the latter approach is in saving bus bandwidth, since it uses half as many bus cycles to transfer the same amount of data; but there is some additional cost in hardware.

**Table 1. A0 Address Decoding for Full-Word 16-Bit Interface Using Byte-wide Memory Transfers**

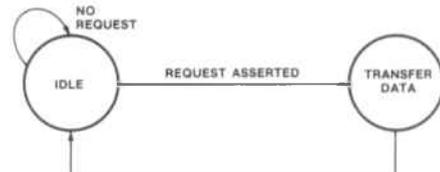
DMA Controller Outputs			Transceiver Enabled Toward (Memory; I/O)		Memory Activity	
A0	$\overline{\text{TxAck}}$	$\overline{\text{RxAck}}$	Upper	Lower	Upper	Lower
—	1	1	—	—	—	—
0	0	1	I/O	—	Read	—
1	0	1	—	I/O	—	Read
0	1	0	Memory	—	Write	—
1	1	0	—	Memory	—	Write

**Note:** — indicates not active.

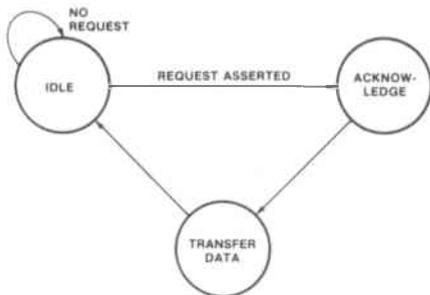
**a. No Request, No Wait**



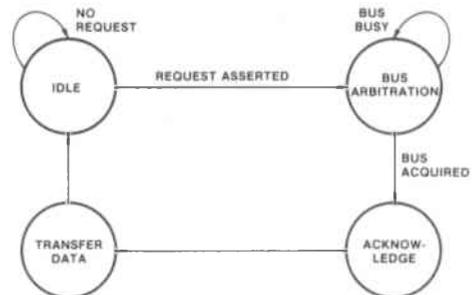
**b. With Request**



**c. With Request and Acknowledge**



**d. With Request, Acknowledge and Bus Arbitration**



**Figure 4. Data Transfer State Diagrams — Four Types**

Four types of data transfers are shown in Figure 4. The first, labeled a, is an unconditional transfer sequence such as the type that would be used to refresh a CRT screen. This type has no use in an Ethernet interface since it is not controlled by availability of storage space or stored data.

The diagram in Figure 4 Part b, illustrates a transfer which is initiated "on demand". The transfer takes place only when a "request" is given. An example of this type is data moved by a processor on its own synchronous bus. Physically the request is generated by the processor, manifesting itself as a set of bus-controls, and an address.

Part c illustrates a transfer that is requested by one entity and acknowledged by another. The acknowledge signal is used to notify the requesting entity that the transfer is about to take place. This implementation provides the requesting entity verification that the transfer is taking place. The diagram represents the response of the acknowledging party to the request. The requesting party normally waits for the acknowledgement to occur. This allows the acknowledging party to delay, if necessary, for data access. This mechanism is used on asynchronous busses, like that of the 68000 microprocessor.

The diagram in Part d is that of a transfer with request, acknowledge, and bus arbitration. This implementation is one that is used to transfer information using a DMA controller on the main system bus. There are actually two request/acknowledgement sequences in this transfer, one for bus acquisition and one to transfer information on the acquired bus. Initially a request generated by one of the two "transferees" queues the DMA controller to exit its idle state, and arbitrate for the system bus by generating a "bus request" signal. When the bus master relinquishes the bus, a "bus grant" acknowledgement is received, notifying the DMA controller that it now owns the bus. The DMA controller then performs the transfer, or transfers, by generating a "DMA Acknowledge" to the original requesting device, and generating the appropriate addresses and read/write control signals. Finally the sequence is terminated with control of the bus returning to the main processor through another arbitration.

Diagrams like these can be used to design state machine programs for interfaces like the one in Figure 5, which employs a single-chip state machine.

### Helpful Hints for State Machine Designers

As with writing a program, it is desirable to start with a "flow chart" or "state diagram". Examples of state diagrams can be seen in Figure 4. The following are the definitions used in the circle-and-arrow state diagrams used here.

1. Each circle represents a single physical machine state or an unconditional sequence of machine states such that there are no "hidden branches" omitted from the diagram.
2. All conditional branches, and wait states (which may be viewed as conditional branches) are indicated explicitly by arrows. Each arrow is labeled with the condition which determines the branch.

Following these or similar guidelines will help to avoid unforeseen anomalies in the operating flow.

Care should be taken in defining the programs for state machines when inputs are asynchronous with respect to the state-register clock. Problems can result when making a conditional branch based on an asynchronous input. Such problems can cause intermittent branching failures with possibilities of perverse consequences. Intermittency makes this type of problem hard to diagnose, so it pays off to avoid them by following these design rules:

1. When a branch is conditional on an asynchronous input bit, assign next-state addresses such that only one state-register flip-flop is affected by the asynchronous bit.
2. For a 3 or more-way conditional branch based on more than one independent asynchronous bit, break it down into independent 2-way branches which conform to rule 1.
3. For inputs which are mutually-dependent combinations of 2 or more bits, it is best to synchronize them with an input register whose clock is synchronized to the state-register clock.

When you have finished the state diagram, you have defined the operating program design. The next step is to choose the hardware that can run your program most efficiently.

After choosing the hardware, you can translate the state diagram, verbatim into program code for the state machine.

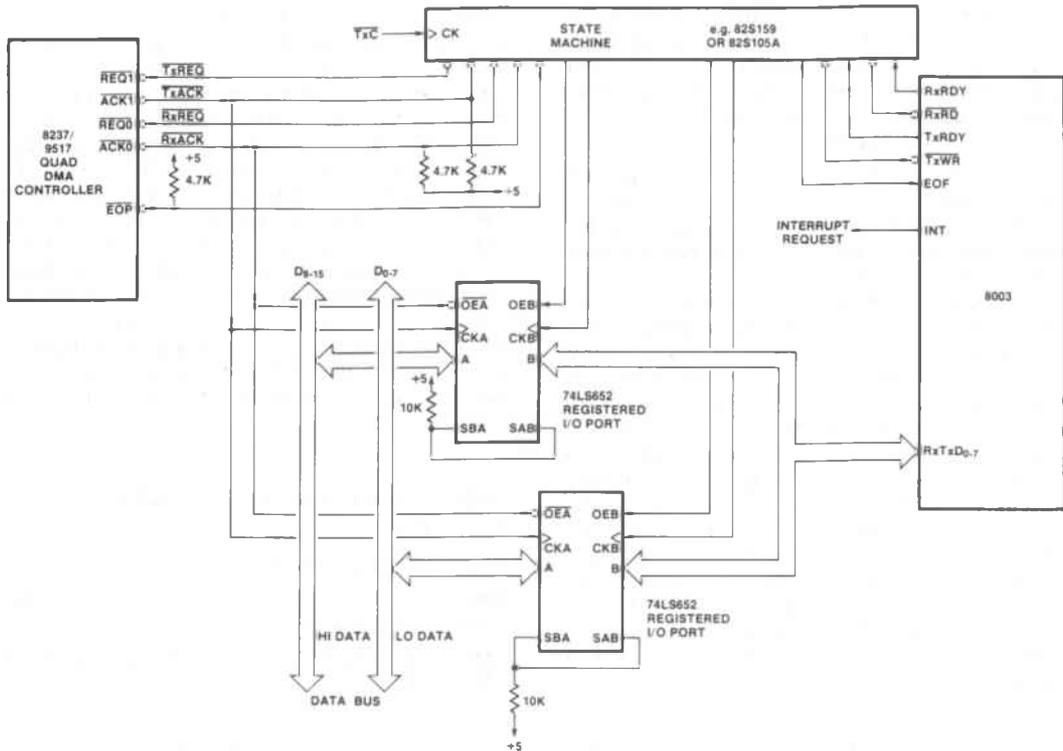


Figure 5. 16-Bit Full-Word DMA Data Interface with 8237/9517 Using Registered I/O Ports

### Full-Word 16-Bit Interface Using Registered I/O Ports

This data interface method assembles/disassembles 16-bit words in a pair of 8-bit registered I/O ports. The data transfers between the memory and the I/O ports are 16 bits wide. Transfers between the ports and the 8003 EDLC™ chip are byte-wide.

Registered I/O ports are configured by taking two 8-bit D-type registers with tri-state outputs and connecting them front-to-back. The result is two 8-bit bus connections, each connected to the D inputs of one register and the tri-state outputs of the other. The port has two register clocks and two output-enable controls. An example of such a chip is the 74LS652. The more popular 8-bit registered I/O port chips on the market are in the 0.3 inch 24-pin package.

This interface technique can be used with some variation for any of the three basic types of system interface, i.e. 1. with FIFO frame buffers, 2. with DMA to off-line frame buffers or 3. with DMA to system memory.

A state machine is used to sequence the assembly and disassembly processes. Programmable single-chip state machines and logic blocks, available from multiple sources, are excellent for this type of design. Most are field-programmable one time by burning fuseable links. Normally, the state machine portion of the design can be done in one or two chips.

A circuit example with the 8237/9517 DMA Controller appears in Figure 5. A single-chip state machine, such as the Signetics 82S159 or 82S105A, coordinates the timing for all other components. Two 74LS652s are the two registered I/O ports. The bus lines on the right side of the ports are commoned to make an 8-bit connection to the RxTxDo-7 pins of the 8003. On the left, the 16 port lines connect to the data bus.

Most of the command signals associated with data transfer are sequenced by the state machine. DMA requests (REQ0 and REQ1), port output-enable line

OEB, register clock CKB, Transmit FIFO write ( $\overline{\text{TxWR}}$ ) and Receive FIFO read ( $\overline{\text{RxRD}}$ ) are all under state machine control. Output-enable  $\overline{\text{OE}}$ A and register clock CKA are controlled by the DMA Acknowledge lines. All the status lines for data transfer connect to the state machine's inputs.

Figures 6 and 7 summarize the state-machine state diagrams for the application in Figure 5. Refer to Figure 6 for the word disassembly diagram. The disassembly process starts with a DMA request issued to the DMA's transmit channel. If the channel is not enabled, no acknowledge will be given and the state machine will remain in the DMA Request State. If the channel is enabled, the DMA Controller will request and acquire the system bus, then issue the DMA Acknowledge. A 16-bit word of data is then read from system memory into the two ports. The next state is Idle 1. Here the state machine waits for a TxRDY ready signal from the 8003 if not already present. When TxRDY is high, the machine goes to the Read First Byte State. This state moves the upper data byte from the upper port into the Transmit FIFO of the 8003. Another idle state occurs where TxRDY is checked for Transmit FIFO readiness. When ready, the lower data byte from the lower port is moved to the Transmit FIFO, ending the cycle.

Refer to Figure 7 for the word assembly state diagram. Word assembly starts in the Idle 1 State. Here, the state machine waits for a signal from the Receive FIFO (RxRDY pin) indicating data is present. When RxRDY is high, the machine advances to load the first byte of the word being assembled to the upper port. As the data is read out of the FIFO, the 8003's EOF line is tested to determine if it is the last byte of the frame. If it is, reading of the second byte is skipped. If not, the Idle 2 State is entered. When ready, the second byte will be loaded into the lower port. Then a DMA Request is given. The DMA Controller will then request the bus, acquire it and give the DMA Acknowledge. Then the state machine passes through the Transfer State, writing the 16-bit word to system memory. That ends the word assembly cycle.

#### Further References Available from SEEQ

8023A MCC™ Data Sheet

8003 EDLC™ Data Sheet

Application Note 3: Manchester Encoding and Decoding for Local Area Networks

Application Brief 6: DMA Interconnection to the 8003 EDLC™

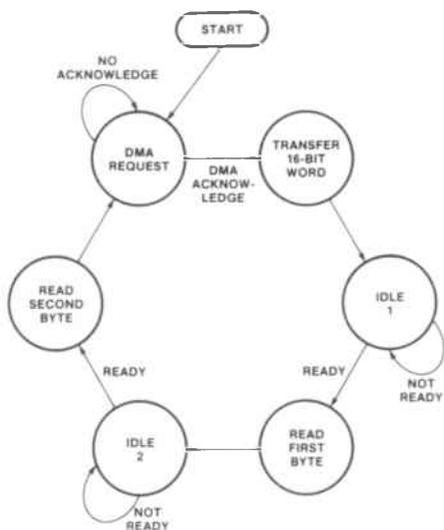


Figure 6. State Diagram for 16-Bit Word Disassembly

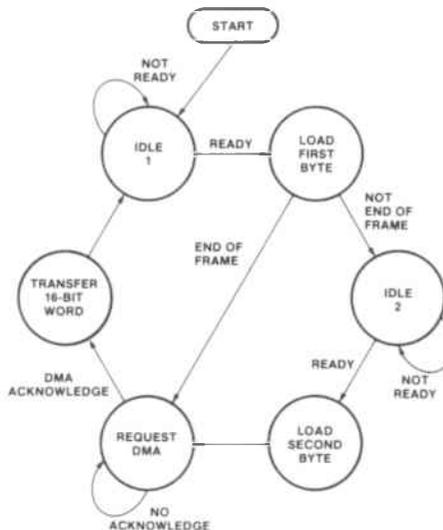
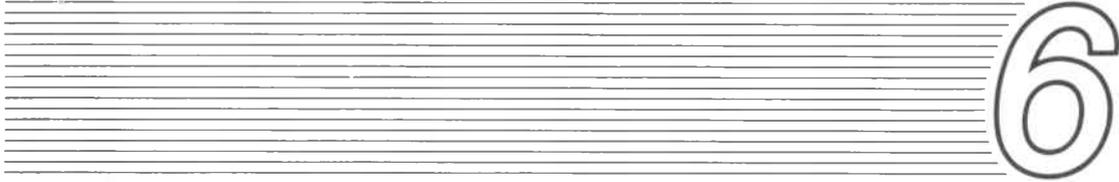


Figure 7. State Diagram for 16-Bit Word Assembly

**Communications Products  
Application Brief**



**6**

**DMA  
INTERCONNECTION  
TO THE  
8003 EDLC™**

*March 1985*

APP. NOTES

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**seeq**  
*Technology, Incorporated*

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# DMA Interconnection to the 8003 EDLC™

## Introduction

SEEQ's 8003 Ethernet-compatible data link controller provides an economical communication interface for terminals, personal computers, workstations, printers, disk drives and host computers. The 8003 is a 40-pin VLSI device which can replace approximately 60 MSI and SSI components in a typical Ethernet node configuration.

This application brief is about design techniques for an Ethernet node when direct-memory access (DMA) is chosen as the means of transferring data between the system bus and the channel. The methods described herein can be applied to virtually any computer or system bus architecture.

Ethernet local area networks use the **broadcast** network topology. That is to say, a signal transmitted by any station reaches all other nodes on the network. This is in contrast to other types of networks, such as the "star" and the "ring", which use point-to-point interconnections. Transmitted messages in Ethernet are "broadcast" on a segment of 50Ω coaxial cable. Communication nodes are attached to this cable via passive taps, so that new nodes can be added at any time without interrupting the network service. Nodes on the network can be addressed individually, in "multicast" groups, or by the "broadcast mode" to all nodes simultaneously. The broadcast topology is a very efficient mode of communication, yet it is simple and inexpensive to implement.

### Ethernet alias IEEE 802.3 CSMA/CD

The first Ethernet local area network was implemented in Palo Alto, California in 1975 as a joint effort of Stanford University and Xerox Corp. Since

then, Ethernet has been expanding in use and accumulating history. Over the years, it has proven to be reliable and efficient in a wide variety of network applications. As a result, it has become the first industry-standard protocol for local area networks, supported internationally by computer manufacturers in the U.S. and Europe.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document and publish this protocol as an international industry-standard. After three years of review and refinement, this specification is about to be published by IEEE Press under the title *IEEE 802.3 CSMA/CD Local Area Network Standard Protocol*. ("CSMA/CD" describes the medium access method, **Carrier Sense, Multiple Access with Collision Detection**.) The IEEE 802.3 document supersedes all previously published Ethernet specifications.

### CSMA/CD — Carrier Sense, Multiple Access with Collision Detection

**CSMA/CD:** This expression describes the medium access method used in Ethernet alias IEEE 802.3 CSMA/CD. **Carrier Sense** means all nodes on the network can detect all signals transmitted on the network from any source. **Multiple Access** means all nodes can have equal access to the network without need for centralized control. A node is permitted to transmit if the network is not already busy. If, however, two or more nodes start to transmit simultaneously, it is called a collision. **Collision Detection** means that all nodes can detect a collision by monitoring the medium. When a collision occurs, the

transmitting nodes resolve which will retransmit first by differential backoff timing.

Data is transmitted in "packets" or "frames" which begin with a preamble for synchronization and end with a CRC field for error detection. In between, the frame has source and destination addresses, a byte-count field and an information field. Total frame length is 72 to 1526 bytes.

The physical signaling format used in Ethernet is baseband Manchester Code transmitted at a rate of 10 million bits per second. In Manchester Code, each bit is encoded by a transition. A "one" is encoded as a low-to-high transition and a "zero" as a high-to-low. In this way there is a continuous supply of bit-framing information for the receiver, since the transmitted signal is never stationary for more than one bit time.

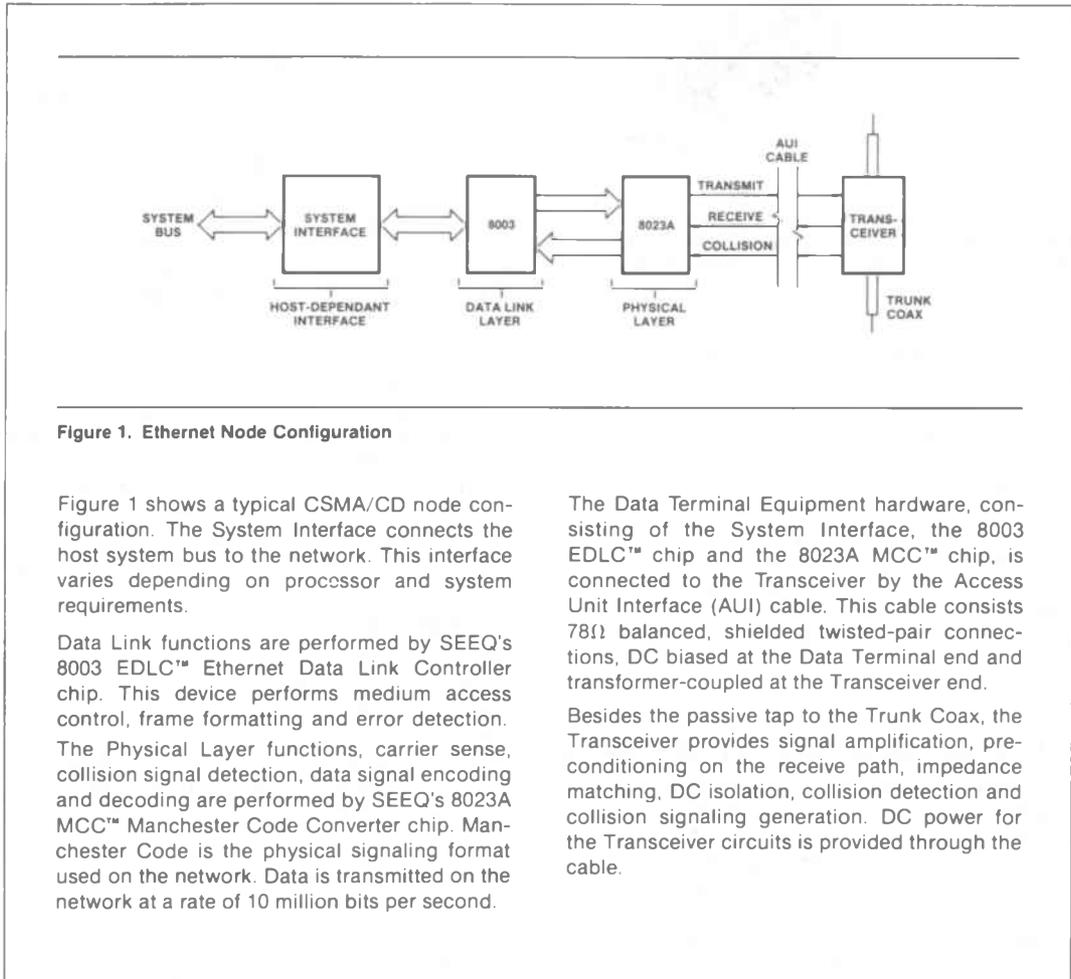


Figure 1. Ethernet Node Configuration

Figure 1 shows a typical CSMA/CD node configuration. The System Interface connects the host system bus to the network. This interface varies depending on processor and system requirements.

Data Link functions are performed by SEEQ's 8003 EDLC™ Ethernet Data Link Controller chip. This device performs medium access control, frame formatting and error detection. The Physical Layer functions, carrier sense, collision signal detection, data signal encoding and decoding are performed by SEEQ's 8023A MCC™ Manchester Code Converter chip. Manchester Code is the physical signaling format used on the network. Data is transmitted on the network at a rate of 10 million bits per second.

The Data Terminal Equipment hardware, consisting of the System Interface, the 8003 EDLC™ chip and the 8023A MCC™ chip, is connected to the Transceiver by the Access Unit Interface (AUI) cable. This cable consists of 78Ω balanced, shielded twisted-pair connections, DC biased at the Data Terminal end and transformer-coupled at the Transceiver end.

Besides the passive tap to the Trunk Coax, the Transceiver provides signal amplification, pre-conditioning on the receive path, impedance matching, DC isolation, collision detection and collision signaling generation. DC power for the Transceiver circuits is provided through the cable.



Figure 2. SEEQ's Ethernet Chip Family: 8003 EDLC™ Ethernet Data Link Controller, 8023A MCC™ Manchester Code Converter

### Direct Memory Access System Interface

There are two basic methods for interfacing the CSMA/CD channel to the system bus using DMA, illustrated in Figure 2. The first method uses DMA to transfer data directly between the Ethernet Data Link Controller and the system memory. In the second method, a temporary buffer memory intervenes between the system memory and the EDLC™ chip. The intervening buffer relieves the system bus of some of the traffic and timing requirements associated with the channel. These two methods will be the subject of the following sections.

### DMA Design Considerations for Ethernet

In designing an Ethernet node, some trade-offs have to be made between processing speed and communication speed, cost and performance, flexibility and simplicity, etc. The right balance can be different for each piece of equipment designed, depending on its purpose and system requirements. In order to help you evaluate the trade-offs for your design, this section discusses some of the key parameters for you to consider at the outset.

#### Time is Data

Since the data transmission rate for Ethernet is 10 million bits per second, data transfers during active

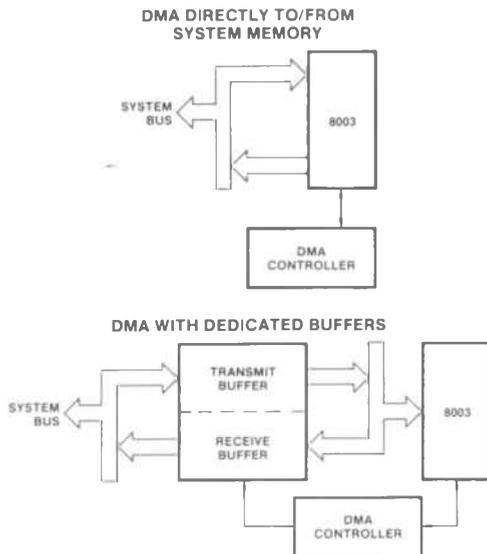


Figure 3. DMA System Interface Techniques

periods will have to keep up. That means data has to be moved at 1.25 million bytes per second to/from the communication channel. The DMA Controller must meet this speed requirement or frames will be lost. If the system is to support loopback diagnostics, both transmit and receive DMA channels will have to operate simultaneously, together transferring 2.5 million bytes per second. Not just any DMA Controller will do.

#### Bus Bandwidth

This is only a consideration for systems with heavy communications traffic and/or critical response timing. The transfer of data on the system bus can sometimes use up a considerable percentage of the bus time, at least for short bursts. If this is a problem, the method with dedicated buffer memory can be used to offload the system bus (see Figure 2 bottom).

#### With or Without Dedicated Buffer Memory

If the system architecture does not support 1.25M Bytes/s DMA, the dedicated buffer approach can solve the timing problem. If the system architecture does support high-speed DMA, then bus bandwidth is the key factor which influences this decision. In this case it is clearly a cost-performance issue. The dedicated buffer can relieve system bus traffic, but it takes more hardware to implement.

### Cycle-steal or Burst Mode DMA

Refer to Figures 3 and 4. In the Cycle-steal DMA Mode, the DMA Controller "steals" a bus cycle to transfer one and only one byte or word of data. In the Burst DMA Mode, each time the DMA Controller acquires the bus, it can transfer several bytes or all the data to fill or empty a buffer. Either of these two modes can work for Ethernet in principle if the transfer speed is adequate. The Burst Mode is usually preferred by reason of timing efficiency. In Burst Mode, bus arbitration and change-over delays are kept to a minimum. Also, Burst Mode allows the DMA Controller to fill or empty a buffer in one DMA cycle.

#### On Demand

Transfers between memory and the communication circuitry must be done *on demand*. Some DMA Controller chips will only transfer blocks of data in predetermined lengths. This will not work since the processor and DMA Controller cannot know in advance how many bytes of data can be transferred at a given time.

#### Maximum Bus Grant Latency

The time it takes to get the bus after a request is made is called bus grant latency. If the DMA method without buffer memory is used, each time a DMA transfer to/from the 8003 EDLC™ chip begins, the DMA Controller must arbitrate for and acquire the system bus. If the latency is too long, the transmitter may underflow or the receiver overflow. The 8003 has transmit and receive FIFOs which are 16 bytes deep, so it must transfer data at least once every 12.8 microseconds when active (16 x 800 nanoseconds). Maximum bus grant latency should be deterministic and always less than that required to prevent underflow and overflow.

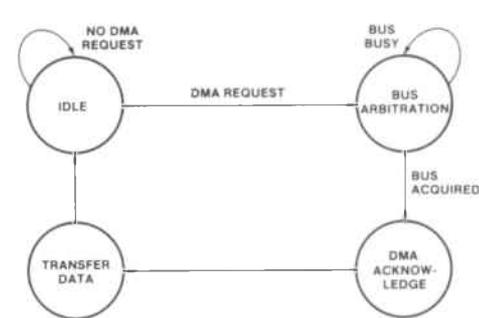


Figure 4. DMA Cycle-steal Mode State Diagram

### 8003/DMA Node Hardware

The 8003 has an 8-bit bi-directional data bus (RxTxD<sub>0-7</sub>) for data transfers to and from its internal FIFOs. In Figure 6, the node hardware is configured to transfer data directly to/from system memory over this bus. (This is the technique referred to previously in Figure 3 at the top.) A two-channel DMA Controller is used, providing one channel for transmit data and one for receive data.

A transfer to the transmitter of the 8003 begins with a DMA Request given by the 8003 (its TxRDY pin goes high). The DMA Controller then issues a Bus Request to the processor. After completing the current cycle, the processor halts and gives a bus grant to the DMA Controller, which then transfers the data by issuing a DMA Acknowledge and all necessary address and control signals. Additional transfers would take place if Burst Mode is used until the Transmit FIFO is full, indicated by the TxRDY pin going low. Then the bus is released to the processor and the DMA cycle is over.

Data transfer from the Receive FIFO happens in the same way but with data flowing in the opposite direction. It starts with a DMA Request from the 8003 (its RxRDY pin goes high). If Burst Mode is used, the DMA will continue to transfer until the Receive FIFO is empty, indicated by a low on the RxRDY pin.

The Data Interface for a DMA node with buffer memory appears in Figure 6. In this case, a 4-channel DMA Controller is used. Two channels are needed as before to transfer data between the 8003 and memory. These two channels operate "off-line" and do not require bus arbitration. The other two transfer data between the buffer memory and the system bus. They do require the usual bus arbitration.

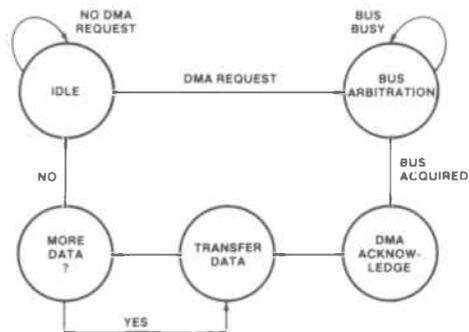


Figure 5. DMA Burst Mode State Diagram

For this design, the RxTxD<sub>0-7</sub> Receive/Transmit Data Bus of the 8003 connects to a separate bus which is isolated from the system bus by a transceiver. This bus gives the 8003 immediate access to the buffer memory without the need for arbitration.

The two channels for memory-to-memory transfer use the usual bus arbitration method to access the system bus. For these two channels, data being

transferred passes through the transceiver shown in the top center of the figure. The tri-state buffer appearing at the bottom center passes the address from the DMA Controller to the System Memory during the transfer. The tri-state buffer and transceiver are enabled by the DMA Controller at the appropriate time in its cycle.

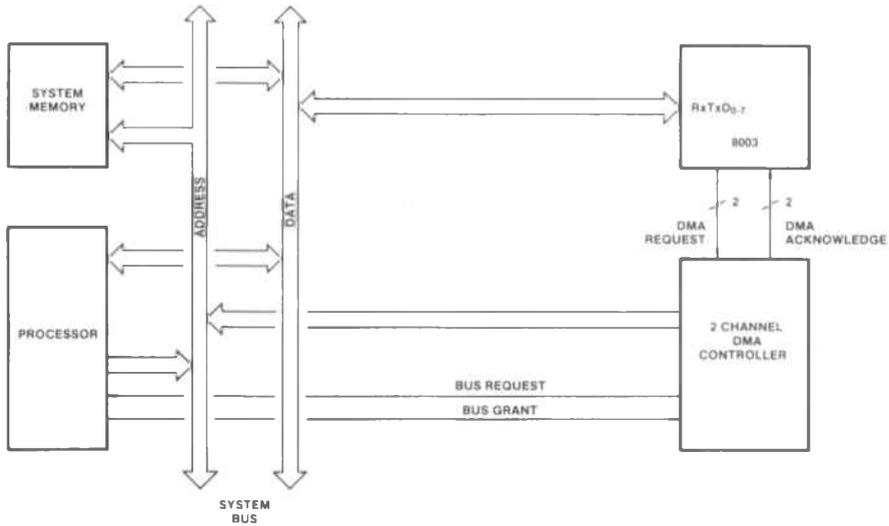


Figure 6. Data Interface for DMA Directly to/from System Memory

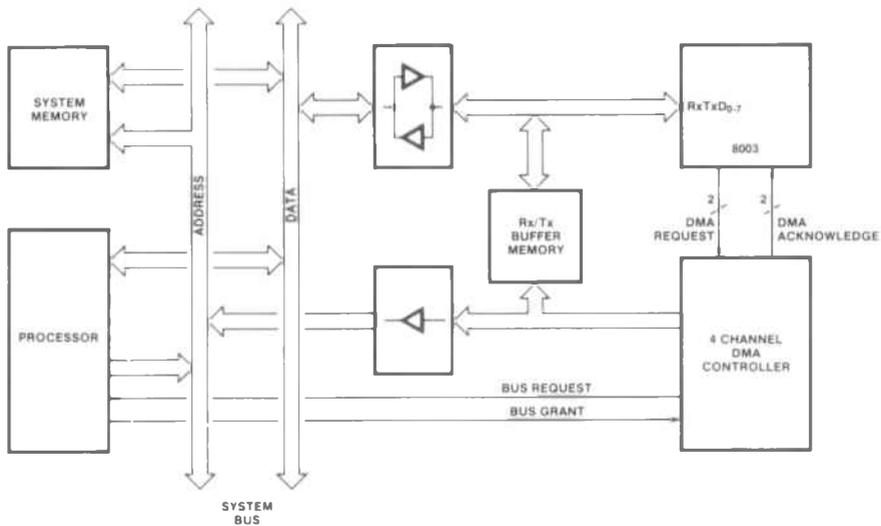


Figure 7. Data Interface for DMA with Buffer Memory

## Command Status Interface

The Command/Status Interface for the 8003 is shown in Figure 8. The 8003 has a separate bi-directional 8-bit bus for accessing its internal command and status registers. This bus is labeled "CdSt0-7" in the figure. Three address lines, A<sub>0</sub>, A<sub>1</sub> and A<sub>2</sub> select the register to be accessed. Refer to the 8003 data sheet for a full description of these registers and their addresses.

To write to a command register, the system bus decoder must provide a low level to both Chip Select ( $\overline{CS}$ ) and Write ( $\overline{WR}$ ) while data and the three address bits are valid. To read a status register, a low is applied to both Chip Select and Read ( $\overline{RD}$ ) while the address is valid.

The Interrupt Request line ( $\overline{INT}$ ) goes high to request an interrupt when specific conditions occur. This line drives the interrupt input of the processor, either directly or through an interrupt-priority logic block. Conditions for generating an interrupt are selected by setting bits in the command registers. For details, see the data sheet. The Interrupt Request line is cleared automatically when the processor reads the status registers.

## 8237/9517 DMA Controller Interface

The interconnection of popular the 8237/9517 DMA Controller to the 8003 is illustrated in Figure 9. The TxRDY control line from the 8003, which indicates that the Transmit FIFO is not full, is used to generate the DMA request for Channel 1, the transmit channel. Similarly, RxRDY which indicates that the Receive FIFO is not empty generates a request for Channel 0, the receive channel. After a request for

Channel 1, the DMA Controller will issue simultaneously a DMA acknowledge (on DACK1) and an input/output write ( $\overline{IOW}$ ), which are used to assert the TxWR write line on the 8003. After a request for Channel 0, the DMA Controller will issue simultaneously a DMA acknowledge on DACK0 and an input/output read ( $\overline{IOR}$ ). These are used to assert the RxRD read line on the 8003.

The  $\overline{EOP}$  control line on the 8237/9517 indicates the "end of process" which has the same meaning as the 8003's "end of frame" line (EOF). These lines are used to terminate the transfer process after the last byte of a frame has been transferred. Both the  $\overline{EOP}$  and EOF lines are bi-directional, the direction depending on the direction of data transfer. They are interfaced together by an inverting transceiver, whose direction of operation is controlled by the DACK0 and DACK1 acknowledge lines.

The active polarities of the DREQ and DACK lines on the 8237/9517 are programmable by setting internal control bits. For the interface shown, they should be programmed active high.

## 68440/68450 DMA Controller Interface

The 8003 interface to the 68440/68450 DMA Controllers from the popular 68000 microcomputer family is shown in Figure 9. The request lines on the 68440/68450 can be programmed to be level or edge sensitive. In this example, level sensitivity is selected by setting internal control bits. As in the previous example of Figure 9, the TxRDY output of the 8003 drives the request line for Channel 1 and the RxRDY requests Channel 0.

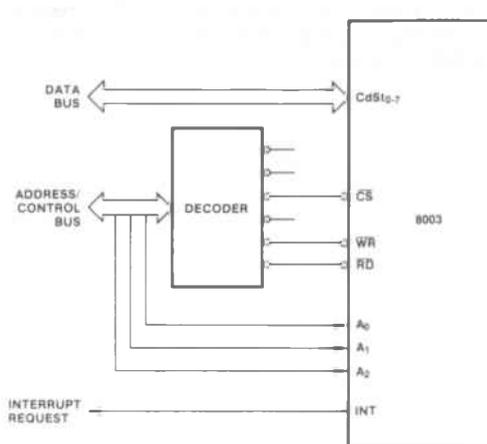


Figure 8. Control/Status Interface

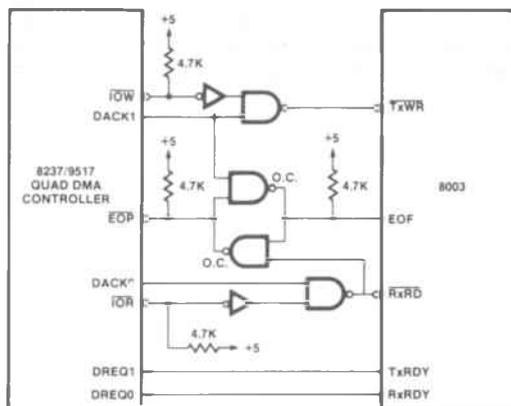


Figure 9. 8003 Interface to 8237/9517 DMA Controller

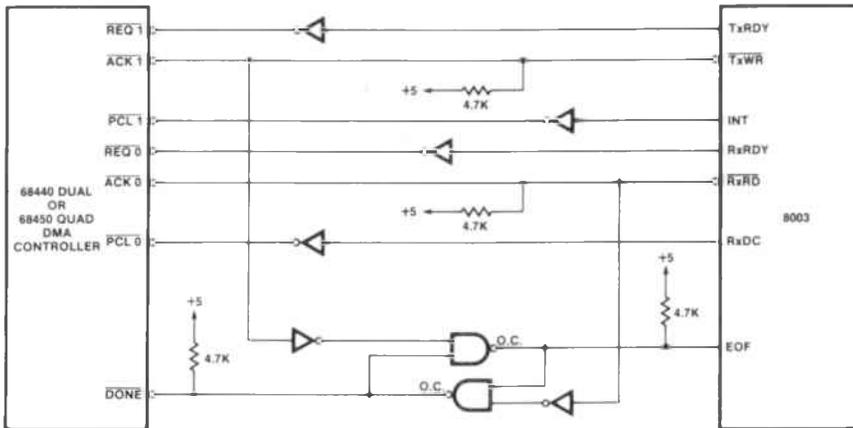


Figure 10. 8003 Interface to 68440/68450 DMA Controller

The acknowledge lines on the 68440/68450 can be connected directly to the TxWR and RxRD inputs of the 8003 as shown in Figure 9.

On the 68440/68450, the EOF function pin is called "done". The DONE pin interfaces to the 8003's EOF pin through an inverting bi-directional transceiver shown at bottom center of the drawing. As in the previous example, this signal terminates the channel activity at the end of the frame.

The  $\overline{PCL0}$  and  $\overline{PCL1}$  lines on the DMA Controller are put to good use in this application. They are programmable inputs associated with Channel 0 and Channel 1 respectively. By setting internal control bits, the  $\overline{PCL1}$  line can be programmed to activate the on-chip interrupt request logic. The interrupt request output of the 8003 (INT) is used to drive it. A low on PCL1 will interrupt the processor to read the

status registers of the 8003. This is used for a variety of conditions which can occur on the network. For example, if 16 consecutive collisions occur, network diagnostics and/or an alarm are ordered by interrupting the processor. The status code which has generated the interrupt is read by the processor from the 8003's internal status registers.

The  $\overline{PCL0}$  input can be programmed to be an input for restarting Channel 0, the receive channel. In this mode, a low on  $\overline{PCL0}$  will re-initialize the channel automatically. It is driven by the 8003's RxDC receive discard line. RxDC goes high following reception of a bad frame or frame fragment. This will in effect discard the bad data and restart the receive channel, without the need for processor intervention in setting up the channel.

**Communication Products  
Application Note**



**8005  
ADVANCED EDLC™  
USER'S GUIDE**

*September 1987*

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**seeq**

*Technology, Incorporated*

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# Advanced EDLC™ User's Guide

## Introduction

Ethernet was developed by the Palo Alto Research Center (PARC) of the Xerox Corporation. The first network was implemented in 1975, as a result of a joint effort by Stanford University and PARC. Over the years, it was proven to be reliable and efficient in a wide variety of network applications. As a result of that success, it became the first industry standard protocol for LANs, supported internationally by computer manufacturers in the United States and Europe.

The network allows equal access by all nodes, can support upwards of 1000 nodes, and can operate with a coaxial cable length in excess of 500 meters. Ethernet is easy to realize, due in large part to currently available LSI chips which implement it.

In 1980 the Institute of Electrical and Electronics Engineers (IEEE) sponsored a committee to review, document, and publish this protocol as an international industry standard. After three years of review and refinement, this specification has been published by the IEEE press under the title, "ANSI/IEEE 802.3-1985 CSMA/CD Local Area Network Standard Protocol". The medium access method is described by the abbreviation CSMA/CD, or Carrier Sense, Multiple Access with Collision Detection.

### **CSMA/CD: Carrier Sense, Multiple Access with Collision Detection**

#### **Carrier Sense**

All nodes on the network can detect all signals transmitted from any source. A node is any connection to the coaxial cable via transceiver, shown in Figure 1.

The transceiver makes a connection to the cable via connectors or has barbs to pierce the cable and establish an electrical connection when a screw or bolt is tightened. The transceiver provides collision detection, electrical isolation and voltage level translation between the system at the node and the cable carrying data.

#### **Multiple Access**

All nodes have equal access to the network. There is no priority assigned to any node. Also, there is no central control, nor is there any token passing. Any given node may transmit if the network is not already busy. If two or more nodes transmit at the same time, a collision occurs.

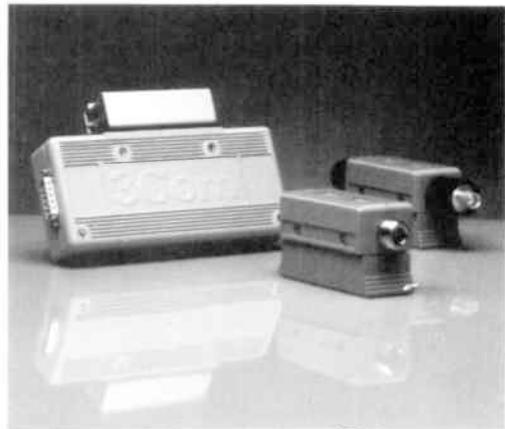


Figure 1.

## Collision Detection

All nodes can detect a collision by monitoring the medium. When a collision occurs, the transmitting nodes jointly decide which node will retransmit first by a technique known as truncated binary exponential backoff, which provides for a random timeout at each node before each retransmit attempt.

## Ethernet Data Format

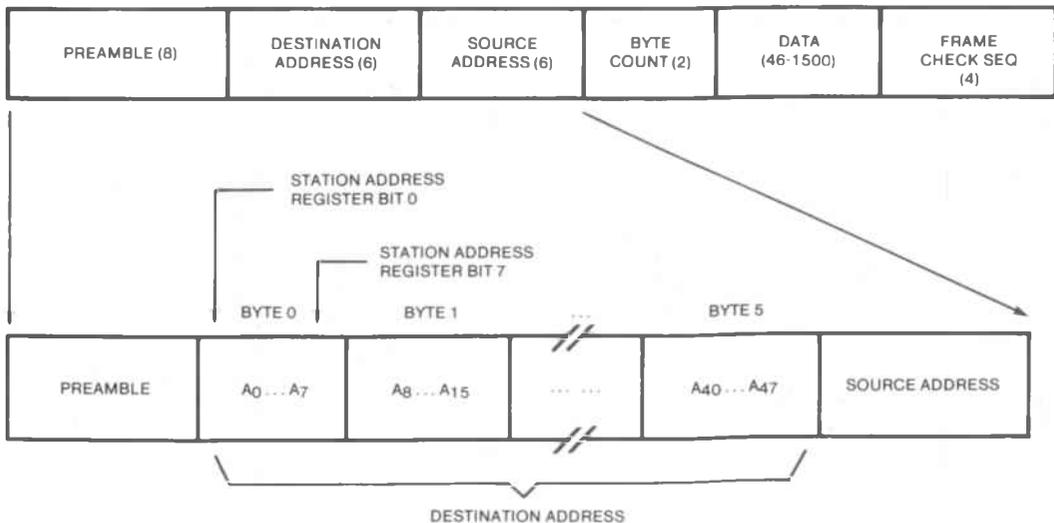
Data is formatted and transmitted in "packets" or "frames", as shown in Figure 2. These frames begin with a preamble for synchronization, and end with a CRC field for error detection. In between, the frame has destination and source addresses, a byte count field, and a data field. This data field contains from 46 to 1500 bytes of information which is passed to a higher layer of software for processing. It is transparent to the media access layer of Ethernet, and may contain any arbitrary sequence of bytes.

Total frame length is 72 to 1526 bytes, including preamble (8 bytes), and frame check sequence (4 bytes).

The signaling method used in Ethernet is base-band Manchester code, transmitted at 10 Megabits per second. Manchester code is such that each bit is defined by a transition at its mid-bit point: a ONE is encoded as a high going signal and a ZERO is a low going signal. Thus, the data is said to be self clocked. This technique provides a continuous supply of bit framing information for the receiver, since the transmitted signal is never static for more than one bit time.

## Addressing Scheme

An Ethernet address contains six bytes to define a station address. This allows for over 140 trillion unique addresses. The 48th bit in the address is reserved to indicate a broadcast or multicast address. Xerox Corporation controls issuing addresses for Ethernet. As a system manufacturer, you receive your block of addresses when you receive a license. It is necessary to assign a unique address for each product that communicates on Ethernet.



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Figure 2. Ethernet frame format. Numbers in parentheses indicate the length of each field. Bits within a byte are transmitted and received LSB first and MSB last.

## Direct Memory Access System Interface

There are two basic DMA techniques for interfacing the network to the system bus. The first, in Figure 3a, uses DMA to transfer data directly between the Ethernet controller and the system memory. In Figure 3b, a temporary buffer memory intervenes between the system memory and the controller chip. This buffer eliminates the need to service LAN traffic in real-time.

### Why a Local Buffer?

Consider the first approach, where no local buffer is used at the node. Since the LAN data rate is 10 Megabits per second, the DMA controller must be capable of handling system data at a minimum of 1.25 Megabytes per second. If the controller cannot operate at this rate continuously, LAN data will be lost. Additionally, if the system is to support loopback diagnostics, both transmit and receive must operate simultaneously, together transferring 2.5 Megabytes per second. Clearly, a garden variety DMA controller will not get the job done. Particular attention must be paid to how long it takes the controller to acquire the system bus. If too long, Ethernet data will be lost.

### Collision Effects

Collisions normally occur during transmission of the first 64 bytes of data. If packets are retrieved via DMA from system memory, when a collision

occurs these 64 bytes must be retransmitted. This is an inefficient use of bus bandwidth.

### An Ethernet Controller is a True Asynchronous Peripheral

Prudent system design calls for buffering any peripherals which are asynchronous in nature. Buffering makes the resource much more manageable at the system level.

### Implementing a Local Buffer

Most currently available Ethernet controllers have a modest buffer built in, usually on the order of 16 bytes. This is sometimes adequate to handle system bus acquisition delay, but it does not make efficient use of bus bandwidth in three important areas:

1. Collisions during transmit. As network traffic increases, the probability of a collision increases. Each time a collision occurs the Ethernet controller must retransmit from the beginning of the packet. The time spent retransmitting due to collision uses bus bandwidth unnecessarily.
2. Frame check sequence (CRC) errors after receive. Since errors are not detected until after a packet has been received, bus bandwidth will be wasted when receiving packets with errors.

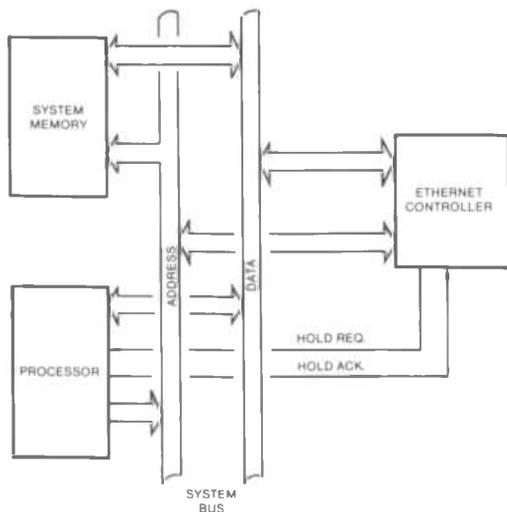


Figure 3a.

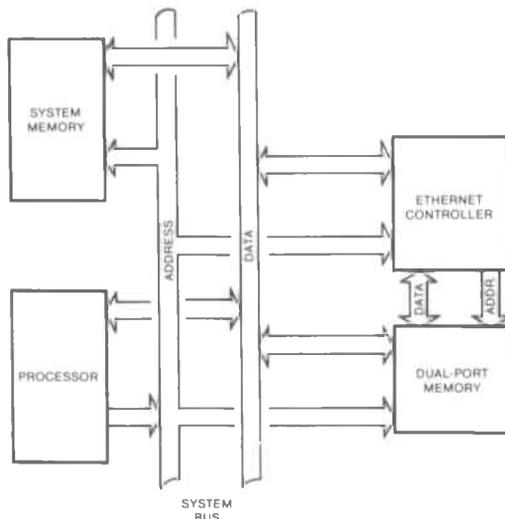


Figure 3b.

3. A significant number of receive packets are minimum size (64 bytes) yet contain much less than 64 bytes of information. For example, packet acknowledgments contain less than 20 bytes of information and are padded to the 64 byte minimum required. Transfer of these pad bytes over the system bus cannot be avoided without some large local buffer.

### Supplementing the Controller Buffer

RAM can be added to the Ethernet board to add to the modest buffer already on the controller chip. Figures 4a and 4b show two possible ways.

The buffer should be at least 1514 bytes long. Static RAMs were chosen in Figure 4a to avoid having to include refresh control circuits in the dual port memory control logic.

The memory control must regulate access to the buffer by two buses: the system bus, and the data bus from the controller. The SRAMs are costly.

If DRAMs are used as in Figure 4b the cost is lower but they do require refresh circuitry in the memory controller.

### Local Buffering with the 8005

The 8005 Advanced Ethernet Data Link Controller combines several unique approaches to the problem of implementing an Ethernet connection. Look at the design in Figure 5.

First consider the local buffer: the 8005 is designed to work with 64K x 4 DRAMs which are readily available, and inexpensive. It has on board refresh circuitry, and just two DRAM chips provide 64 Kbytes of local buffer storage.

The 8005 treats the DRAM in a unique fashion: it multiplexes both address and data over eight lines. This saves on circuit board traces: only 12 lines are required to interface with the DRAMs, compared with 26 lines if static RAMs are used.

The 8005 also directly supports an address (EE) PROM, which allows for storage of the 8005's Ethernet address and configuration data.

The 8005 supports six unique station addresses. Thus, one physical connection on the Ethernet suffices for six logical connections. You could make effective use of this feature by, for example, connecting six devices to one Ethernet node, and controlling access to each device.

Figure 6 illustrates a cluster controller which services three printers and three PCs or terminals, and provides access to the Ethernet for the devices.

The printer controller services the cluster of three printers, and a low cost, low speed LAN provides coverage for the PCs. This LAN coverage may represent a relatively small geographic area, like a single corporate department. Note, however, that each device has access to the Ethernet, and each has a specific Ethernet address.

### Design Examples

In this section, we'll briefly examine the way in which the 8005 can put two popular micro-processor bus formats on Ethernet, by way of using the Intel and the Motorola bus modes built into the 8005. Then we'll look in detail at a intelligent Ethernet controller which could realistically reside on a PC board, and usurp a minimal amount of resources from the system in which it is installed.

#### The Intel Mode

Figure 7 shows an implementation of the 8005 in an environment using an Intel processor. Note that BUSMODE is pulled up, indicating that the 8005 will produce Intel-compatible output signals, and accept inputs from an Intel bus. Also, in this example, we have selected a 16 bit bus, since BUSSIZE is high.

#### The Motorola Mode

In Figure 8, the 8005 is configured for use with Motorola processors, and the interface fits that processor family. BUSMODE is a ZERO, and we have specified a 16 bit bus, as before with the Intel mode.

### A Board Level Ethernet Controller

Figure 9 illustrates a design using the Intel 80186 as a co-processor with the 8005, on the same PC board, to implement Ethernet. The 80186 is a particularly good choice for this application, because it has an on-chip DMA controller.

The 80186 has multiplexed address and data lines, here shown being demultiplexed by the latch. The data bus is buffered by the 74LS245s, but these may not be required, depending on the fanout required by the specific application.

The important signals between the two chips are the following; refer also to Intel 80186 and SEEQ 8005 data sheets.

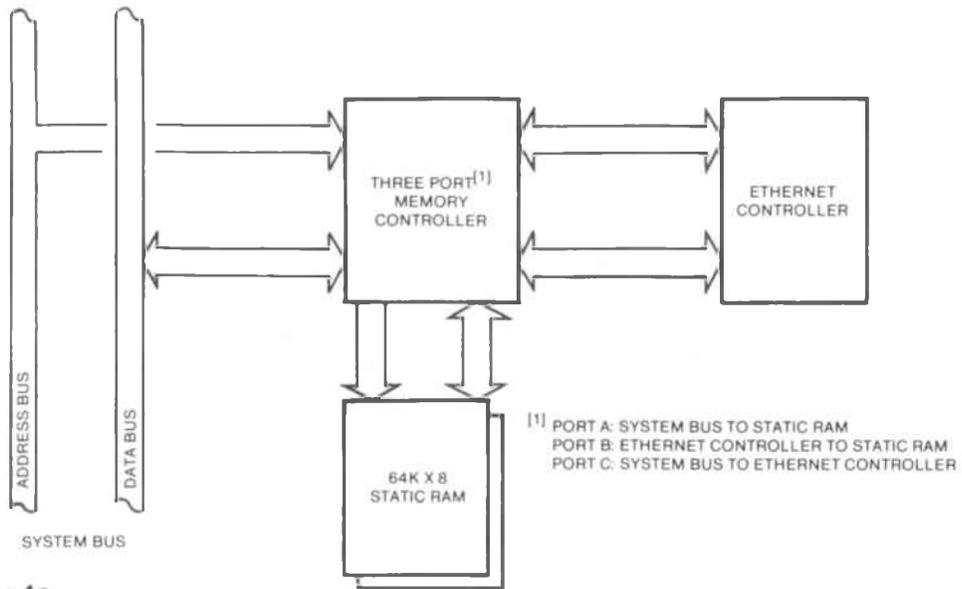


Figure 4a.

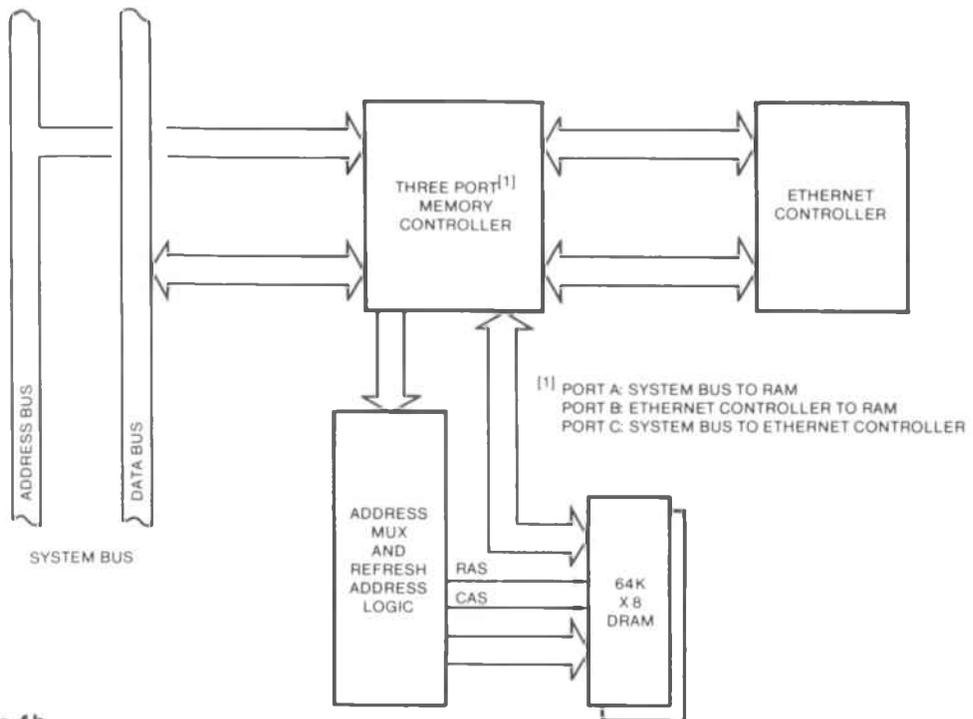
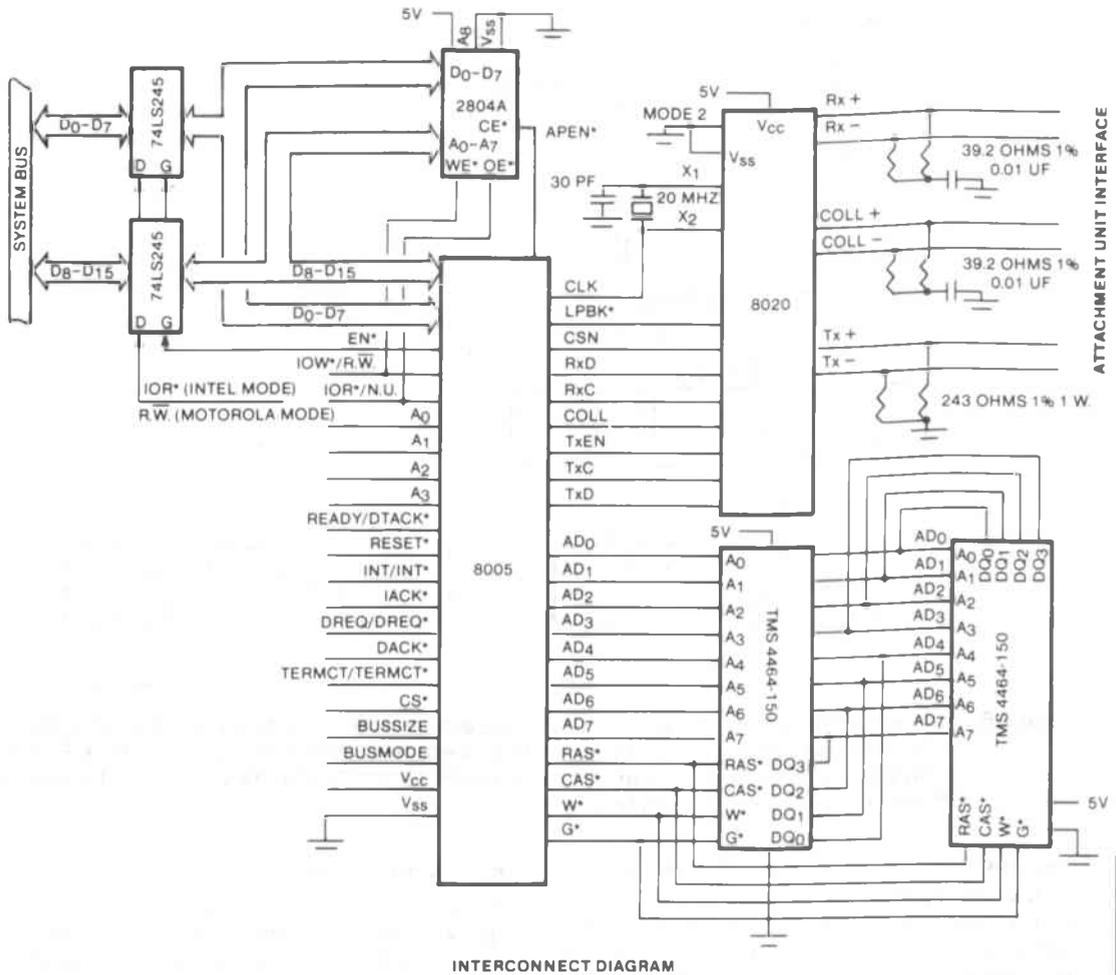


Figure 4b.

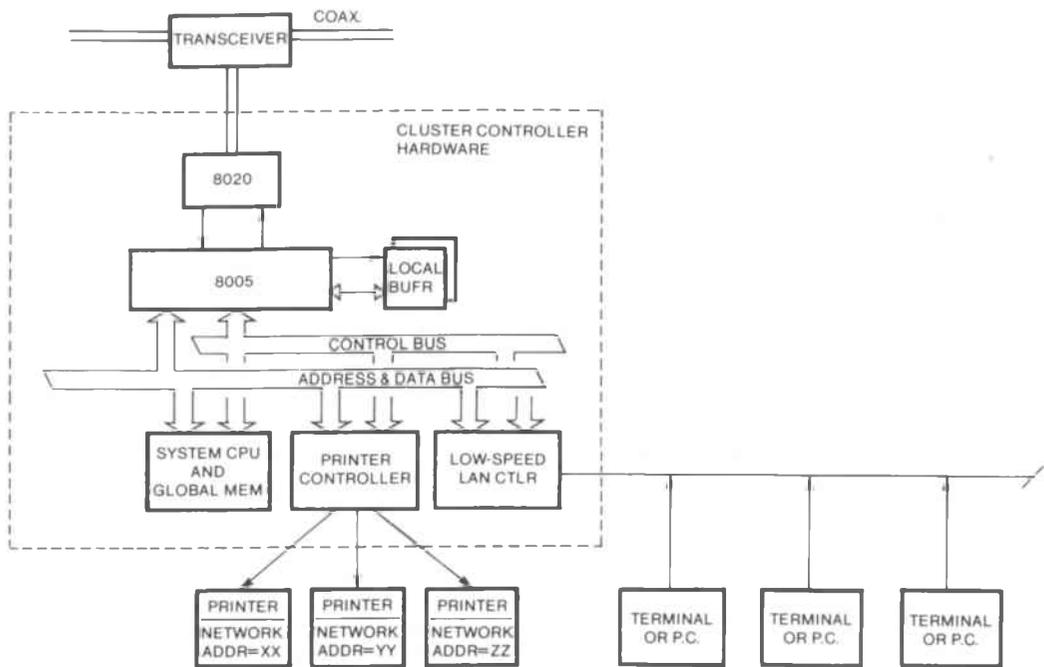
Figure 4. Implementing a local buffer for Ethernet traffic, using static RAM (a), and dynamic RAM (b). DRAMs are lower in cost, but require refresh circuitry.



ATTACHMENT UNIT INTERFACE

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**Figure 5. The 8005 Advanced Ethernet Datalink Controller: it supports a local buffer via DRAM, keeps its Ethernet address and configuration data in its own on-board PROM, and provides a very flexible and sophisticated link between your system and Ethernet.**



**Figure 6.** You can connect up to six devices to one Ethernet node using the capability of the 8005 to decode up to six station addresses. In this example, three printers and three PCs or terminals are connected to one Ethernet node. The 8005 and its system CPU controls Ethernet access to and from the devices.

Use DREQ from the 8005 into DRQ0 of the 80186. This is the highest priority DMA request on the 80186. Since the 80186 has no explicit DMA acknowledgment signal, you need to use the peripheral chip select signal: PCS1 is used as the DMA acknowledgment, and PCS0 is the 8005 CS (chip select). The 8005 INTerrupt is connected to the 80186 INTO, and IACK of the 8005 is pulled up, since the 80186 does not provide for its use.

The RDY line of the 8005 is connected to the ARDY (asynchronous ready), since the two chips are each running off their own clocks. At the 80186, pull up SRDY (synchronous ready).

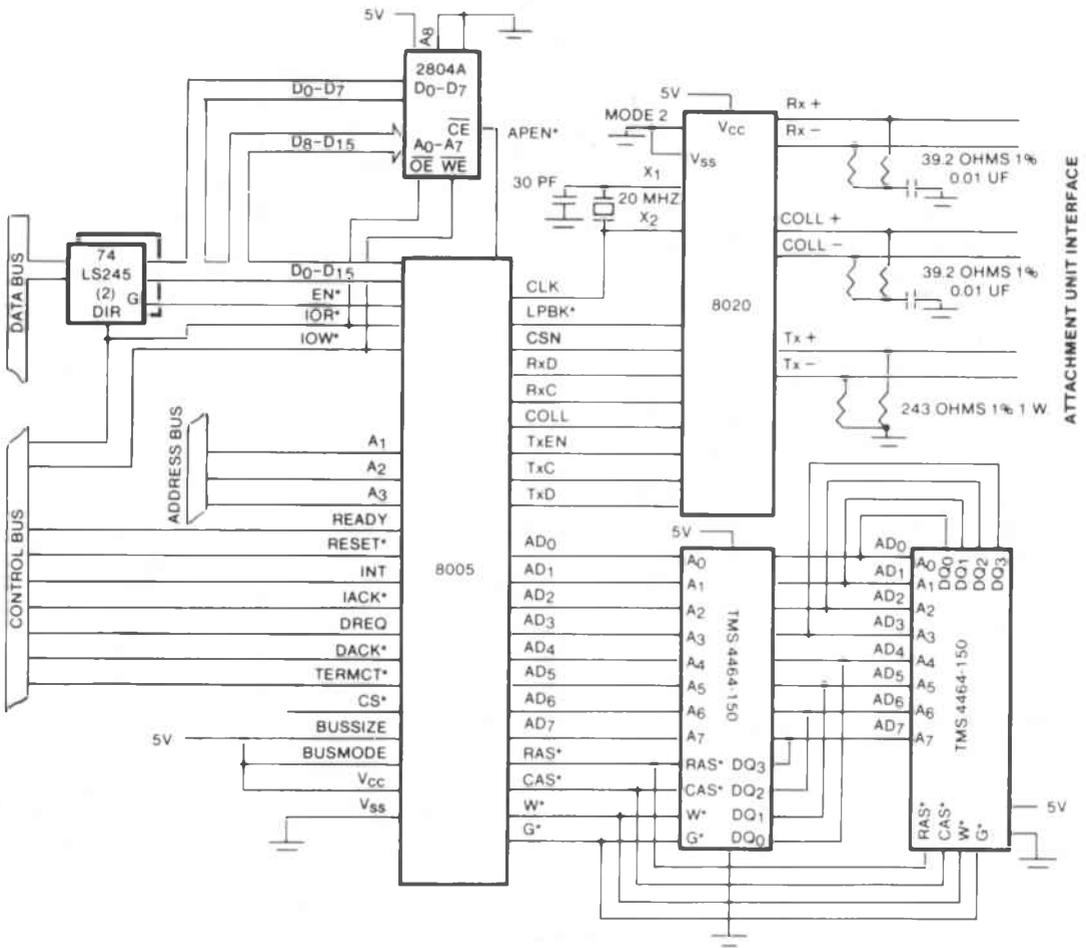
The 80186 does not provide a terminal count output, as do many other DMA controllers, to indicate to the 8005 to drop its DMA request. Therefore, when the 80186 Terminal Count Interrupt occurs, software must disable the DMA request in the 8005 by setting bit 11 in the command register.

### Other Support Circuits

The 8005 supports a PROM, shown here as a 2804A E<sup>2</sup>PROM. The PROM is used primarily to store its Ethernet address and configuration data, but other convenient data may be stored there too.

The 8005 supports the TI TMS 4464 DRAMs (or equivalent) with a minimum of PC board circuit traces by multiplexing both address and data lines to the DRAMs. Two DRAM chips provide an ample 64 Kbytes of Packet Buffer storage. The 8005 allows you to partition this buffer into receive and transmit areas of your own choice.

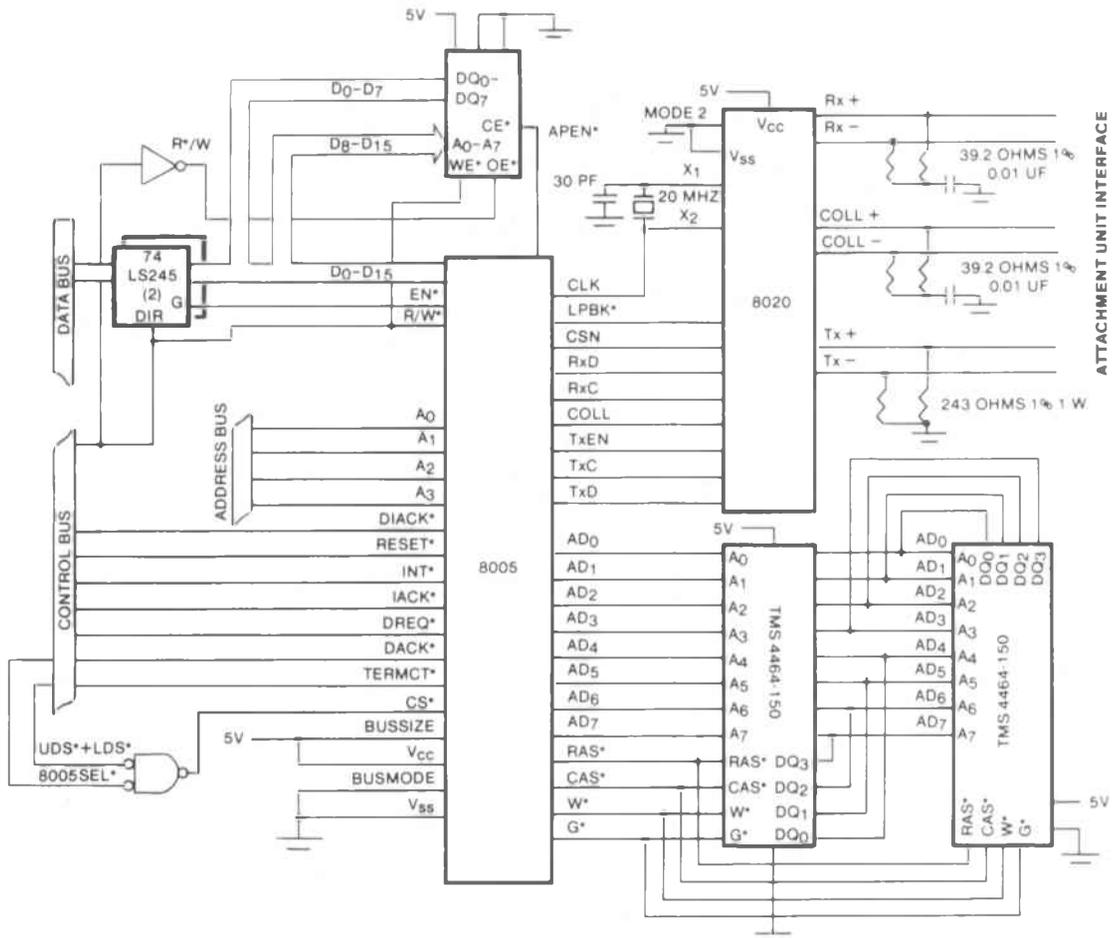
Finally, the diode RC network provides a power on reset pulse (minimum 10 microseconds wide) for both the 8005 and 80186.



INTERCONNECT DIAGRAM  
8005, 16 BIT BUS, INTEL MODE

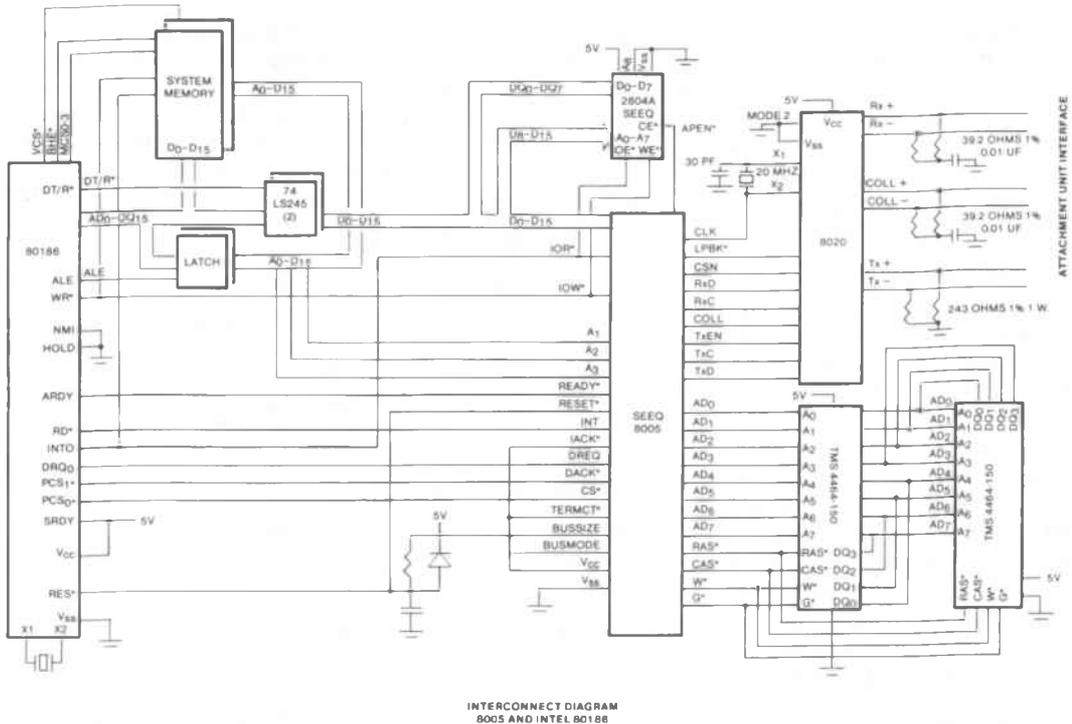
Figure 7. The 8005 interfaced with an Intel processor. This example illustrates the use of a 16 bit bus, since BUSSIZE is a ONE.

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INTERCONNECT DIAGRAM  
8005, 16 BIT BUS, MOTOROLA MODE

Figure 8. The 8005 in a Motorola environment, and with a 16 bit bus size.



INTERCONNECT DIAGRAM  
8005 AND INTEL 80186

**Figure 9.** The use of the 8005 and the Intel 80186 to implement a board level intelligent Ethernet data link. The 80186 is a good companion for the 8005, since it has an on-chip DMA controller. The 8005 supports an address PROM, and 64 Kbytes of DRAM to serve as a local Packet Buffer.

### The 8005 in Non Ethernet Applications

The Ethernet, because of its simplicity and high speed, is often used in smaller physical configurations than those for which it was originally intended. Applications include communications between processors in a large parallel processing engine.

The 8005, because of its configurability, can be "trimmed down" for use in networks which need not strictly follow the Ethernet format.

The Ethernet address is six bytes long. The 8005 may be configured to accept just a 2 byte address, saving four bytes per address in a packet. Since there are two address fields per packet (destination and source), eight bytes are saved.

Ethernet specifies a minimum "slot time" of 51.2 microseconds. This represents the time required for one round trip of a packet on a maximum

length cable, and is required for reliable collision detection. The 8005 may be configured for a slot time of 12 microseconds, which shortens waiting time after a collision. Additionally, when you select the shorter slot time, the 8005 automatically reduces the Collision Jam Pattern from 8 to two bytes, and reduces the interframe spacing from 9.6 to 2.4 microseconds.

Refer to the 8005 data sheet for more detail on selecting these optional parameters.

### Configuring the 8005

This step is required following hardware reset or software reset. Note that a hardware reset must be provided following power on. Following reset, allow 10 microseconds after the reset before attempting access to the part.

Configuring includes loading the Ethernet station address(es), selecting transmit and receive packet buffer size and defining interrupt conditions and an optional interrupt vector.

All this information may be stored in a PROM on the same PC board as the 8005. This allows the assigned Ethernet station address(es) to travel with the board.

### Register Architecture

The general approach to initializing the 8005 consists of reading information from the PROM into system RAM and writing it back into several registers inside the chip. See Figure 10, which depicts the Register Model of the 8005.

There are nine 16-bit registers which are directly accessible by using the signals Chip Select, I/O read, I/O write and  $A_1$  through  $A_3$ . There are also four registers which are selected by the buffer window code bits and accessed indirectly through the buffer window register.

In the discussion below, note that the 8005 has been configured for a 16 bit bus. Input  $A_0$  (pin 54) is ignored when in 16 bit mode, and is shown as a "Don't Care" (X). In 8 bit mode,  $A_0$  selects the low order byte when a ZERO, and the high order byte when a ONE.

### Reading the Address (EE) PROM

After reset, if you are using a local Address PROM, write that location to the DMA Address Register which points to the first configuration byte in the PROM. Select access to the Address PROM by writing 0006 to the Buffer Code Bits in Configuration Register #1. The 8005 will then drive the chip enable line of the PROM via APEN (pin 10) for each Read or Write to the Buffer Window Register. When all configuration and station address bytes have been moved into system RAM, the next step is to write them into the 8005.

### Loading Indirect Registers

Indirect registers are selected by the buffer code in Configuration Register #1 and accessed through the buffer window register. All indirect registers are 8 bits wide and therefore only use data bits  $D_0$ - $D_7$ .

### Station Address Registers

To load the station address registers, select the desired station address register set by writing a

value from 0000 to 0005 to Configuration Register #1. Then write the appropriate 6 byte address to the buffer window register, one byte at a time, with the most significant byte first, and the least significant byte last. Each write automatically increments an internal pointer register to the next byte of the station address. Repeat this process until you have loaded all desired station address registers.

### Specify Transmit Buffer Size

Write a 0007 to Configuration Register #1 to select the Transmit End Area register. Write an 8 bit value to the Buffer Window register which specifies the most significant byte of the last address in the Transmit Buffer space.

For example, to define space for four packets, each 1514 bytes long:

$$\begin{aligned} 1514 \times 4 &= 6056 \text{ bytes for data} \\ 4 \times 4 &= \underline{16} \text{ bytes for header} \\ &6072 \text{ bytes required;} \end{aligned}$$

$$6072/256 = 23+, \text{ or hex } 0017$$

Thus, we would write hex 0017 to the transmit end area register. This also sets the receive buffer area, by default, to start at hex 1800, which leaves 58 Kbytes (hex FFFF minus hex 1800) for receive packets.

If interrupts will be enabled and an interrupt vector is required, write a 9 into Configuration Register #1 to select the Interrupt Vector Register, and then write the 8 bit interrupt vector into the Buffer Window Register.

### Specify Receive Buffer Size

Write an 8 bit value into the least significant byte of the Receive End Area Register to specify the most significant byte of the last buffer address for receive packets. This would normally be hex FF if the rest of the local buffer is to be used for received frames.

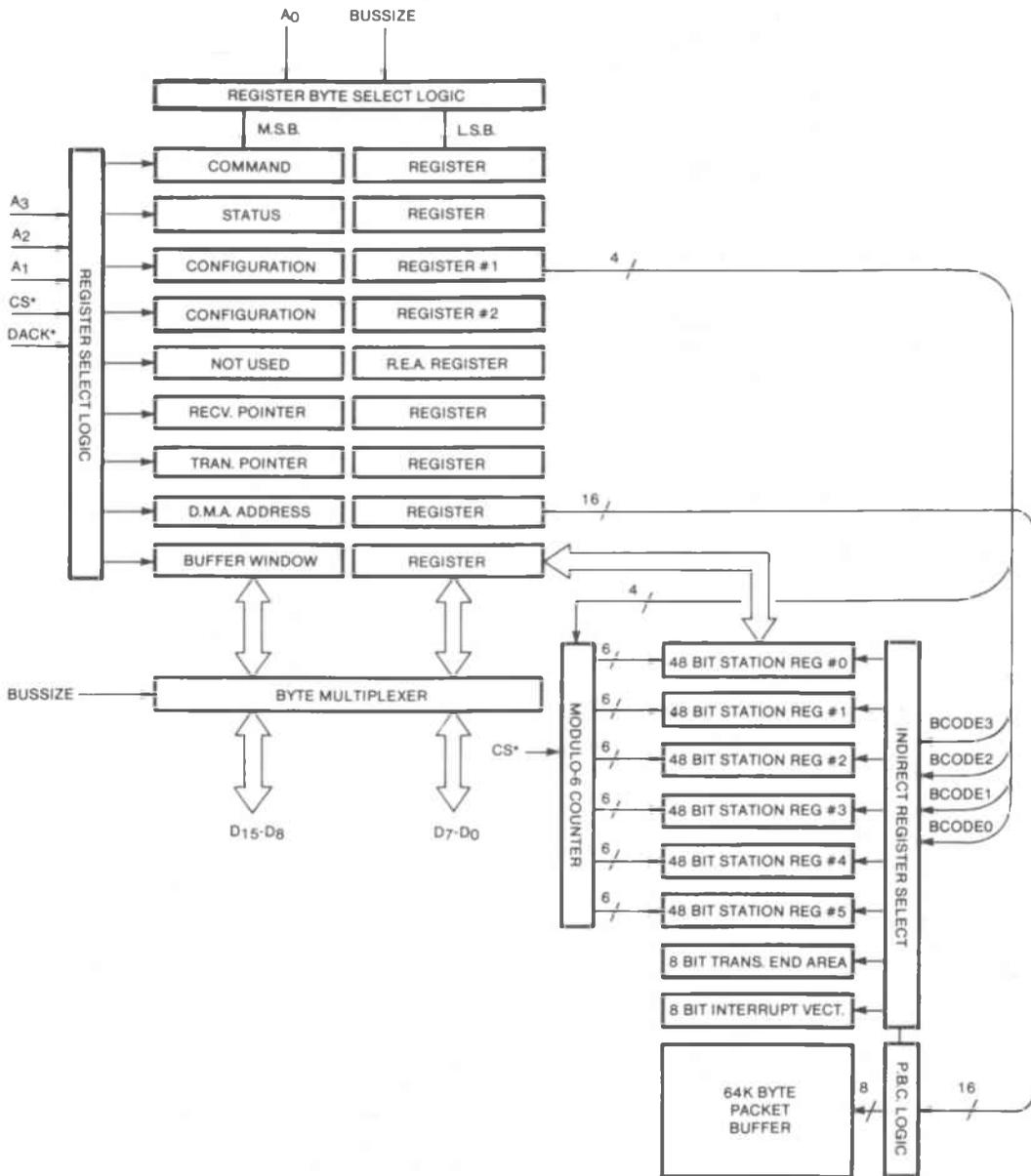
### Loading Direct Access Registers

#### Initialize Transmit Pointer Register

Write 0000 to this register.

#### Configuration Register #1

Loading this register defines receiver match modes, enables station address register sets and sets up DMA burst interval and size. Access this register by setting  $A_3$ - $A_0$  to 001X.



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**Figure 10. Register Model, which illustrates the register architecture inside the 8005. Using both directly and indirectly accessible registers lowers pin count. All access to indirect registers and the Packet Buffer is through the Buffer Window Register.**

## Configuration Register #2

Following reset, this register is configured for IEEE 802.3 compatible network interface. It contains bits to select non-IEEE 802.3 network operation, diagnostic modes (CRC enable/disable for both receive and transmit), enable receiving packets with errors (short frames, dribble errors, CRC errors, overflow errors), select byte order for 16 bit bus and enable automatic receive end area update.

### Initialize Receive Pointer Register

Load this register with the same value as the Receive Start Area (16 bit Transmit End Area address plus hex 0100). Save this value, since it points to the first byte of the next packet header, and you will need it to find the next received packet.

In the example above, the Transmit End Area address was hex 17FF. Therefore, the Receive Pointer Register should be loaded with hex 1800.

### Initialize DMA Address Register

If no packets are to be loaded into the transmit area, load this register with the contents of the Receive Pointer Register.

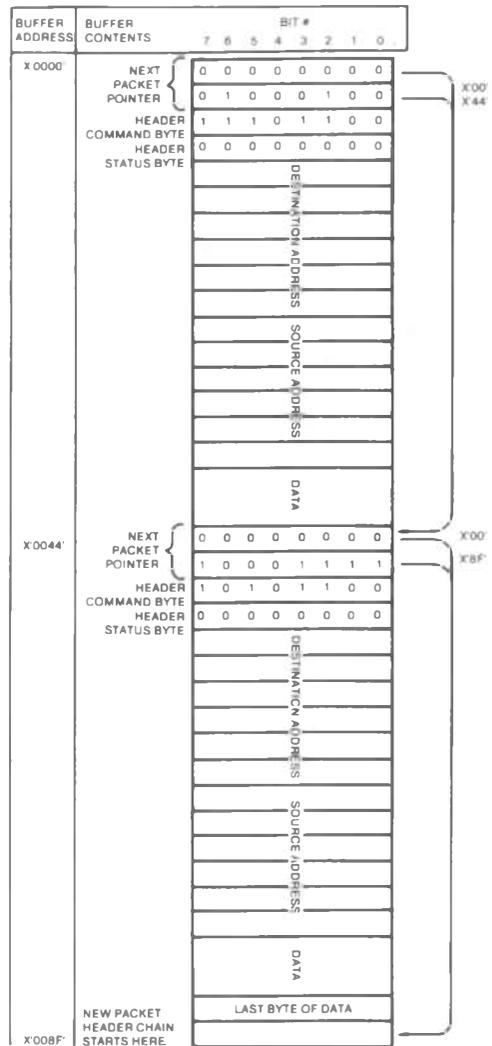
### Command/Status Register

Set  $R_{XON}$  (bit 9), and, if desired,  $R_{XINT}$  Enabl (bit 1) to ONEs. If you are not using interrupts, you may poll  $R_{XINT}$  (bit 5) to see if a frame has been received.

### Transmitting a Frame

This discussion assumes that the system is connected to an IEEE 802.3 compatible network. The contents of a Transmit frame have no meaning to the Packet Buffer Controller and the Ethernet Data Link Controller circuitry, and can be arbitrary in length and content. As discussed above, transmission of the Preamble and CRC (frame check sequence) can be suppressed under software control for specialized network requirements or diagnostic tests.

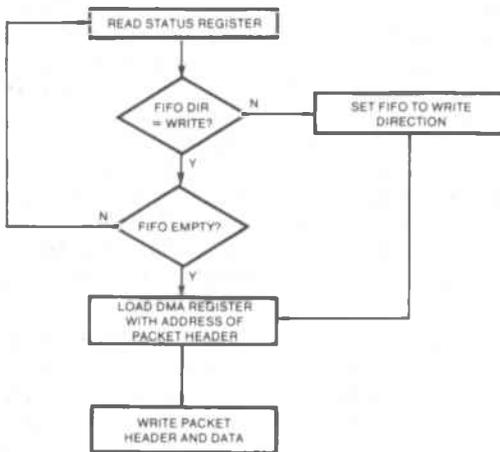
After you have gone through the configuring as outlined above, the 8005 is ready to receive or transmit frames. Refer to Figure 2 and recall that a frame consists of from 64 to 1514 bytes, which includes a 6 byte destination address, a 6 byte source address, and an area for data all of which is supplied by your system software. The entire frame has a prefix containing a 62 bit preamble



**Figure 11. Transmit Packet Chain, residing in the Packet Buffer, and ready to be transmitted. Two packets are in this chain. Note that the Packet Buffer is nondestructively read, and the packets are still in the buffer after they have been transmitted. After transmission, the 8005 updates the Header Status Byte (byte 4). The first two bytes of the Packet Header point to the address of the first byte of the second Packet Header.**

(which synchronizes the phase-locked-loop in the Manchester Code Converter with respect to the received packet), and a 2 bit start frame delimiter. Following the data field there is a 4 byte frame check sequence. All of the components of the prefix and the CRC are supplied by the 8005.

A packet is prepared for transmission by writing into the Transmit Buffer Area a 4 byte header, followed by the destination address, the source address, and finally the data field. Refer to Figure 11. You may choose to do this via programmed I/O, or via an external DMA controller. Frames may be chained together up to the capacity of the available Transmit Buffer Area by using the Next Packet Pointer (first two bytes) and the Chain Continue bit (bit 6) in the Transmit Header Command byte.

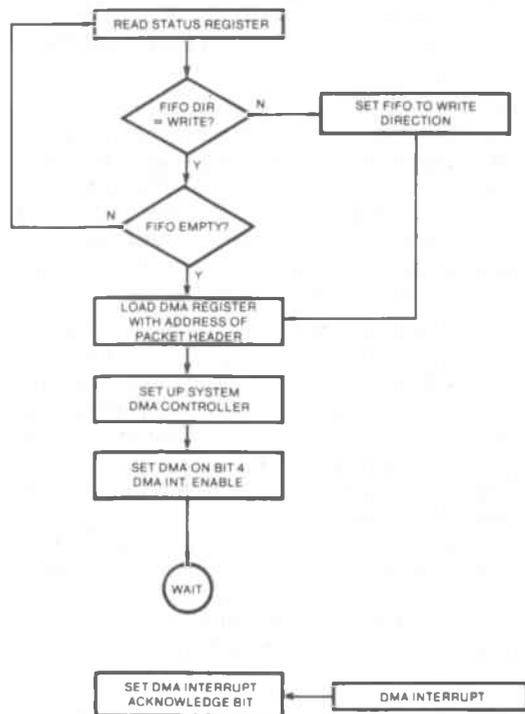


LOADING TRANSMIT PACKETS INTO LOCAL BUFFER PROGRAMMED I/O

**Figure 12. Loading Transmit Packets Into the local Buffer, under Programmed I/O conditions. Note that, if you change the direction of the DMA FIFO, or load the DMA Pointer Register, you will lose any data stored in the FIFO.**

Refer to Figure 12. Read the Status Register to see if the DMA FIFO direction is set to the Packet Buffer (bit 15 cleared). If it is and the DMA register is not going to be loaded with a new value then data can be written immediately. If the DMA register is to be changed, then check to ensure that the FIFO is empty (Status Register bit 4 set). If the FIFO is not empty, continue testing bit 14 until the FIFO is empty. If you change the FIFO direction or write to the DMA Register, FIFO contents will be cleared.

If necessary, load the DMA Register with the address for the first byte of the Packet Header, and write Packet Header and data into the FIFO. The first Packet Header address is normally 0000.



LOADING TRANSMIT PACKETS INTO LOCAL BUFFER DMA TRANSFER WITH INTERRUPT

**Figure 13. Loading Transmit Packets Into the Local Buffer under DMA transfer, using Interrupt.**

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Figure 13 depicts the same operation, only under DMA control. After you set up the system DMA controller, set DMA ON (Command Register, bit 8), and DMA Interrupt Enable (Command Register, bit 0), if desired. The former enables the DMA request logic, and the latter causes an interrupt to be generated at the completion of a DMA operation i.e., when terminal count has been input.

After all of the packets in a given chain have been written into the Transmit Buffer Area, load the Transmit Pointer Register with the address of the first byte of the first transmit packet header, set  $TxON$  (bit 10) and, optionally,  $TxINTEnabl$  (bit 2) to ONes in the Command/Status Register.

The 8005 will then read the first header, which is pointed to by the Transmit Pointer Register, and process that packet, and all additional packets in the packet chain in turn. Any retransmission of a packet due to a collision will be automatically handled by the 8005, thus relieving your system from having to transfer that packet of data more than once.

When a packet has been successfully transmitted (or 16 collisions occur), the Done bit (bit 7) in the transmit header status byte will be set to a ONE. The Transmit Buffer Area occupied by that packet is now available for another packet, and may be written to at the same time as subsequent packets are being transmitted. The 8005 will move to the next packet in the chain.

When all packets in a chain have been completed (transmitted successfully or collided 16 times), the 8005 resets  $TxON$  (bit 10) in the status register to indicate that it is ready to transmit another packet chain. If 16 collisions occur on a packet, the 8005 stops transmission attempts for that packet only and moves to the next packet in the chain, if one exists. In the example in Figure 11, bits 2 and 3 are ON in the transmit header command byte which will cause the 8005 to set the transmit interrupt bit in the status register and, if enabled, interrupt the processor when 16 collisions occur or the transmission is successful.

The last packet in the chain is denoted by having the Chain Continue bit cleared to a ZERO. The Next Packet Pointer points to the address following the last byte of the last packet.

You may treat the transmit packet buffer in one of two ways:

1. As a circular buffer with wraparound, where you remember the address to load new packet

headers and packet data. The DMA register automatically wraps around to address 0 when the transmit end area has been reached.

2. As a linear buffer, where you reset the transmit pointer to 0000 after each packet chain transmission.

## Receiving Frames

Once the 8005 has been configured and the receiver enabled, frames which meet the match mode and station address requirements specified in Configuration Register #1 and the enable bits 2 - 5 in Configuration Register #2 will be moved into the Receive Buffer Area beginning at the address contained in the Receive Pointer Register.

When one or more packets are available in the receive area, the 8005 sets  $Rx$  Interrupt (bit 5) in the Command/Status Register to a ONE. If receive interrupts are enabled (Command Register bit 1 set), then the external interrupt (pin 11) is asserted. Frame header and data can now be read by loading the DMA Register with the starting address of the Packet Header and executing successive reads. If Auto Updat REA (bit 1 of Configuration Register #2) is set, the Receive End Area Register will be updated with the upper byte of the DMA register each time a DMA read occurs. This releases buffer space as its contents are read, and allows for the receipt of more data at the same time as data is being read out.

The action taken on a receive packet depends on the status of the packet and its contents. If the packet status is bad, it may be skipped entirely without transferring any of its data to system memory by loading the Receive End Area Register with the most significant byte of the next packet pointer. This will release the buffer space of the previous packet for future packets. In like fashion, if the packet data shows it to be an "overhead" packet (such as a Packet Acknowledgement), this can be so noted in network software and the packet skipped. Thus, unnecessary transfer of the packet over the system bus can be avoided, and system bandwidth preserved. If the packet data must be processed, just the information portion of a packet (exclusive of any bytes used to pad the packet to a minimum size) can be read to system memory by programmed I/O or by an external DMA controller.

## Receive Packet Chaining

The 8005 automatically chains together receive packets using a circular FIFO buffer structure. Each packet is prefaced by a 4 byte header whose first two bytes form a 16 bit address that points to the next header. A chain of packets always ends with a header-only packet whose 4 bytes equal 00. The address of this header-only packet should be saved, since it will contain the header of the next packet received. It is a simple matter to follow the packet chain from header to header until the chain Continue/End bit is read as a ZERO, calculate the length of the chain and set up the DMA Register and an external DMA controller to transfer the entire chain of packets to system memory if desired. This is advisable in applications where high average receive data rates are expected and data must be moved quickly from the local buffer to the system memory at the expense of bus bandwidth. To minimize system bus utilization, packets can be moved one at a time; this permits moving only the information content of a packet.

### Calculating Packet Chain Length

In order to perform a DMA transfer, you need to give the DMA controller the "count"; i.e., how many bytes (or words, in a 16 bit system) will be transferred. To do that, you need to calculate how many bytes are available in the Packet Buffer as a result of receive activity.

Refer to Figure 17. This flow chart illustrates the steps required to calculate the length of the packet chain.

The first step requires that you know the Packet Buffer address of the last packet header read in the most previous receipt of Ethernet data. If the 8005 has just been initialized, the address is the beginning of the Receive Packet Buffer which was determined earlier in this note (hex 1800). If packets have been previously been read this address will be the location of the header last read that had the chain continue/end bit reset.

The next step, referring to Figure 17, is to turn off the Auto Updat REA (Configuration Register #2, bit 1). This insures that the 8005 will not use the area occupied by this packet chain for new receive data.

Read each Packet Pointer in turn, and then read the Header Status byte immediately after the Pointer, which is Byte #3. Bit 6 of Byte #3 is the

Chain Continue bit. Continue reading this bit in each packet header until this bit goes to ZERO. This signals the end of the chain. Save the local buffer address of the first byte of this last header as this is the address of the header for the next packet received. Subtract the address of the first header in the chain from this address. If the result is a positive number, you have the chain length directly.

If the result is negative it denotes that the Receive Pointer Register has wrapped around past the beginning address of the receive area. The chain length will be equal to the sum of the receive buffer size plus the value (including sign) of this result. You already know the buffer size, since you defined it during configuration of the 8005: hex FFFF minus the receive start address (defined during configuration) plus 1. For the previous example, the buffer length is hex E800 (FFFF - 1800 + 1). Load the chain length into the DMA controller, and set Auto Updat REA. You are now ready to read data out of the receive buffer and into system memory.

There are two ways to read Packets out of the Local Buffer:

1. Via programmed I/O.
2. Via DMA transfer.

The front end portion of each procedure is the same: first, check to see if the FIFO is empty; then set it to Read. If the FIFO is not empty, check to see if it is in the Write direction. If not, load the DMA Register with the address of the next Packet Header. If this is the first Packet to be read, this address will be that which was derived when you defined the Transmit Buffer size during configuration of the 8005.

### Reading Packets Using Programmed I/O

The data path between the local buffer and the host bus is buffered by a 16 byte FIFO called the DMA FIFO. It serves as a rate buffer between the host and the local buffer, especially for 16-bit data transfers. Because the local buffer is a shared resource (there are 4 ports including the DRAM refresh port), the initial read from the buffer window which follows loading the DMA register may take eight microseconds worst case. The 8005 signals this delay by deasserting Ready (if Busmode=1) or delaying D<sub>TACK</sub> (if Busmode=0). If this initial read wait state is unacceptable, then the buffer window interrupt feature can be used.

The buffer window interrupt is asserted for programmed I/O reads (not DMA reads) when the DMA FIFO has data available.

Under Programmed I/O control (see Figure 14), after you load the DMA Register, read Status Register bit 7, Buffer Window Interrupt or wait for a hardware Buffer Window Interrupt if it is enabled. When the interrupt is asserted, read Packet Header and data out of the receive FIFO, via the Buffer Window, until all bytes have been transferred.

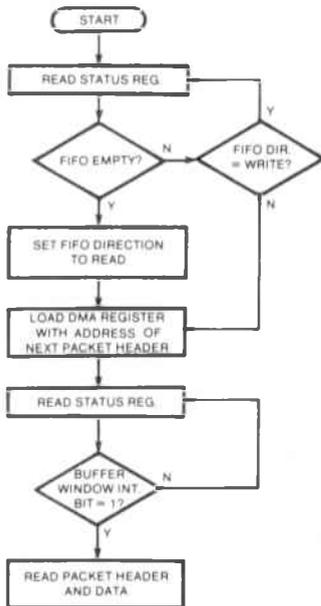
### Reading Packets Using DMA

The second approach is by DMA transfer. See Figure 15. After loading the DMA Register, load the system DMA controller with the destination address in system memory, and the previously

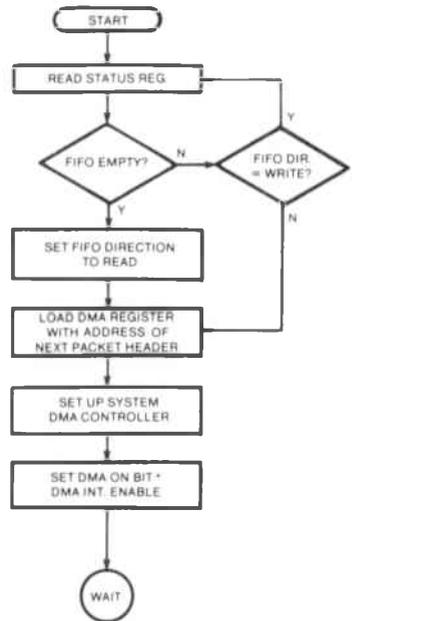
calculated packet chain length. Then set DMA ON (bit 8 in the Command Register). This enables the DMA Request logic inside the 8005. Optionally, set DMA Interrupt Enable, which will cause an Interrupt to be generated when the DMA controller has asserted Terminal Count. The DMA Request output signal will be asserted when there are a sufficient number of bytes in the DMA FIFO to satisfy the DMA Burst Size (2, 4, 8, or 16 bytes) which you selected earlier when configuring the 8005.

### Interrupts

There are several interrupt sources in the 8005. This section describes these interrupts and how to service them. For this discussion, refer to Figure 18.



READING A PACKET FROM LOCAL BUFFER PROGRAMMED I/O



READING A PACKET FROM LOCAL BUFFER DMA TRANSFER WITH INTERRUPT

Figure 14. Reading Packets out of the FIFO using the Programmed I/O procedure.

Figure 15. Reading the Local Buffer under DMA control.

## Transmit Interrupts

There are four transmit interrupt sources in the 8005; Babble, Collision, 16 Collisions, and Transmit Success. Each of these can set the transmit interrupt bit in the status register if so programmed in the transmit header command byte. If  $T_x$  Interrupt Enable (Command Register bit 2) is set, the 8005 will also assert an interrupt on pin 11. The transmit interrupt is cleared by setting  $T_xINTACK$  (bit 6) in the command register.

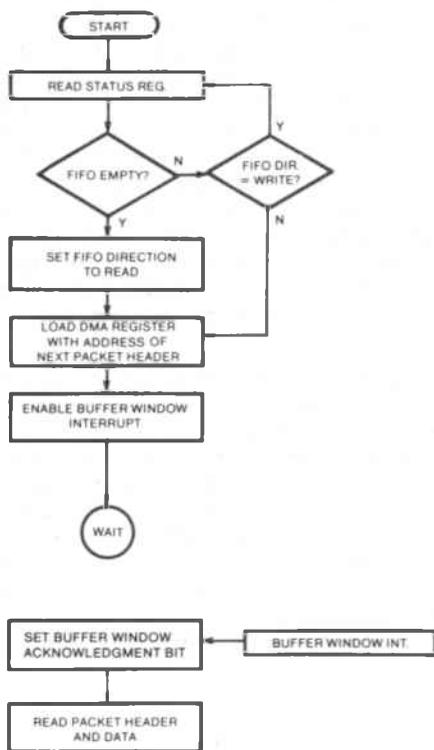
## Babble Interrupt

The 8005 will transmit packets as large as will fit in the transmit buffer. The IEEE 802.3 standard

specifies a maximum packet size of 1514 bytes. The babble interrupt indicates that a packet larger than 1514 bytes was transmitted.

## Collision Interrupt

When a packet collision occurs, the 8005 packet buffer controller automatically restores its transmit pointer to the beginning of the packet and schedules retransmission following the back-off time. In some applications it may be desirable to record the number of collisions that occur. This bit enables setting the  $T_xINT$  bit in the status register for each collision.



READING A PACKET FROM LOCAL BUFFER USING BUFFER WINDOW INTERRUPT

Figure 16. Reading a Packet from the local Packet Buffer using the Buffer Window Interrupt approach.

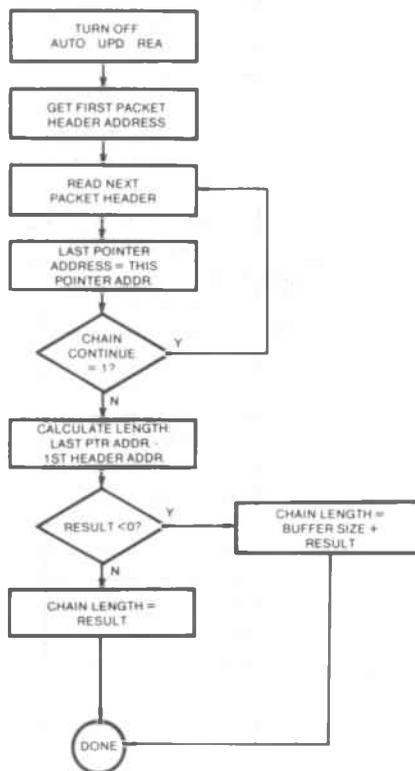


Figure 17. The steps necessary to calculate the length of a Packet Chain. You need to save the address of the last header in the last packet read, in order to perform the calculation.

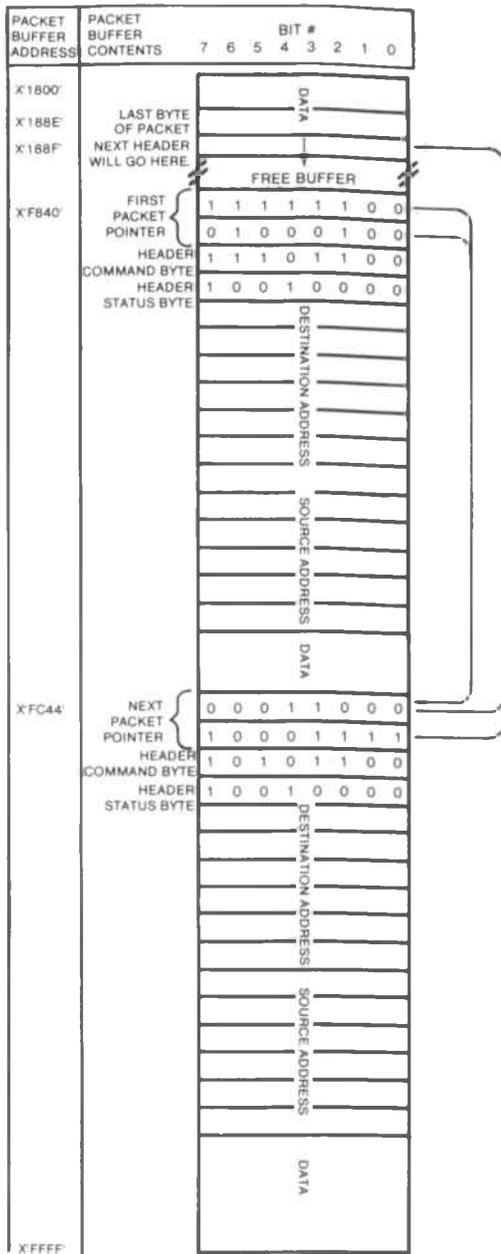


Figure 17a. Example of two receive packets in a packet chain with wraparound.

### 16 Collisions Interrupt

The 8005 counts the number of collisions that occur on each packet. If a packet has collided 16 times, the usual cause is a network fault such as an unterminated coaxial cable or an open in the cable. This interrupt notifies the host that a packet has collided 16 times, and the packet buffer controller will now abandon transmit attempts for that packet and move on to the next packet in the chain if one exists.

### Transmit Successful Interrupt

This interrupt indicates that a packet was successfully transmitted with less than 16 collisions.

### Receive Interrupts

The 8005 sets the receive interrupt bit (status register bit 5) whenever a packet that meets the criteria in bits 2 - 5 of Configuration Register #2 has been placed in the local buffer. It will remain set and, if the receive interrupt enable bit is also set, the external interrupt will remain asserted until the receive interrupt acknowledge bit is set. If a separate interrupt for each packet is desired, the receive interrupt should be acknowledged within 70 microseconds, which is the minimum time for receipt of a subsequent 64 byte packet. If more than 70 microseconds elapses before acknowledging a receive interrupt, it is possible for additional packets to be added to the packet chain.

The 8005 protects the receive interrupt condition such that if a new interrupt is being generated while the host is setting the receive interrupt acknowledge, the receive interrupt will persist. If, however, a new frame is received after the interrupt acknowledge and before the calculation of the packet chain length, the packet chain which is read will include the new packet associated with the new interrupt. The new interrupt, when serviced, will now be associated with an empty packet since it was part of the previous chain.

### DMA Interrupts

The DMA interrupt bit in the status register is set following receipt of terminal count from the external DMA controller. If the DMA interrupt enable bit (command register bit #0) is also set, an external interrupt will be asserted. The interrupt is cleared by writing a 1 to the DMA interrupt acknowledge bit.

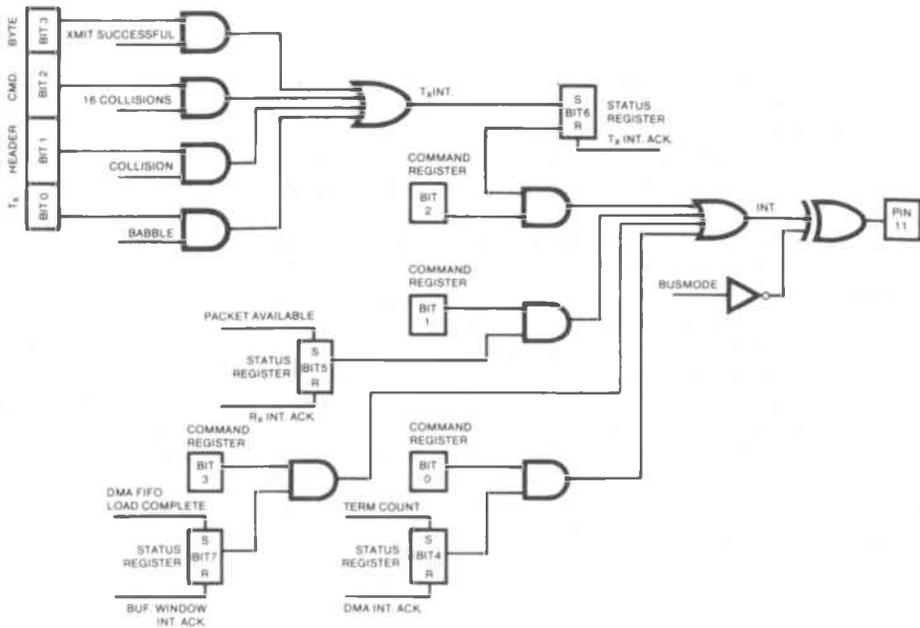


Figure 18. Functional diagram of interrupt logic.

### Self-Test and Network Diagnostics

The 8005 contains a number of special features for self-test and network diagnostic support.

#### Loopback

Two forms of loopback are possible with the 8005. Local loopback is accomplished when the 8005 is connected to an 8020 Manchester Code Converter. When bit 1 of Configuration Register #2 is set, the loopback pin of the 8020 will be brought low. This causes transmitted data to be looped back to the receiver of the 8020. If the packet transmitted meets the match mode and is addressed to one of the 8005's enabled station addresses, it will be received and placed in the local buffer. Using diagnostic control bits 9 and 10 in Configuration Register #2, it is possible to transmit packets with CRC errors to check the receive CRC logic, and to include the CRC in a receive packet to check the transmit CRC logic. Loopback can also be accomplished by connecting the 8020 to an Ethernet transceiver. Because the network is half-duplex, any data transmitted will also be received. Thus the same loopback test as above can be performed while the network is active by simply sending a packet to oneself.

### Interrupts

The 8005 has separate control bits for turning on or off the receive logic, transmit logic and DMA logic. The interrupts for these functions can be tested without actually performing the function by setting both the on and off control bits simultaneously. For example, if the receive interrupt logic is to be tested set both  $R_{XON}$  and  $R_{XOFF}$  bits in the command register. This will cause the receive interrupt bit in the status register to be set and, if the receive interrupt enable bit is also set, will cause an external interrupt. This mode has no effect on any logic other than the interrupt logic and associated status register bit, i.e., packets can be transmitted and received while this diagnostic mode is set.

### Detecting Network Cable Faults

It is possible to make a gross determination of cable faults by taking advantage of the full-duplex nature of the 8005: although it will not transmit while receiving (that would violate the Ethernet specification), it does receive while transmitting, as long as the packet destination address fits the receiver match mode.

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### **Cable Opens/Missing Terminator**

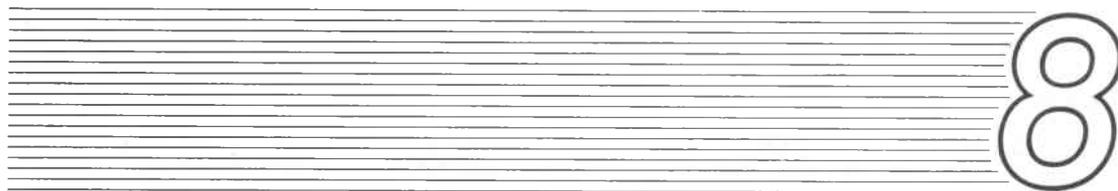
An open coaxial cable or a missing cable terminator results in the transmission line being terminated in an infinite impedance. Thus, any data transmitted will be reflected back from the impedance mismatch some time delay after it is transmitted. This time delay depends on the physical distance to the impedance mismatch, so the length of the packet must be large enough to insure that data are still being transmitted after one round trip propagation delay to the mismatch. A 256 byte packet should be an adequate size. The reflected signal will partially cancel the transmitted signal and cause a collision to be detected by the transceiver. Thus an open is indicated by repeated collisions when transmitting a packet or, if the network is known to be quiet (no other nodes active), a single collision when transmitting. It is also possible to make a rough

determination of where the fault is by enabling receipt of packets with errors (Configuration Register #2 bits 3 - 5) and then counting the number of bytes correctly received. Note that if the cable open is very close to the transmitting node, the collision may occur during the preamble and the 8005 would unconditionally reject the receive packet.

### **Cable Shorts**

A shorted coaxial cable causes premature loss of carrier sense to the receiver of the 8005 while it is transmitting. It is therefore possible to send a packet of at least 256 bytes to oneself with the receiver enabled to accept frames with errors. A cable short results in a truncated receive packet; the size of the receive packet indicates the rough distance to the cable short.

# **Memory Products Application Note**



## ***EEPROM INTERFACING***

*April 1987*

APP. NOTES

**seeq**  
*Technology, Incorporated*

# EEPROM Interfacing

## Introduction

The continuing rapid evolution in semiconductor E<sup>2</sup>ROM memory device technology offers the system designer an ever-increasing choice of function and capability. With these increasing choices for E<sup>2</sup>ROM devices, however, comes the problem of standardization (or lack thereof) concerning such specifications as endurance, timing characteristics, interface requirements, ad infinitum. Today, there are two popular types of commercially available E<sup>2</sup>ROM devices.

Both of these types of devices have the JEDEC-approved pinout shown in Figure 1, including the multi-functional pin 1, but differ in the timing of the control interface. The first E<sup>2</sup>ROM type, the latched type device, such as SEEQ's 52B33 latches the addresses, control, and data inputs on the falling edge of WRITE ENABLE (WE). For this type device, the WE input must remain active low for the duration of the write cycle. The second type of E<sup>2</sup>ROM, the timer-type device, latches addresses, data, and control signals on the rising edge of WRITE ENABLE or the rising edge of CHIP ENABLE (CE). For the timer device, such as SEEQ's 2864 the WE input need not be held low for the entire write cycle. The primary difference between the latched and timer devices is the control timing required to interface to the microprocessor. Each of these types of devices has advantages depending on system performance and configuration requirements.

When the designer attempts to use the advantages of both in the same system, a problem is encountered.

One of the most frustrating problems facing a system designer is the design of an E<sup>2</sup>ROM/microprocessor interface that will allow compatible operation of timer and latched type E<sup>2</sup>ROM devices in the microprocessor-based system. The purpose of this application note is to give examples of cost-effective designs of E<sup>2</sup>ROM/microprocessor interfaces, which allow the use of both timer and latched E<sup>2</sup>ROM devices in the system with no changes required to either the controlling software or the hardware. With the interfaces shown in this application note, it is possible to operate with BOTH latched and timer devices simultaneously in the system if the device access times are compatible.

The microprocessor interfaces described in this application note are for the 8085, 8086, 8088, Z80, and 71840. Software examples are provided for the Z80 and 71840 processors. By extension, the Z80 code is easily transportable to 808X processors. In most cases, the hardware required for compatibility consists of only two additional standard (14-pin) TTL packages.

It is hoped that these example interfaces will assist the system designer in implementing E<sup>2</sup>ROMs in his system. By no means are these special cases presented to limit the system designer, but to provide a starting point for his design. The interface circuits presented are for the family of E<sup>2</sup>ROM devices (16K, 32K, and 64K). Other extensions of the ideas presented may permit lower power, lower cost, or optimization of other parameters deemed more important.

The body of this application note consists of two sections. First, the Basic Operation section gives the theory of operation of all of the interfaces and should be read to familiarize oneself with those factors common to all of the microprocessor interfaces. Second, the Microprocessor Interface section details the design of the TTL interface required for the given microprocessor.

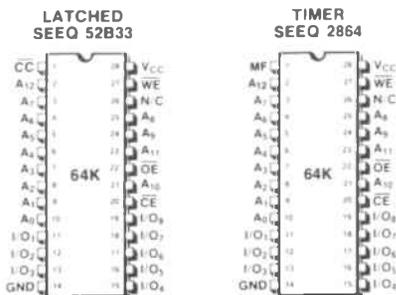


Figure 1. JEDEC Pinout — 64K E<sup>2</sup>ROMs

## Basic Operation

Each of the E<sup>2</sup>ROM microprocessor interfaces described in the next section integrates hardware and software to achieve compatibility between latched and timer E<sup>2</sup>ROM devices. Naturally, both hardware and software are processor-dependent. However, the write cycle used is basically the same for all the examples shown.

For compatibility between the latched and timer E<sup>2</sup>ROM devices, the interface provides control waveforms that have timing compatible with both, since the major difference between latched and timer E<sup>2</sup>ROM devices is the timing of the write control interface to the microprocessor (see Introduction). The basic waveforms for latched and timer E<sup>2</sup>ROMs are shown in Figures 2a and 2b, respectively. The latched type E<sup>2</sup>ROM device acquires data on the leading edge of WRITE ENABLE

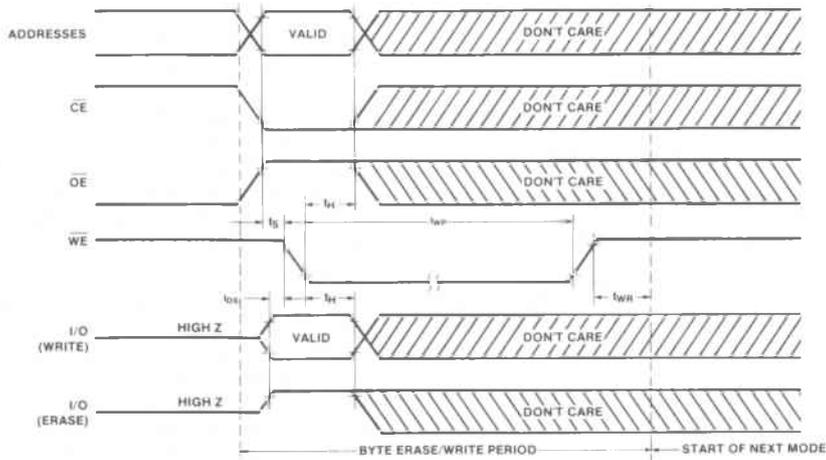


Figure 2a. Latched E<sup>2</sup>ROM Write Cycle

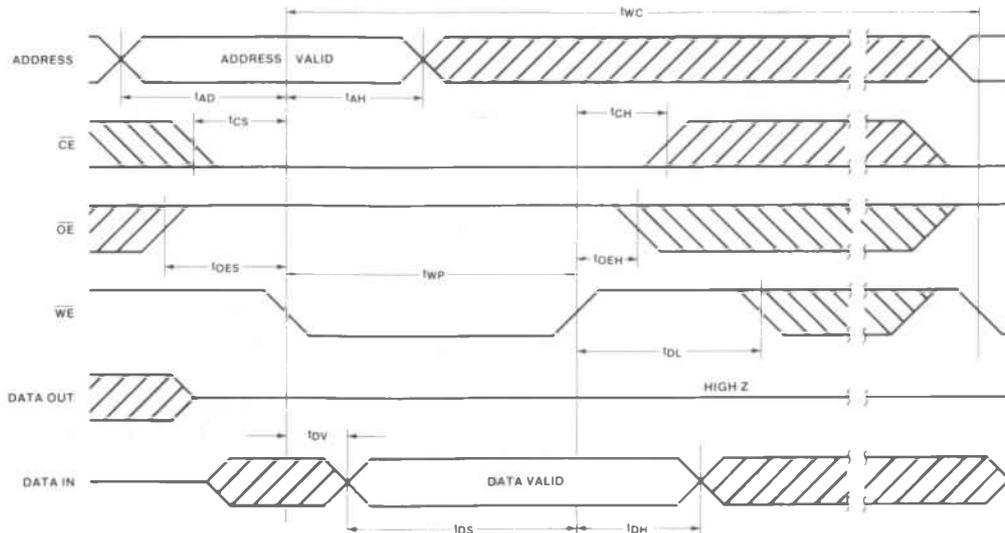


Figure 2b. Timer E<sup>2</sup>ROM Write Cycle

( $\overline{WE}$ ). The timer type device acquires data on either the trailing edge of  $\overline{WE}$  or the trailing edge of  $\overline{CHIP\ ENABLE}$  ( $\overline{CE}$ ). Interface compatibility is achieved between the latched and timer devices by strobing the data, control, and addresses on the leading edge of the Write Enable pulse for the latched device and then by strobing the data on the trailing edge of  $\overline{CHIP\ ENABLE}$  for the timer device (see Figure 3). By using this technique, the hardware interface is greatly simplified.

The software part of an E<sup>2</sup>ROM interface is very simple, but very important. A read operation for both latched and timer E<sup>2</sup>ROM devices is accomplished by a straightforward issuance of a microprocessor Read

command at a particular address (see Figure 4). A write operation, however, involves a more complex process.

The flow chart for writing to the E<sup>2</sup>ROM is the same for all microprocessors and is shown in Figure 5. After a Write command is issued, time is required to allow proper writing to the storage cell of the E<sup>2</sup>ROM device. A Read command is then issued to terminate the write operation. Note that this Read command is not to be used to actually read the E<sup>2</sup>ROM device, but is inserted to reset the logic circuits used to drive the  $\overline{WE}$  input of the E<sup>2</sup>ROM device.

Between initiation and termination of a write cycle, the interface uses some timing mechanism to assure proper write conditions to the E<sup>2</sup>ROM and to know when the E<sup>2</sup>ROM is available for another read/write cycle. The duration of the timeout ( $t_{WPP}$ ) depends upon the type of E<sup>2</sup>ROM used. For all types,  $t_{WPP}$  should fall between the minimum and maximum specifications of all E<sup>2</sup>ROMs for which the application is designed. The latched type of device requires less write time than does the timer type device.

The implementation of this timing can be accomplished in either hardware or software. In hardware timing, a timer can interrupt the processor at regular intervals, or at the end of the desired write time ( $t_{WPP}$ ). In software timing, the processor simply counts down, waiting for the desired  $t_{WPP}$ . For ease of general implementation, the given examples utilize software timing (see Figure 5). The tradeoffs, however, between software and hardware timing comprise an involved topic. The system designer must make this decision, considering such factors as processor throughput, board space, and expense.

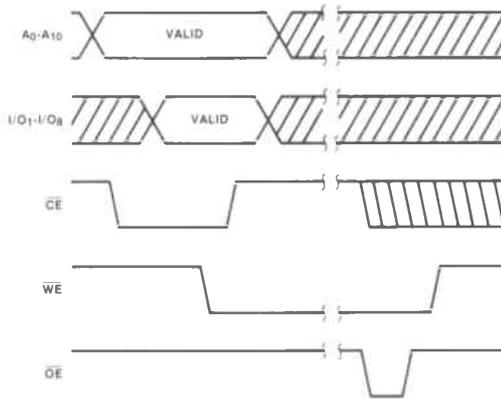
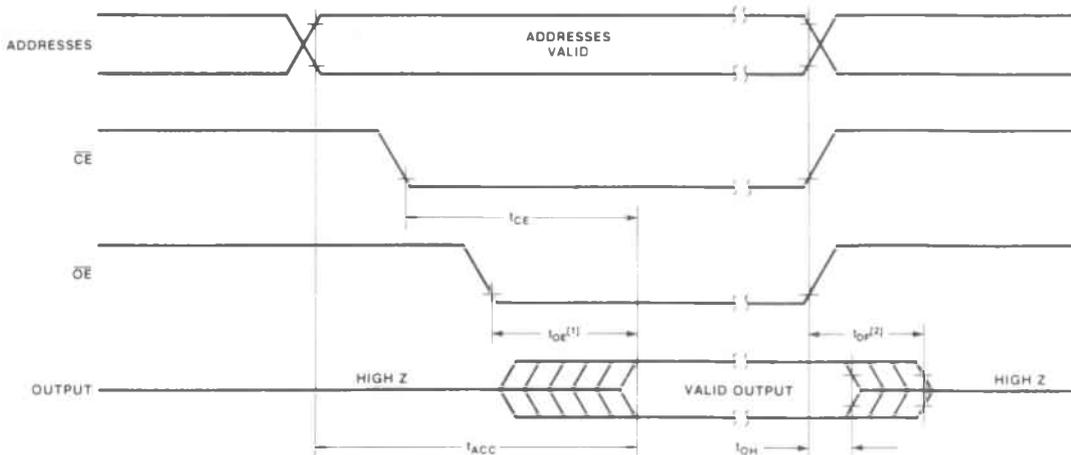


Figure 3. Latched/Timer Compatible E<sup>2</sup>ROM Write Cycle



- Notes: 1  $\overline{OE}$  may be delayed up to  $t_{ACC} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{ACC}$ .  
 2  $t_{OH}$  is specified from  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs first.  
 3 This parameter is periodically sampled.

Figure 4. E<sup>2</sup>ROM Read Cycle

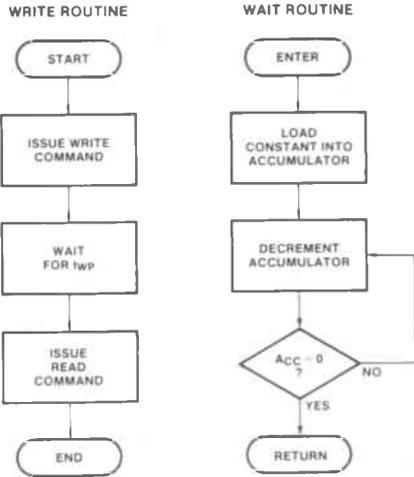


Figure 5. Software Flowchart — E<sup>2</sup>ROM Write Cycle

After the cycle described by Figure 5 is complete, the E<sup>2</sup>ROM device is available to be accessed for another Read or Write command. Often, another read will be performed in order to verify the written data. With the solution proposed, this subsequent read cycle will have normal timing, and all required write recovery parameters will be satisfied.

The general description provided above applies to most of the processors shown in the specific examples below. For more detailed information, the reader should refer to the schematic, waveforms, and software that apply to a specific processor.

## Microprocessor Interfaces

### 8085 Interface

The schematic for the 8085 interface to a timer or latched E<sup>2</sup>ROM device is shown in Figure 6. This interface consists of one each of a 74LS02 and 74LS74 type package and allows the system designer to use the  $\overline{WR}$  signal from the 8085 to initiate the write cycle to the E<sup>2</sup>ROM device. The design permits use of either a timer

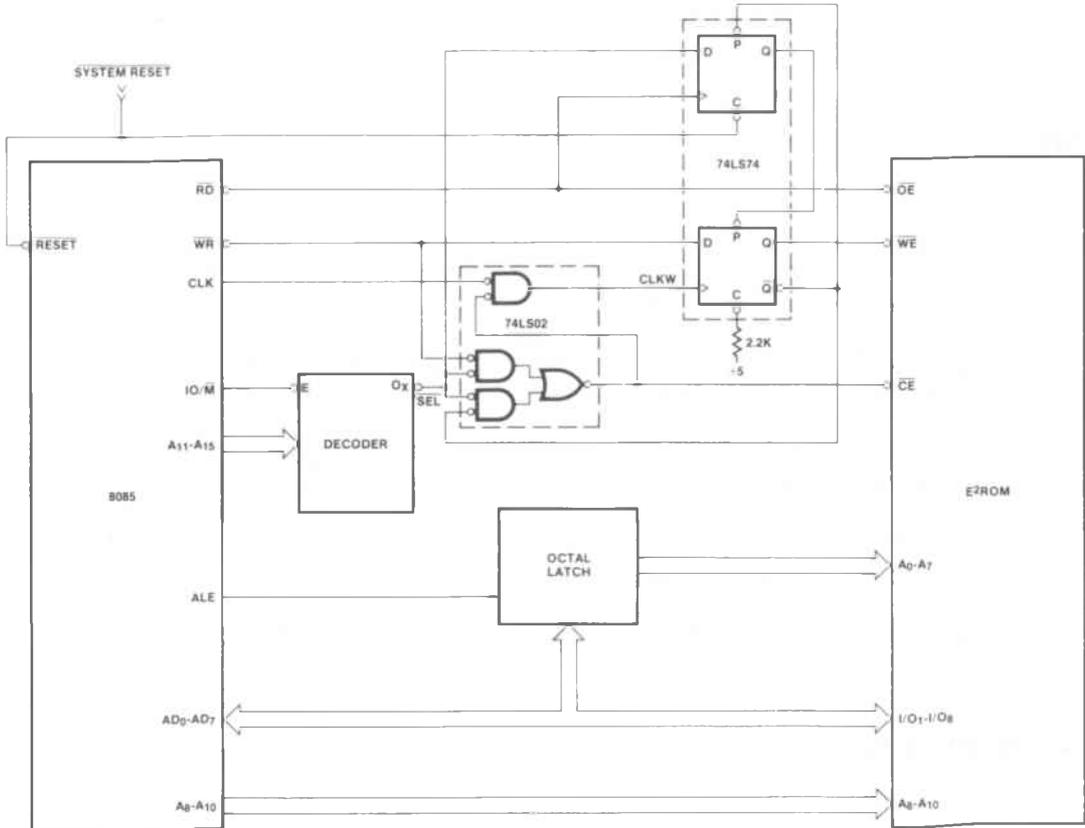


Figure 6. 8085/E<sup>2</sup>ROM Interface

OR a latched E<sup>2</sup>ROM device with no change required to the controlling software or hardware. The following discussion of the operation of the 8085 interface relies on the 8085 timing diagram summary for read and write cycles shown in Figures 7a and 7b respectively.

Initiating a write cycle requires the software control routine as charted in Figure 5. Should the reader desire a specific example, the Z80 code (see Figure 12) is transportable to the 8085.

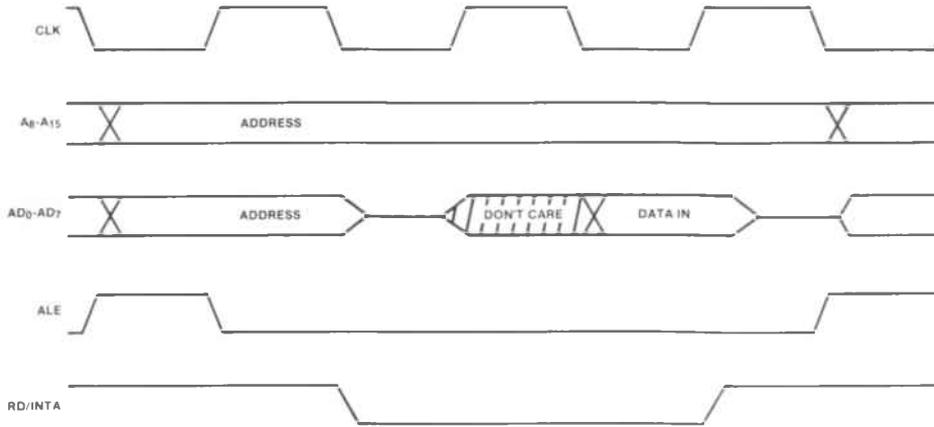


Figure 7a. 8085 Read Timing Summary

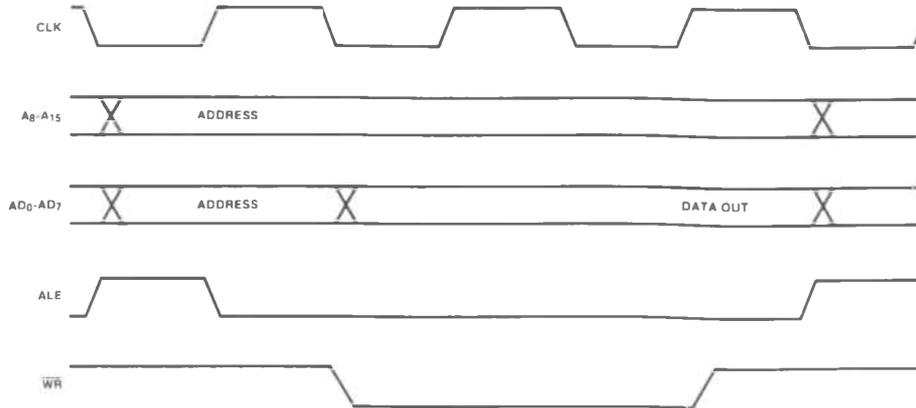


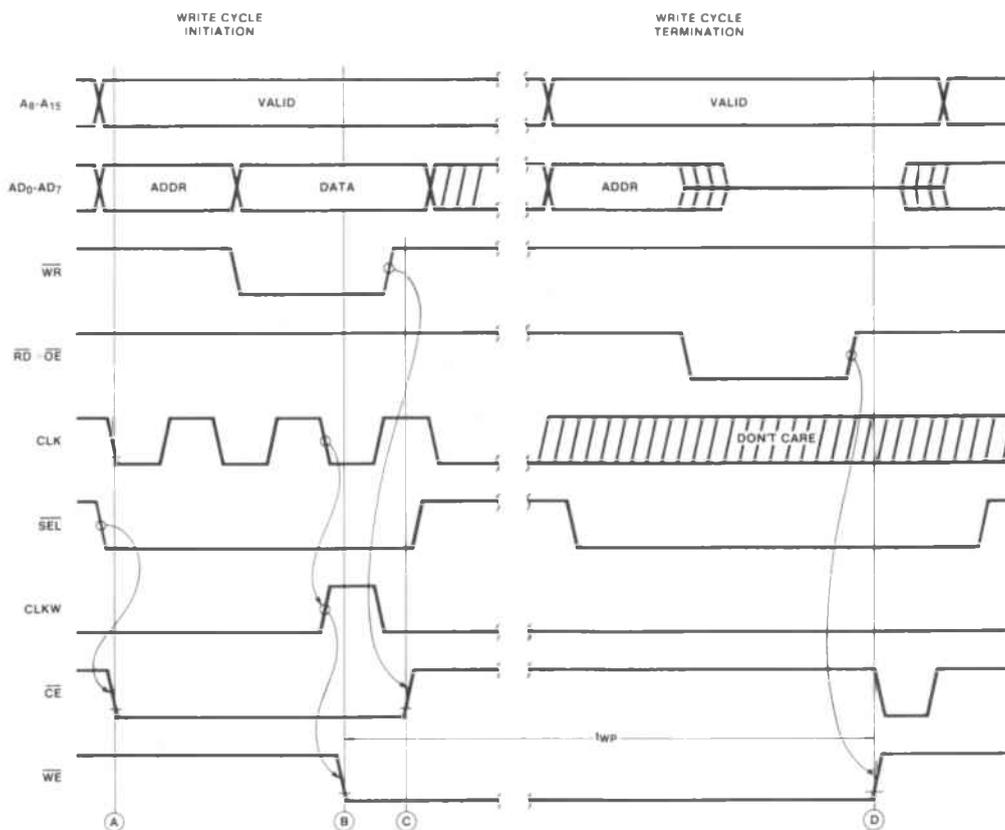
Figure 7b. 8085 Write Timing Summary

The basic write operation waveforms for this interface are shown in Figure 8. The write cycle begins with the addresses becoming valid and being decoded to drive  $\overline{\text{SELECT}}$  active low, in order to drive the  $\overline{\text{CHIP ENABLE}}$  ( $\overline{\text{CE}}$ ) active low at the E<sup>2</sup>ROM device pin (selecting the desired device) (see (A) in Figure 6). An active low level on  $\overline{\text{WR}}$  from the 8085 (indicating a write cycle initiation) allows the  $\overline{\text{WRITE ENABLE}}$  latch of the interface to be clocked by the next falling edge of the 8085 clock output (CLK) (see (B)). Addresses, data, and control inputs to the latched type E<sup>2</sup>ROM are latched in at the falling edge of  $\overline{\text{WRITE ENABLE}}$  ( $\overline{\text{WE}}$ ) — shown as (B) in Figure 8. For the timer type E<sup>2</sup>ROM device, however, data is latched on the rising edge of  $\overline{\text{CHIP ENABLE}}$  ( $\overline{\text{CE}}$ ) — shown as (C) in Figure 8. Note that  $\overline{\text{CE}}$  is held active low for a relatively short period of time, while  $\overline{\text{WRITE ENABLE}}$  ( $\overline{\text{WE}}$ ) is held low

for the entire write time of the E<sup>2</sup>ROM device. In this manner, the waveforms shown in Figure 3 are produced, providing signals compatible with both the latched and timer type devices.

To end the write cycle, the 8085 issues a Read command to the E<sup>2</sup>ROM device. This read cycle enables the Write Reset latch which in turn presets the  $\overline{\text{WRITE ENABLE}}$  latch (shown in Figure 6). The preset to the  $\overline{\text{WE}}$  latch brings  $\overline{\text{WE}}$  to  $V_{IH}$  (see (D) in Figure 8). As indicated in Figure 8, this read cycle does not produce valid data from the E<sup>2</sup>ROM. This read cycle is used merely to terminate the write cycle.

The latched and timer devices respond identically in a read cycle. The 8085 read cycle, shown in Figure 7a, produces the read cycle waveforms shown in Figure 4.



\*A<sub>8</sub>-A<sub>15</sub>: ADDRESS SIGNALS MULTIPLEXED WITH DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 8. Timing Diagram — 8085/E<sup>2</sup>ROM Interface

## Z80 Interface

A sample interface is shown for a Z80 processor (see Figure 9). The timing diagram for write cycle waveforms at this interface is also shown (see Figure 10). The basic circuit is very similar to the 8085 interface, with the differences based on the fact that the Z80 has data valid at both edges of  $\overline{WR}$  (see Figure 11). This simplified timing allows a more simple interface. The CLK output from the processor is not necessary, and  $\overline{WR}$  alone provides timing for the write cycle initiation.

The operation of the circuit is otherwise very similar to the 8085 interface. After addresses are brought valid on the address bus, they are decoded to drive  $\overline{SEL}$  active low, which drives  $\overline{CE}$  active low at the E<sup>2</sup>ROM device pin (see Figure 9, and (A) in Figure 10). At the falling edge of  $\overline{WR}$  (when this device is selected), the  $\overline{WE}$  latch

is clocked, bringing  $\overline{WE}$  active low (see (B) in Figure 10). At this time, the latched type device latches address, data, and control signals, while the timer type device latches address and control signals. At the falling edge of  $\overline{WR}$ , the gating circuitry brings  $\overline{CE}$  high, latching data for the timer type part (see (C) in Figure 10). Within a normal processor cycle, a write cycle has been initiated with timing in accordance with the general approach of Figure 3. Even with additional buffers which may be common in a bus oriented system, this interface can be used with a Z80, Z80A, or Z80B operating with no wait states at up to 6 MHz clock frequency. The individual system designer, of course, must check his own application to ensure satisfaction of applicable setup and hold requirements in the specific system for which the application is intended.

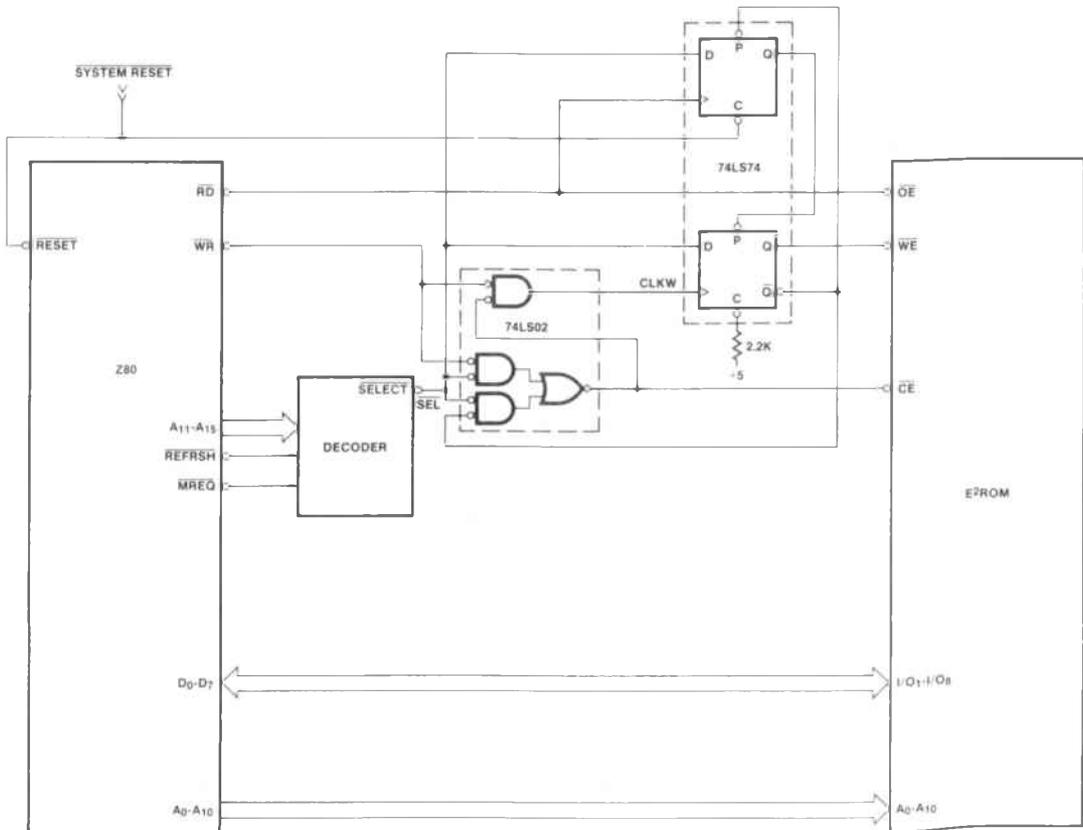


Figure 9. Z80/E<sup>2</sup>ROM Interface

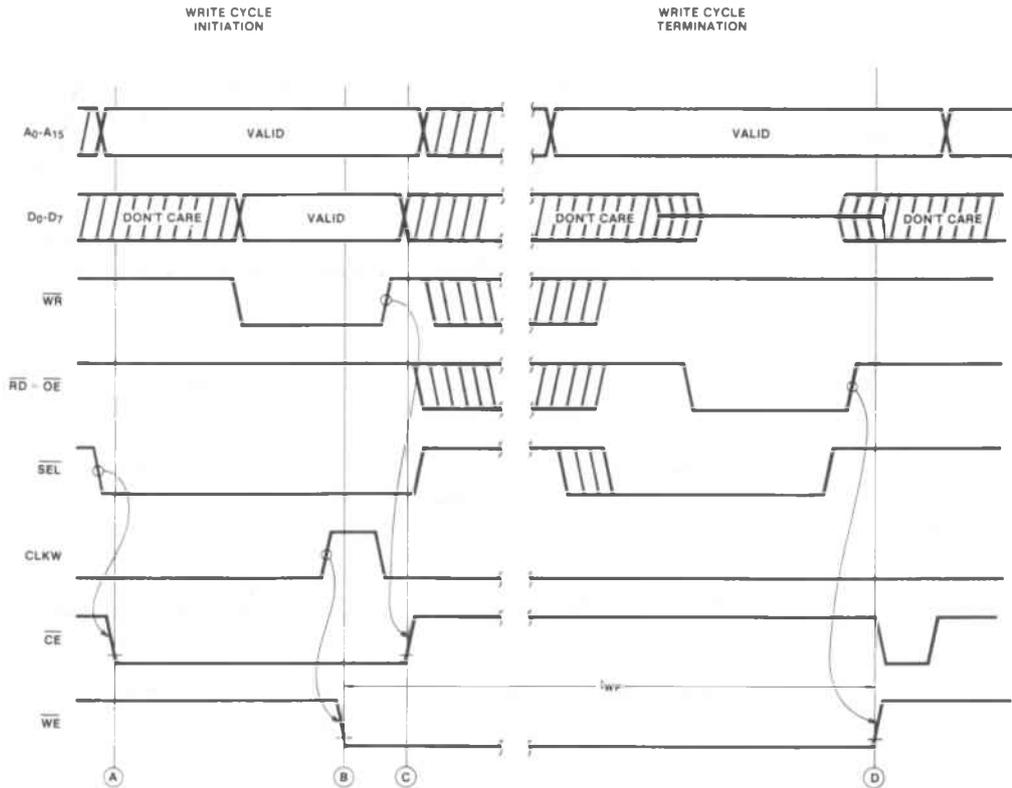


Figure 10. Timing Diagram — E<sup>2</sup>ROM Interface (Write Cycle)

The termination of a write cycle is very straightforward. As shown in the Basic Operation section (see Figure 5), a read operation to the E<sup>2</sup>ROM terminates the write cycle, but does not provide valid data. For the interface operation in write cycle termination, the reader should refer to Figure 10. The addresses are brought valid on the address bus, and are decoded to drive  $\overline{SEL}$  active low (see (A) in Figure 10). The gating circuitry, however, inhibits  $\overline{CE}$ , and  $\overline{CE}$  remains at  $V_{IH}$ . At the rising edge of  $\overline{RD}$ , the flip-flop receives a positive edge trigger, and clocks in the  $\overline{SEL}$  signal to preset the  $\overline{WE}$  latch. At this point,  $\overline{WE}$  is brought high (see (D) in Figure 10), terminating the write cycle. For the remainder

of this processor bus cycle,  $\overline{CE}$  becomes valid for a short while. However,  $\overline{RD}$  is no longer active low, and no valid data is read in this bus cycle. There is no problem with  $t_{WR}$  since the write recovery time occurs during the remaining part of this bus cycle.

Frequently, one may wish to read again from the device, in order to verify data written. This read will be a normal read, following the general waveforms of Figure 4. In a read operation, the interface drives  $\overline{CE}$  active low to select the device, and  $\overline{RD}$  enables the output from the E<sup>2</sup>ROM device.

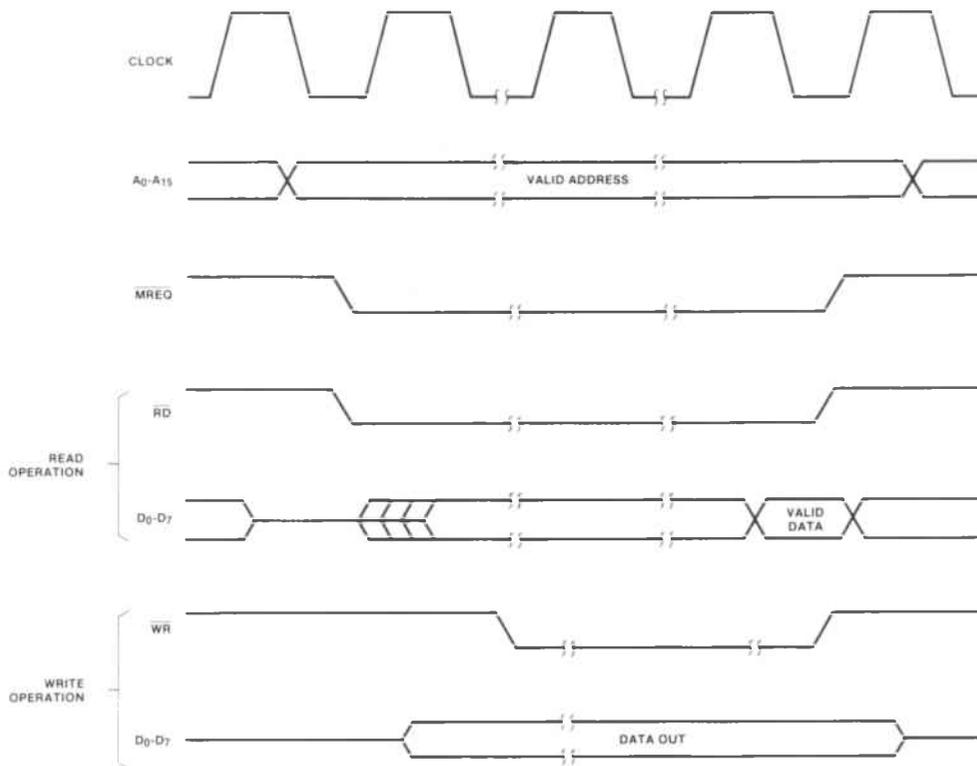


Figure 11. Z80 Read and Write Cycle

```

                                EEWZR80.1
LOC  OBJ CODE M STMT SOURCE STATEMENT                                ASM 5.9

                                175
                                176 ; -----
                                177 ; Z80 EEPROM Write routine.
                                178 ; Incorporates auto-erase and timing
                                179 ; in software.
                                180 ; Accepts: address to be written: Reg DE
                                181 ; Data to be written: Reg B
                                182 ; Uses: A, B, D, E Destroys: A
                                183 ; -----
                                184
009B 3EFF          185 EEWZ: LD      A,0FFH ; FF for erasure.
009D 12            186 LD      (DE), A ; BEGIN ERASE
009E CDAE00       187 CALL   WaitTwp
00A1 1A            188 LD      A, (DE) ; END ERASE
                                189
00A2 78            190 LD      A,B ; Data to be written
00A3 12            191 LD      (DE), A ; BEGIN WRITE
00A4 CDAE00       192 CALL   WaitTwp
00A7 1A            193 LD      A, (DE) ; Read to end Write
00A8 1A            194 LD      A, (DE) ; Read to Verify
00A9 BB            195 CP      B ; Check Verification
00AA C2CB00       196 JP      NZ, ERPI
00AD C9            197 RET
                                198
                                199
                                200 ; -----
                                201 ; Wait routine for EEPROM Byte/ Erase
                                202 ; Uses: Registers A, B,C
                                203 ; Destroys: A,C
                                204 ; -----
00AE 78            205 WaitTwp:LD   A,B
                                206 ; Store B reg in TMP1
00AF 3202C0       207 LD      (TMP1),A
                                208
                                209 ; Set timing constant for Twp.
                                210 ; This 16-bit constant is loaded
                                211 ; into Registers BC, and depends
                                212 ; on the speed of the CPU clock.
00B2 3E07         213 LD      A, 07
00B4 47            214 LD      B,A
00B5 3E06         215 LD      A, 06
00B7 4F            216 LD      C,A
                                217
                                218 ; The following loop performs the wait,
                                219 ; by decrementing BC until the 16-bit
                                220 ; number contained in BC equals zero.
                                221
00BB 3E00         222 LD      A, 00H
00BA 0B            223 More:  DEC   BC
00BB BB            224 CP      B
00BC C2BA00       225 JP      NZ, More
00BF B9            226 CP      C
00C0 C2BA00       227 JP      NZ, More
00C3 3A02C0       228 DUN:  LD      A, (TMP1) ; Restore B Reg
00C6 47            229 LD      B,A
00C7 C9            230 RET

```

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Figure 12. Z80 E<sup>2</sup>ROM Erase/Write Routine

## 8088 Interface

An example interface is shown between an 8088 (operating in minimum mode) and a 16K E<sup>2</sup>ROM (see Figure 14). The reader may note that this is almost identical to the 8085 E<sup>2</sup>ROM interface (see Figure 6), with only minor differences. First, the NOR gates used cannot be a standard TTL or LSTTL device, but must be a CMOS or other high impedance input, so that the CLK signal is not loaded. The CLK signal, as output by the 8284, is used as the clock input to the 8088. The V<sub>OH</sub> level on this signal can fall below specification as a result of a TTL load. A CMOS NOR package, such as a 74C02 or

similar device, eliminates this problem. Since the 74LS74 operates from bussed control and data lines, its requirements are not so stringent, and a 74LS74 will work fine in most applications.

The operation of this circuit is almost identical to the operation of the 8085 interface, as a comparison of the timing diagrams will show (see Figures 7b and 15). Because these processors share similar bus timing, the signals differ only in magnitudes of setup and hold times. All required setup and hold times should be confirmed to the satisfaction of the system designer.

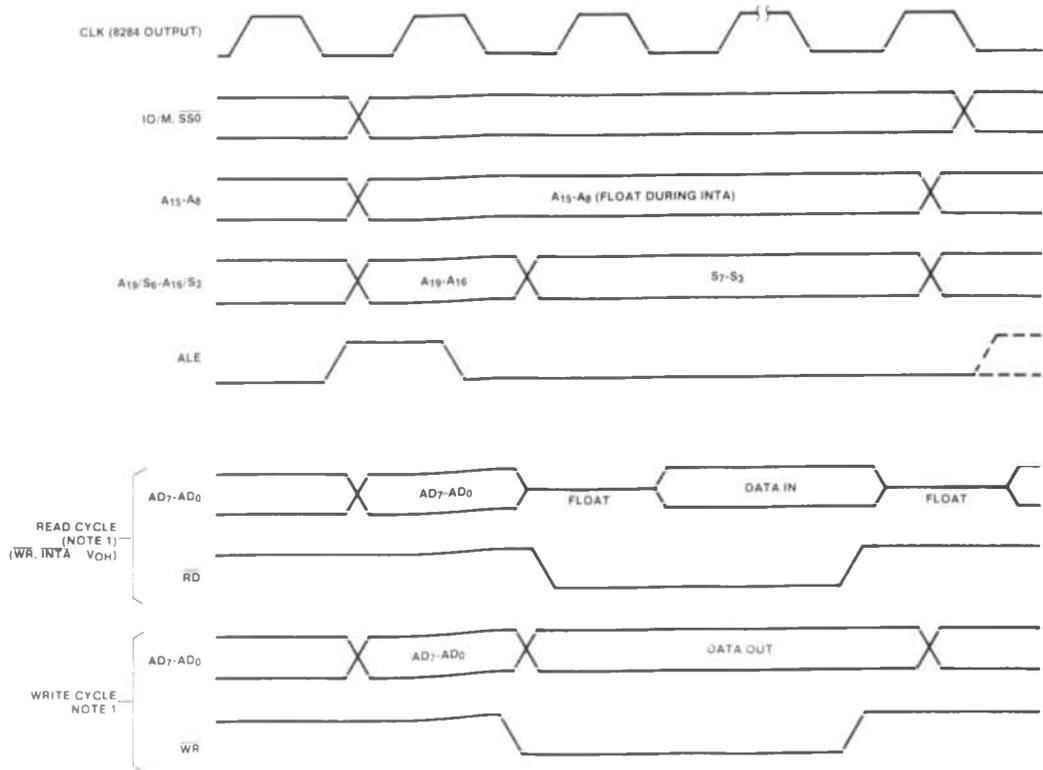


Figure 13. 8088/8086 Bus Timing — Minimum Mode

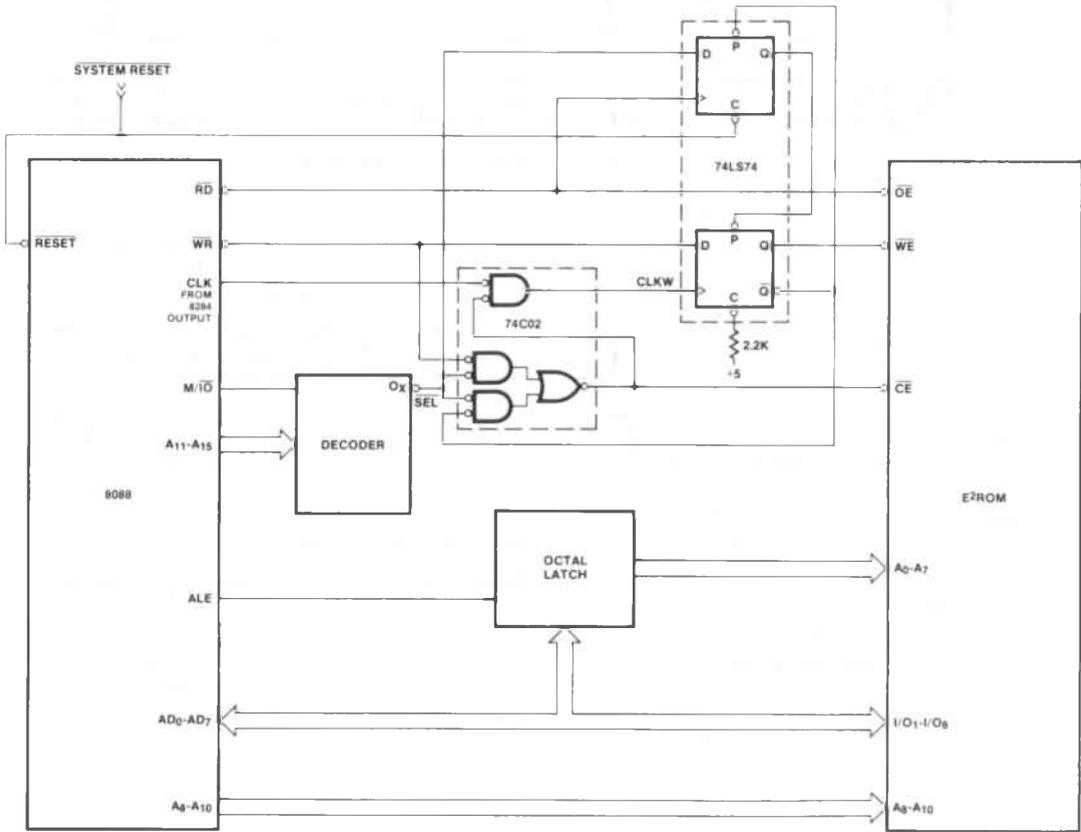
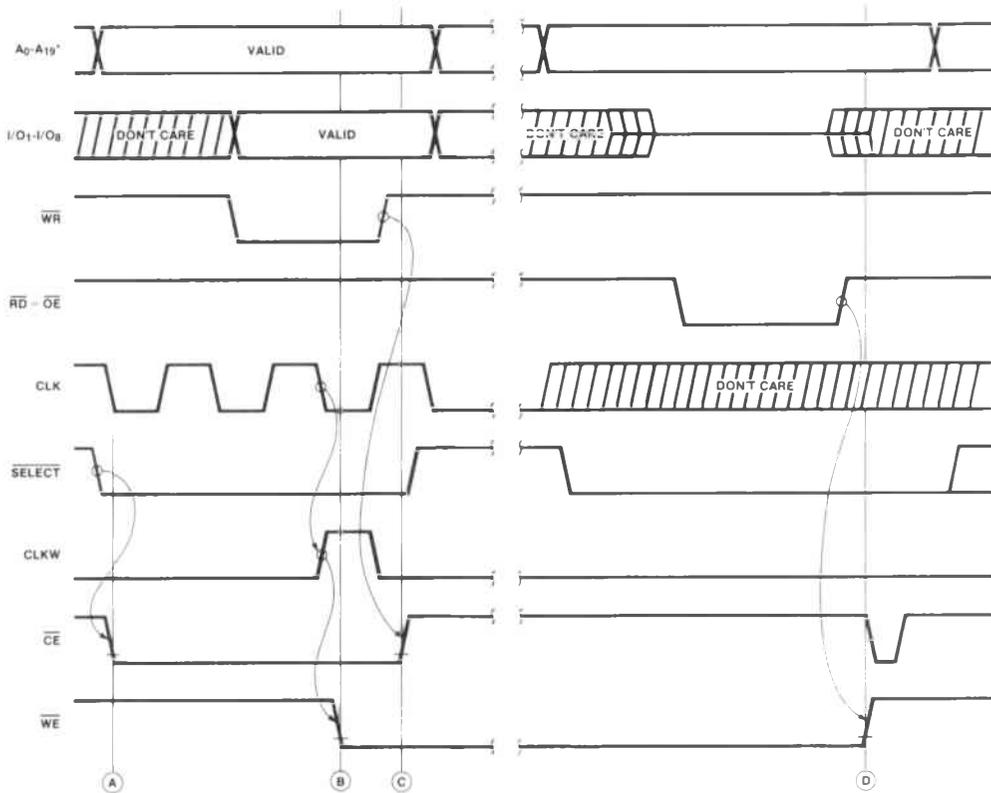


Figure 14. E<sup>2</sup>ROM Interface — 8088 (Minimum Mode)



\*A<sub>0</sub>-A<sub>19</sub>: ADDRESS SIGNALS MULTIPLEXED WITH STATUS AND DATA SIGNALS MUST BE DEMULTIPLEXED USING OCTAL LATCHES.

Figure 15. Timing Diagram — 8088/8086 E<sup>2</sup>ROM Interface

### 8086 Interface

A sample E<sup>2</sup>ROM interface shown for the 8086 (see Figure 16) compares very closely in layout and operation to that for the 8088 (see Figure 14). The 8086 interface accounts for the 16-bit 8086 data bus by latching both bytes of address and implementing a pair of devices to read and write an entire word at a time. E<sup>2</sup>ROM interface control signals are identical to those for the 8088 interface (see Figure 15).





**Memory Products  
Application Note**



**SOFTWARE DOWNLINE  
LOAD USING SEEQ'S  
CMOS EEPROMS**

*June 1987*

APP. NOTES

**seeq**  
Technology, Incorporated

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# Software Downline Load Using SEEQ's CMOS EEPROMS

## Introduction

Non-volatile semiconductor memories have been commercially available for some time but these early devices required multiple power supplies, high voltages and were slow in programming. The RAM-like nature of the new Electrically Erasable Read Only Memory (EEPROM) greatly simplifies their use in all areas of micro-processor based design. The elimination of complex timing and voltage requirements makes it attractive to the designer to incorporate in a design an EEPROM such as SEEQ's 28C64 or 28C256. These EEPROMs are self-supporting and as simple to use as a static random access memory. In addition, because of internal control over the write cycle, they can plug into the standard socket of the 8K by 8 bit and 32K by 8 bit static RAM.

These EEPROMs are true non-volatile memories. Non-volatility is provided in the same way as EPROM. Unlike EPROM they can be written to without prior ultra violet light erasure. The byte-write requirements are identical to that of static RAM except that the EEPROM write cycle, once initiated by normal static RAM timing takes as long as 10ms. Once a write operation begins, the EEPROM is self supporting freeing the processor and all external circuitry for other tasks. This is accomplished through latches, as internal self-timing circuit and wave shaping circuitry. It also generates all necessary high-voltage programming pulses. These features fit well in a RAM environment where 5 volts is the only voltage level available. The read timing cycle of the EEPROM is identical to that of a standard EPROM, RAM or ROM.

The early EEPROMs had small storage capability. For this reason, they were not seriously considered as main program storage medium. Therefore, most of the initial EEPROM applications used the EEPROM for limited data storage, such as calibration parameters and system configuration. The use of the EEPROM for main program storage was obviously reserved for those who could afford the cost and the board space required. The availability of the 28C256 EEPROM along with the reduction in cost of lower density devices has created new interest among design engineers. The EEPROM is now considered a cost effective approach to non-volatile main program storage, either by itself or in combination with ROMs and EPROMs. It will operate with the signals normally applied to a RAM, with the only restriction being the worst-case delay of 10ms after starting a write cycle before accessing data.

## Device Operation

The internal circuitry of the 28C64 and 28C256 EEPROM does not write entered data bytes immediately to the array of memory cells. The bytes first accumulate in a 64 byte page buffer and subsequently transfer to a specific "page" of the array in an independently timed manner. As a result, up to 64 bytes can be written within one 10 ms write cycle to the EEPROM array.

Each byte can be written to any location within the address space boundary of the currently active page. Because the device ignores the row address input after the first byte write, an attempt

to load data bytes beyond this boundary will not affect data elsewhere in the EEPROM array, but will cause the data to be written to the page buffer at a location determined by the lower 6 bits of the address bytes. The procedure to transfer a data byte from the bus to the EEPROM array consists of three steps: the load cycle, the write cycle and the optional data polling.

#### The load cycle

The load cycle is basically a byte-load window ( $t_{BLC}$ ) during which a data byte can be entered into a 64 byte page buffer before the write cycle starts. If an additional data byte is entered within the byte-load window the initial window timer is retriggered and the internal write cycle is prevented from commencing. Taking in consideration the  $t_{WP}$  min and  $t_{BLC}$  min specifications, it will require only 22.4 us to enter a string of 64 bytes into the page buffer. The latest high to low transition of either the Chip Enable signal ( $\overline{CE}$ ) or Write Enable signal ( $\overline{WE}$ ) latches the address bits into the address latches. It also resets the internal page load timer. In order to ensure proper latching and write cycle initiation the  $\overline{WE}$  and the  $\overline{CE}$  signals must meet  $t_{WP}$  min. Upon the earliest low to high transition of either  $\overline{CE}$  or  $\overline{WE}$  the EEPROM latches the data byte, places it in the page buffer and starts the internal page load timer  $t_{BLC}$ .

#### The write cycle

If no data byte has been loaded within the byte-load window the EEPROM terminates its load cycle and initiates its write cycle. During this write cycle, which takes maximum 10 ms, additional load attempts are ignored. The EEPROM, during these 10 ms, is not on the bus and requires no processor service.

The timing diagram on the 28C64 and 28C256 data sheet shows that it can complete a byte load cycle within 170 ns.

$$\text{i.e. } (t_{AS} + t_{WP} + t_{DH}) = 20 + 150 + 0 = 170 \text{ ns.}$$

The remaining 9.99983 ms of the 10 ms write cycle can be used to execute other system tasks. The write cycle is illustrated in Figure 1.

#### DATA polling

During the write cycle, the data bus of the EEPROM exhibits high impedance. The write cycle ends when the internal operations are completed, at which time the EEPROM is immediately available for access. A read command will then present true data at the output port. The maximum write cycle time is 10 ms, but typically it takes less time. The 28C64 and 28C256 have a built-in software feature to take advantage of this shorter write cycle.

When the EEPROM, while still in its write cycle, is read anywhere in its address space, the software feature will present at the EEPROM data bus the ones-complement of the data byte at the last address loaded. For example, data byte 10001101 is read as 01110010. With this feature the end of the write cycle can be detected and data loading can immediately be resumed. As a result the processor waiting time is reduced. This polling procedure is illustrated in Figure 2.

#### Design Considerations

The page mode feature can reduce the overall write-time by a factor equal to the page size. Unfortunately, page sizes as well as timing specifications for EEPROMs vary significantly among manufacturers and may not always match the timing requirements of a particular processor. For instance, a tight byte-load window specification, i.e.  $t_{BLC}$  min to  $t_{BLC}$  max, might not take full advantage of the page load feature. Consequently, the maximum possible data transfer rate is not obtained. To illustrate this, the specifications of the most significant EEPROM parameters, as given by different manufacturers, are shown in Figure 3. The byte-load window specification of the SEEQ 28C64 and 28C256 EEPROMs accommodates a large number of processors.

#### Software examples

Processors with MOVE STRING or LOOP/REPEAT instructions might be able to load a

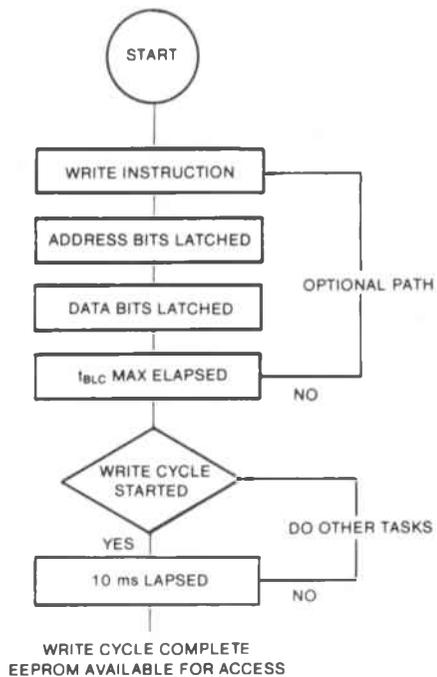


Figure 1. Page Mode EEPROM Write Cycle.

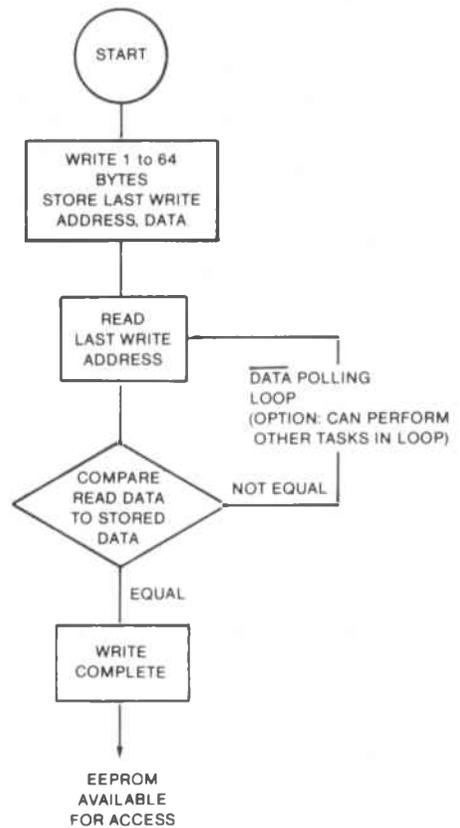


Figure 2. Page Mode Write DATA Polling

## Specification Comparison Table for 64K EEPROM

MANUFACTURER	t <sub>BLC</sub> MIN.	t <sub>BLC</sub> MAX.	t <sub>PLW</sub> MIN.	PAGE SIZE
SEEQ*	200 ns	200us	infinite	64 bytes
#1	3 us	20 us	150 us max.	16 bytes
#2	3 us	100 us	infinite	32 bytes
#3	30 us	100 us	infinite	32 bytes
#4	100 us	500 us	infinite	32 bytes

## Specification Comparison Table for 256K EEPROM

MANUFACTURER	t <sub>BLC</sub> MIN.	t <sub>BLC</sub> MAX.	t <sub>PLW</sub> MIN.	PAGE SIZE
SEEQ*	200 ns	200us	infinite	64 bytes
#1	2 us	100 us	infinite	64 bytes

\*Times are shown for military temperature range devices.

Figure 3.

group of data bytes faster than the EEPROM allows. In that case the data transfer rate of the processor is in conflict with the minimum byte-load-time specification of that EEPROM. The solution to this problem is to emulate the MOVE STRING instruction in assembly code. This approach might cause conflict with the maximum byte-load-time specification.

### Example 1, the t<sub>BLC</sub> min specification

The MOVE BLOCK instruction of the 8086 processor moves data bytes so rapidly that it conflicts with the t<sub>BLC</sub> min of the EEPROM specification from several manufacturers. The following code instructions illustrate this.

```
DESTADD EQU          ES:BYTE PTR [DI]
SRADD EQU           DS:BYTE PTR [SI]
```

```
----- code instructions to
----- cause registers to point
----- to EEPROM address and
----- data source address.
```

```
MOV CX, NLOAD      ; load page size
REP MOVSB DESTADD, SRSADD ; do page load till CX=0
.
.
.
RET
```

The REP MOVSB DESTADD, SRSADD instruction requires 9 clock periods to initiate the byte-move process and 17 clock periods to move each consecutive byte. Consequently, the 8086 driven by a 6 MHz clock can move a byte in 2.83 us. This is in conflict with the minimum value for the t<sub>BLC</sub> specification of the 64K EEPROM made by manufacturers #1, #2, #3 and #4.

Any solution to this problem would reduce the data transfer rate. SEEQ EEPROMs are much faster and, as the table below illustrates, accommodate these data rates easily.

PROCESSOR	CLOCK RATE	DATA RATE
80186	8 MHz	1.0 us /byte
80286	8 MHz	0.5 us /byte

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Figure 4.

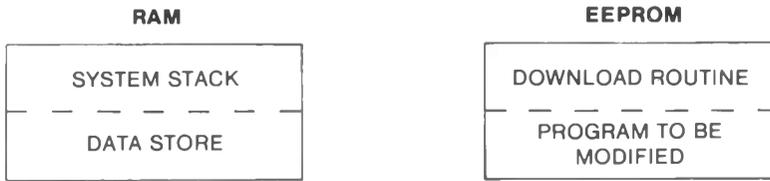


Figure 5.

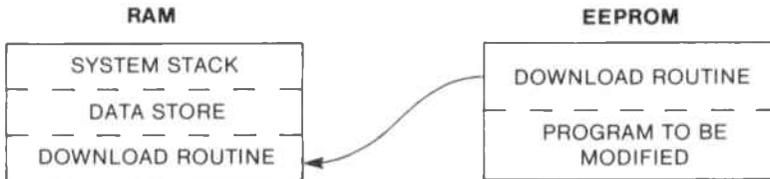


Figure 6.

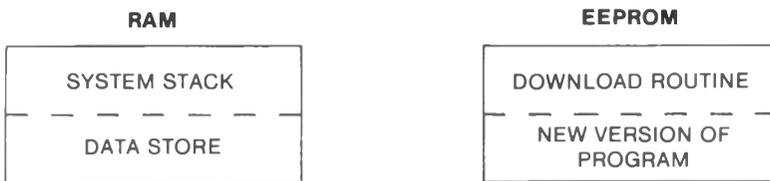


Figure 7.

---

### Example 2, the $t_{BLC}$ max specification

Since the 8051 processor does not have BLOCK MOVE instructions it must emulate a BLOCK MOVE with 13 instructions, each requiring 24 clock periods.

At a clock cycle rate of 12 MHz the data rate is 26  $\mu$ s per byte. This conflicts with the  $t_{BLC}$  max specification of manufacturer #1. Other examples, which violate the specification of manufacturer #1 are shown in the table below.

PROCESSOR	CLOCK RATE	DATA RATE
6805	4 MHz	20 $\mu$ s/byte
6801	4 MHz	36 $\mu$ s/byte

### Example 3, the $t_{PLW}$ max specification

EEPROMS from some manufacturers require that all bytes be loaded into the page within a specified maximum time ( $t_{PLW}$ ). For example, if a processor has a data load rate of 10  $\mu$ s per byte then this value complies with the  $t_{BLC}$  specifications of an EEPROM from manufacturer #1. The  $t_{PLW}$  specification of the same EEPROM is 150  $\mu$ s and therefore, the processor can only load 150/10=15 bytes before the write cycle starts. As a result, the page buffer capacity is not fully utilized, and it takes longer to program the EEPROM.

SEEQ does not specify a limit for  $t_{PLW}$ . The total page-load window time is infinitely long assuming the time between byte loads meets  $t_{BLC}$  max.

### EEPROM Download

The cost of updating software contained in ROM or EPROM in the field is very high. EEPROMs allow the system software to be changed remotely, either through a terminal or a modem link to a main computer. Therefore, the key advantage of the EEPROM is reduced service cost for it allows update of software contained in non-volatile memory, without removing the memory

device from the system. These remote software updates are very attractive for updating system software, self-calibration or changing the system configuration or capabilities. Data load rates in excess of 50,000 bits/sec are possible using the page mode feature of SEEQ's 28C256 and 28C64.

### EEPROM and resident PROM configuration

In the case of an EEPROM and processor resident bootstrap PROM combination, the actual download routine resides in the PROM as shown in Figure 4. The processor can now fetch instructions from the PROM during the EEPROM write cycle.

### All EEPROM configuration

If only EEPROM is used for the program storage and the code to be modified is on a different EEPROM than the one from which the processor is executing then a situation similar to figure 4 exists. A more general approach which allows any EEPROM in the system to be written is the EEPROM and RAM configuration.

### EEPROM and RAM configuration

In the case of the EEPROM and RAM configuration, the following approach is required. The procedure starts with the memory contents as shown in Figure 5.

In the first step both the download routine and the system program are stored in EEPROM. Once the system is instructed that the new version of the program is to be downloaded, the system copies the download routine from EEPROM to the RAM. At this point, the memory contents are as shown in Figure 6.

The processor then jumps to the RAM and executes the download routine and loads the new main program in the EEPROM. Next, the processor jumps to the new main program in EEPROM to continue its normal task, leaving the RAM available for other services. Figure 7 shows the final contents of the memory devices.

---

## Applications

EEPROM is the preferred memory device when variable data storage is required. There are three important characteristics associated with EEPROM

1. Data contained within the EEPROM is retained when power is removed.
2. The EEPROM can store sufficient data to accommodate large lookup tables or computer programs.
3. Data in the EEPROM is easily alterable, remotely or locally.

The list below illustrates that EEPROM applications are as various as they are numerous.

- Data lookup tables.
- Smart cards
- Electronic toys
- Terminal configuration (baud rate, data format, parity)
- Measurement instruments
- Digital positioning machinery
- Boot-up storage
- Calibration data
- Traffic control equipment
- Telemetry
- Navigational reference system
- Music synthesizers
- Signal synthesizers
- Radio and TV program control
- Disc Drive Servo
- Robotics
- Data encryption
- Self-modifying code.

**Power-Up/Down with  
SEEQ's EEPROM**



# **POWER-UP/DOWN WITH SEEQ's EEPROM**

*April 1987*

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**seeq**  
Technology, Incorporated

# Power-Up/Down with SEEQ's EEPROM

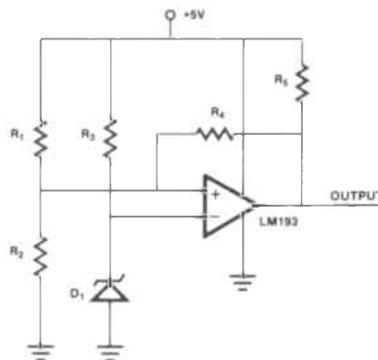
## Introduction

Electrically Erasable programmable Read-Only Memories (E<sup>2</sup>ROMs) are semiconductor devices offering high-density non-volatile random-access data storage. A read operation with E<sup>2</sup> devices is similar to that for an EPROM or static RAM. The write operation, however, requires a millisecond or longer. Previous generations of E<sup>2</sup>ROMs required high-voltage wave-shaped pulses during a write operation. With such strict requirements for the write control signal, the typical E<sup>2</sup> system designer was careful to ensure the correct level of this signal under all conditions, including power-related situations when the system is turned off or on. Only recently has the convenience of E<sup>2</sup>ROM been available in devices which can be written with simple TTL-compatible signals. SEEQ offers such devices in several densities.

With the advent of five-volt E<sup>2</sup>ROMs, non-volatile memory has shown far greater flexibility and ease of implementation. The ease of use allowed by TTL interfaces cannot release the designer from the normal constraint of ensuring reliable operation during power on/off situations. What signals should the interface devices provide when the system is turned off or on (or otherwise loses power)? Under conditions of extreme or repeated brownouts? During times such as these, when V<sub>CC</sub> may be outside of specified limits for correct operation of support logic, this support logic can supply signals to the E<sup>2</sup>ROM which initiate an undesired write cycle. This causes an inadvertent write to a location in the E<sup>2</sup>ROM. In order to ensure system reliability in such situations, it is very important to ensure that inputs (during power up/down conditions) from support devices do not cause inadvertent writes to an E<sup>2</sup>ROM device. A certain amount of the required protection

is included on-board the E<sup>2</sup>ROMs, and is described below. At the system designer's option, system reliability may be enhanced by absolute prevention of false writes.

The purpose of this application note is to provide the system designer with a simple method by which to prevent false writes during power-up and power-down situations. A simple circuit is shown (see Figure 1), its operation is explained, and some useful design considerations are outlined.



- R<sub>1</sub> = 63.4 K $\Omega$  (1% Metal Film)
- R<sub>2</sub> = 71.5 K $\Omega$  (1% Metal Film)
- R<sub>3</sub> = 51 K $\Omega$
- R<sub>4</sub> = 1.5 M $\Omega$  (1% Metal Film)
- R<sub>5</sub> = 10 K $\Omega$
- D<sub>1</sub> = LT1004 - 2.5

Figure 1. E<sup>2</sup>ROM Write-Protection Circuit

The ideas and designs presented in this note are meant to serve as a starting point for the designer, to assist him in accomplishing his goal. The solution given, however, is not the only approach. There are many ways to ensure desired signals to the E<sup>2</sup>ROM during power up/down conditions. The designer is encouraged to tailor his solution to the specific requirements of his application.

## Using E<sup>2</sup>ROM's Built-in Protection

In SEEQ's E<sup>2</sup>ROMs, protection against false writes has been simplified by 3 built-in protection mechanisms on the chip. This protection logic (transparent to the user) does not make writing any less convenient. Table 1 shows the conditions which are required in order to guarantee initiation of a write cycle.  $V_{CC}$  must be within specified limits,  $\overline{CE}$  must be active low, and  $\overline{OE}$  must be  $V_{IH}$ .  $T_{CS}$  (50 ns) before the falling edge of  $\overline{WE}$ . Due to E<sup>2</sup>ROM's protection logic, under certain other conditions, there are modes in which writing is inhibited (see Table 2). First, if  $V_{CC}$  is less than 3.0 V, writing is prevented, regardless of the other input signals. Second,  $\overline{OUTPUT ENABLE}$  ( $\overline{OE}$ ) at  $V_{IL}$  (satisfying  $T_{CS}$ ) inhibits writing. Third, in order to inhibit a write cycle,  $\overline{WE}$  or  $\overline{CE}$  can be held at  $V_{IH}$ .

Several failure modes are prevented by the protection logic described above. For example, if  $V_{CC}$  comes up

with  $\overline{WE}$  already low, this will be interpreted as a continuous low on  $\overline{WE}$  and will not initiate a write cycle, because a falling edge on  $\overline{WE}$  is required AFTER  $V_{CC}$  rises. Inadvertent writes are prevented when  $V_{CC}$  is less than 3.0 V (see Table 2); all that is left to external circuitry is write-protection for  $V_{CC}$  between the levels of 3.0 V (the lowest  $V_{CC}$  level at which the device can write) and the  $V_{CC}$  level at which the support logic issues valid signals.

## External Write-Protection Circuitry

With the protection logic on board the E<sup>2</sup>ROMs, the part can be protected against inadvertent writes in any of several ways. The system designer can ensure that  $\overline{CE}$  is high during power-up and power-down. Alternatively, one can ensure that  $\overline{WE}$  never has a falling edge during power-up or power-down. For example, one could ensure that  $\overline{WE}$  stays at  $V_{IL}$  on power-up until a latch is reset, releasing a pull-down. This would ensure write prevention.

Another manner of write protection has been to bring  $\overline{OE}$  low during power-up and power-down. This inhibits writing (see Table 2), often allows the simplest realization, and is the general path chosen in this application note. Yet the timing and levels of signals provided must be scrutinized here, as well.

Merely inserting a pull-up on  $\overline{OE}$  will tend to pull  $\overline{OE}$  down when  $V_{CC}$  is low, but may not force a valid  $V_{IL}$  level. Inserting a low forward voltage drop diode between the system-wide  $\overline{RESET}$  signal and the E<sup>2</sup>ROM's  $\overline{OE}$  signal may work, but depends on the timing of  $V_{CC}$  and  $\overline{RESET}$ .

The specific form of protection against inadvertent write cycles chosen for this application note, one with more certainty of protecting against inadvertent writes, is to force either  $\overline{OE}$  low ( $V_{IL}$ ) or  $\overline{CE}$  High ( $V_{IH}$ ) during power-up and power-down. Figure 1 shows a circuit that can be used to fulfill this requirement.

**Table 1. Conditions Required to Guarantee Write-Cycle Initiation in E<sup>2</sup>ROMs**

$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$V_{CC}$	All Other Pins
	$V_{IL}$	$V_{IH}$	4.5 -5.5 V	X

**Notes:**

- Active levels shown in above table require  $T_S$  set-up time of 50 ns (see E<sup>2</sup>ROM's data sheet)
- X = TTL Don't Care

**Table 2. Conditions Required to Inhibit Write-Cycle Initiation in E<sup>2</sup>ROMs**

	$\overline{WE}$	$\overline{CE}$	$\overline{OE}$	$V_{CC}$	All Other Pins
Inhibition Mode 1	$V_{IH}$	X	X	X	X
Inhibition Mode 2	X	$V_{IH}$	X	X	X
Inhibition Mode 3	X	X	$V_{IL}$	X	X
Inhibition Mode 4	X	X	X	Under 3.0 V	X

**Notes:**

- Active levels shown in above table require  $T_S$  set-up time of 50 ns (see E<sup>2</sup>ROM's data sheet)
- X = TTL Don't Care

The circuit shown in Figure 1 provides a proper output signal (comparator's output) to prevent false write. During power-up, as is shown in Figure 2A, the output of the comparator is kept low from the time that  $V_{CC}$  is 2.5 V until it reaches 4.8 volts. The output switches to  $V_{IH}$  when  $V_{CC}$  goes above 4.8 volts. During power-down, however, as is shown in Figure 2B, the comparator's output is forced low as soon as  $V_{CC}$  falls below 4.6 V and is kept low until  $V_{CC}$  goes below 2.5 volts. Circuit functionality is not guaranteed below this point.

To prevent inadvertent writes, either  $\overline{OE}$  or  $\overline{CE}$  pin can be used. The first method is by forcing and keeping  $\overline{OE}$  low ( $V_{IL}$ ) when  $V_{CC}$  is below 4.5 volts. This can be done, as is shown in Figure 3A, by connecting comparator's output directly to E<sup>2</sup>ROM's  $\overline{OE}$  pin. As soon as  $V_{CC}$  falls below 4.6 V, the  $\overline{OE}$  is forced low preventing any internal write initiation. This pin is kept low (valid) until  $V_{CC}$  goes below 2.5 volts. Internal protection circuitry protects the part beyond this point (activated when  $V_{CC}$  falls below 3.0 V).

The second method of protecting the part against inadvertent write is by forcing and keeping  $\overline{CE}$  high when  $V_{CC}$  is below 4.5 and above 2.5 volts. This can be done, as is shown in Figure 3B, by NAND gating (74HCT00) the comparator's output with a CS signal. The output of the NAND gate, which is connected to E<sup>2</sup>ROM's  $\overline{CE}$  pin, is controlled by the CS input when  $V_{CC}$  is above 4.6 volts. The other input controls NAND gate's output when  $V_{CC}$  is below 4.6 V (above 2.5 V). Keep in mind that the CS line must be a high true signal and the NAND gate should be a high speed CMOS device.

Either method described above can be used for protection against inadvertent writes. System designers have to determine their need first and based upon that, select one of the above circuits or one of their own.

### Circuit Operation

The circuit shown in Figure 1 is designed to provide a high ( $V_{IH}$ ) output (comparator's output) when  $V_{CC}$  is above 4.8 volts and a low ( $V_{IL}$ ) output when  $V_{CC}$  falls below 4.6 V (above 2.5 V). This is done by using a comparator (LM193 available from National Semiconductor), a temperature compensated voltage reference device (LT1004MH-2.5 available from Linear Technology) and a few resistors. The circuit has been designed to operate over military temperature range.

As it can be seen in Figure 1, the negative input of the comparator is connected to ground through a temperature compensated voltage reference device ( $D_1$ ) and to  $V_{CC}$  through a resistor ( $R_3$ ). As long as

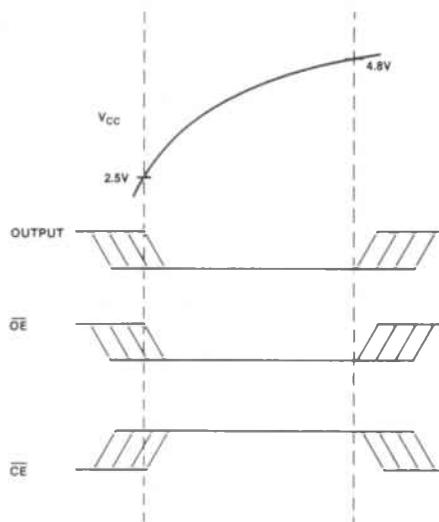


Figure 2A. Timing Diagram—Power-Up Using Either CE or OE Protection

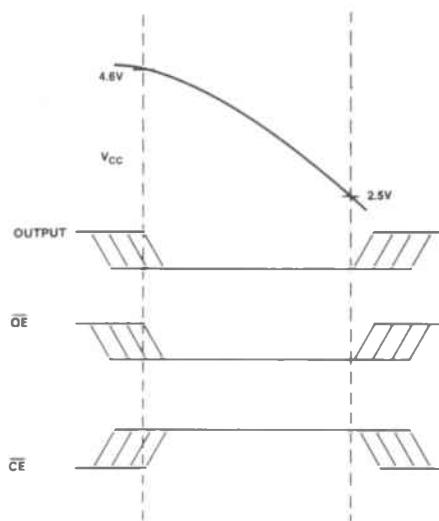


Figure 2B. Timing Diagram—Power-Down Using Either CE or OE Protection

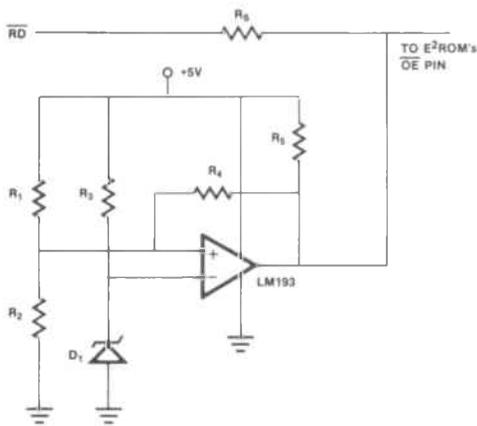


Figure 3A.  $\overline{OE}$  Protection Circuit

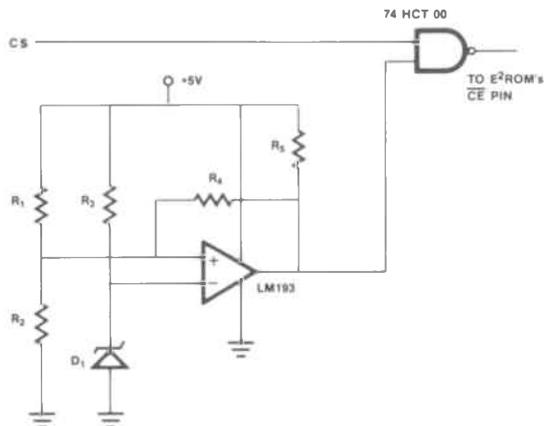


Figure 3B.  $\overline{CE}$  Protection Circuit

$V_{CC}$  is below 2.5 V,  $D_1$  is not conducting (no current flow through it). However, as soon as  $V_{CC}$  goes above 2.5 V and stays there,  $D_1$  conducts providing a 2.5 V reference voltage at the negative input (no current flow into negative input). The resistor ( $R_3$ ) is used to limit the amount of current through  $D_1$ .

The positive input on the other hand, is connected to a voltage divider ( $R_1$  &  $R_2$ ) as well as the output (through  $R_4$ ). The voltage at this input forces the output to go either high ( $V_{IH}$ ) or low ( $V_{IL}$ ). When  $V_{CC}$  is below 4.6 V, the voltage divider causes this input to be below reference voltage with respect to ground forcing the output low. On the other hand, when  $V_{CC}$  goes above 4.8 V, the positive input voltage goes above reference voltage forcing the output high. The output stays high as long as  $V_{CC}$  is above 4.8 volts. The feedback resistor ( $R_4$ ) is used to enforce output voltage on the positive input while  $R_5$  is used as a pull-up resistor. Proper device selection, as is recommended in this Application Note, can insure correct operation of the circuit over military temperature range.

### System Consideration

As was mentioned above, correct circuit operation requires proper device selection. The comparator and temperature compensated voltage reference device ( $D_1$ ) selections are critical. You have to be sure that  $D_1$  provides 2.5 V drop across allowing half a volt safety margin between external protection circuit and the internal one (3.0 V internal power protection). It is suggested to use devices recommended in this Appli-

cation Note. Other circuit elements that can influence circuit operation are the resistors. For correct operation over temperature, it is recommended to use 1% metal film resistor for  $R_1$ ,  $R_2$  and  $R_4$ . The other two can be carbon film resistors.

If  $\overline{CE}$  pin is used for protection, the comparator's output must be NAND gated with a CS signal. Proper gate output is guaranteed if a high speed CMOS gate is used. Also, designers have to make sure that the CS input is a high true signal. However, no NAND gate is needed if  $\overline{OE}$  pin is used to protect the part against false write. Comparator's output can be connected to  $\overline{OE}$  (through  $R_5$ ). A choice of values for  $R_5$  Resistor depends on  $\overline{OE}$  driver (RD line). The  $R_5$  resistor is used to insure a low  $\overline{OE}$  input when  $V_{CC}$  is below 4.6 V (comparator's output is low). If open collector driver is used, the pull-up resistor can replace  $R_5$ .

### Conclusion

It has always been important for a system designer to ensure reliability as his system is turned off and on. Currently, the importance of this area of design is increasing. As the usage of five-volt E<sup>2</sup>ROMs increases, applications are expanding into environments where  $V_{CC}$  may be undependable, power glitches may exist, and in general a system must be more fault-tolerant. With the circuit contained in this application note, the designer can more easily ensure that his system meets applicable specifications and is able to utilize the convenience of E<sup>2</sup>ROMs.



**Memory Products  
Application Note**



**POWER FAIL PROTECTION  
WITH SEEQ'S CMOS  
EEPROMS**

*October 1987*

APP. NOTES

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# Power Fail Protection With Seeq's CMOS EEPROMS

Since 1982, SEEQ Technology Inc. has been producing EEPROMs that can be programmed in-circuit using only a 5 volt supply. All of the high voltages necessary for programming are generated by an on-chip charge pump. Therefore, the external signals required to initiate a write need only be at TTL levels. Unfortunately, these external signals can do unpredictable things during power-up or power-down. If during these power transitions (or during a brown-out), the signals needed to initiate a write to the EEPROM are generated, the system's non-volatile memory may be corrupted.

Several methods of insuring the integrity of a system's data have been proposed, and these methods are often referred to as "write protection". The two major classifications of write-protection are "software write-protection" and "hardware write-protection".

## SOFTWARE WRITE-PROTECTION

Software write-protection involves the use of decoders and latches which need to be written to by the system processor in a specific manner. This "unlock code" sequence must be executed before the EEPROM's control signals can become valid, allowing a write into the EEPROM. These latches and decoders can be on the EEPROM die itself or part of the external circuitry.

The idea is that during power-ups and power-downs the chances of the proper sequence of signals needed to program the EE being generated randomly are very slim. While this is true, there are some limitations to this technique which need to be discussed:

1. Since the unlock code used must be resident somewhere in the system's software, a "run-away" processor could easily execute the unlock sequence, causing false writes. The only way to prevent this from happening

during power-up or power-down is by generating a system reset signal via a low voltage detector. How to prevent this during "normal" processor operations is beyond the scope of this article.

2. What happens if power fails after the system has executed a legitimate unlock sequence to perform a desired write? In this case, the EEPROM is vulnerable to false writes on power down unless some form of low voltage detector disables the EEPROM.
3. If power fails during the EEPROM's internal programming cycle (while new data is actually being written into the memory array), data may be corrupted.

Obviously, software write-protection has some limitations which can only be overcome through the use of external hardware.

## HARDWARE WRITE-PROTECTION

Hardware write-protection is just that; the use of hardware to eliminate false writes. Much of this circuitry is contained onboard the EEPROM itself. Absolute protection against false writes is thus accomplished with the addition of some external hardware (which we have seen is needed even if software write-protection is used). An additional benefit of hardware write-protect is that it is totally transparent to the system's software designer.

For these reasons, the remainder of this article will address the various aspects of hardware protection.

## SEEQ'S ON-CHIP WRITE-PROTECT CIRCUITRY

### A. Bandgap Reference Voltage

Internal to all of SEEQ's CMOS EEPROMS is a bandgap voltage level detector. This detector

disables the EEPROM whenever  $V_{CC}$  is below the WRITE INHIBIT VOLTAGE,  $V_{wi}$ . Characterization data (see figure 1) has shown  $V_{wi}$  to be between 3.85 volts and 4.25 volts over the entire military temperature range. When  $V_{CC}$  is below  $V_{wi}$ , two things will be true:

1. The internal charge pump is disabled, preventing the high voltages which are necessary for programming the EEPROM from being generated. It is impossible for any data to be altered when the charge pump is disabled.
2. The EEPROM's internal oscillator is disabled, forcing the device into a low-power standby mode. This feature results in an orderly shutdown of the device when the system's power fails or is turned off. Also, this feature will save power in an all CMOS system where a low  $V_{CC}$  standby mode is used.

Since SEEQ's EEPROMs are guaranteed to be disabled when  $V_{CC}$  is below 3.85 volts, but TTL signals are only valid when  $V_{CC}$  is above 4.5 volts, some external circuitry must disable the EEPROM (and probably hold the system in reset) while  $V_{CC}$  is between 3.85 volts and 4.5 volts. In a CMOS system, logic signals are valid with  $V_{CC}$  as low as 3.0 volts, which is well below the  $V_{wi}$  threshold of the EEPROM. It would seem then that an external voltage detector

might not be needed in a CMOS system. We will see that this assumption may not be valid.

On power-up, this assumption would be valid because the EEPROM would be idle and disabled until well after the system's bus had settled down into valid logic levels. Unfortunately, if power is lost while the EEPROM is in the midst of an internal programming cycle, the data being programmed may be stored incorrectly.

Of course, with the orderly shutdown feature of SEEQ's EEPROMs, and because the page address is latched into the device upon the first falling edge of WE, only those locations being changed when power was lost might be corrupted. All other locations will remain unchanged. Also, if the system processor was doing a page load on SEEQ's EEPROMs and  $V_{CC}$  was to drop below 3.85 volts before the  $T_{blc}$  Timer timed out (see data sheet), then that programming cycle would never start and no locations would be changed.

Fortunately, there is a way to eliminate the possibility of having the EEPROM in an internal programming cycle, while allowing one final data store, when  $V_{CC}$  fails. This is accomplished by detecting a drop in the raw DC or AC voltage used to power the system (see Figure 2). As long as  $C_f$  is large enough, which is load

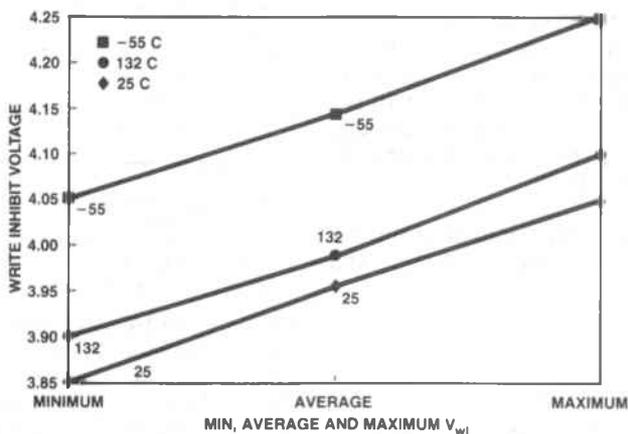


Figure 1. WRITE INHIBIT VOLTAGE—28C256 AND 28C64

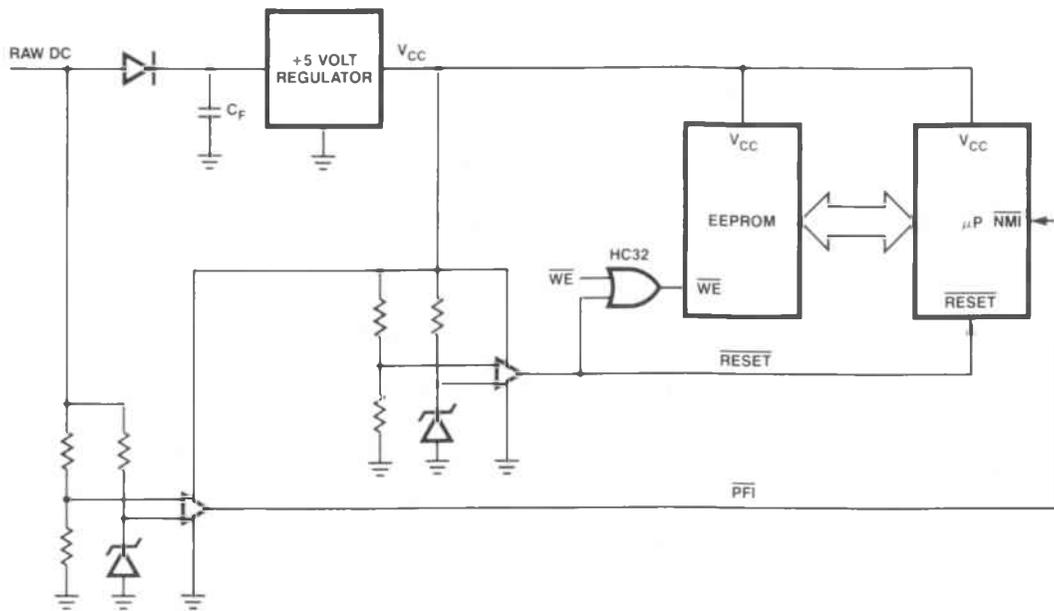


Figure 2.

dependent, a POWER FAILURE IMMINENT (PFI) signal can be generated at least 10 ms before  $V_{CC}$  fails.

This PFI signal can then be used to warn the system processor that there is time for only one more programming cycle before shut-down. Up to 64 bytes of data can be stored in one 10 ms programming cycle and return to its standby mode before  $V_{CC}$  fails. The final store is accomplished, and all data is intact.

Now we must turn our attention to disabling the EEPROM when  $V_{CC}$  is between 3.8 volts and 4.5 volts.

## B. Multiple Control Pins

There are three control signals on SEEQ's EEPROMs, and each signal must be at the proper logic level for a write cycle to begin. Therefore, writes can be inhibited if any of the following input conditions are met:

CE	WE	OE	$V_{CC}$	WRITE MODE
$V_{IH}$	X	X	X	INHIBITED
X	$V_{IH}$	X	X	INHIBITED
X	X	$V_{IL}$	X	INHIBITED
X	X	X	BELOW $V_{WI}$	INHIBITED

1.  $3.8 < V_{wi} < 4.25$
2. X - Don't Care
3. All other inputs are don't care
4. Set-up and hold times on transition are in the specific data sheets for each part.

By using an HCMOS logic gate and a RESET signal (see figure 2) we can force any one of the control lines to a known state to disable the EEPROM when  $V_{CC}$  is below 4.5 volts. We could also use the RESET signal to remove power from the device, which will accomplish the same thing. An HCMOS gate should be used since it will drive the control line to either power rail even with  $V_{CC}$  as low as 3.0 volts.

Why must we have a separate RESET line? Why not use the PFI line to disable the EEPROM? Well, that would allow the EEPROM time to finish an internal programming cycle before  $V_{CC}$  fails, but there are several problems with this approach.

First, during power-up, the unregulated voltage could be above threshold (enabling the EEPROM) some time before  $V_{CC}$  has reached 4.5 volts. This could lead to false writes. Second, if the EEPROM is disabled as soon as an imminent power failure is detected, the system would be unable to initiate any final programming cycles prior to shut-down. This could lead to the loss of valuable data.

From this, we can see that the EEPROM disable signal must be generated from a low voltage detector on the  $V_{CC}$  line. This disable signal

would be the system's normal RESET line (see figure 2).

### EXTERNAL WRITE-PROTECT CIRCUITRY (SEE FIGURE 2)

In this circuit, the RESET signal will disable the EEPROM and hold the  $\mu P$  in RESET any time  $V_{CC}$  is below 4.5 volts (or whatever other threshold is chosen). This will prevent any false writes from occurring during power-up. However, the RESET line will only prevent false writes during power-down if the EEPROM was not already in an internal programming cycle. If this does happen, only those bytes which were being reprogrammed could possibly be corrupted.

The PFI signal will prevent this from happening, as well as allowing the system enough time to save any vital data prior to power failure. By

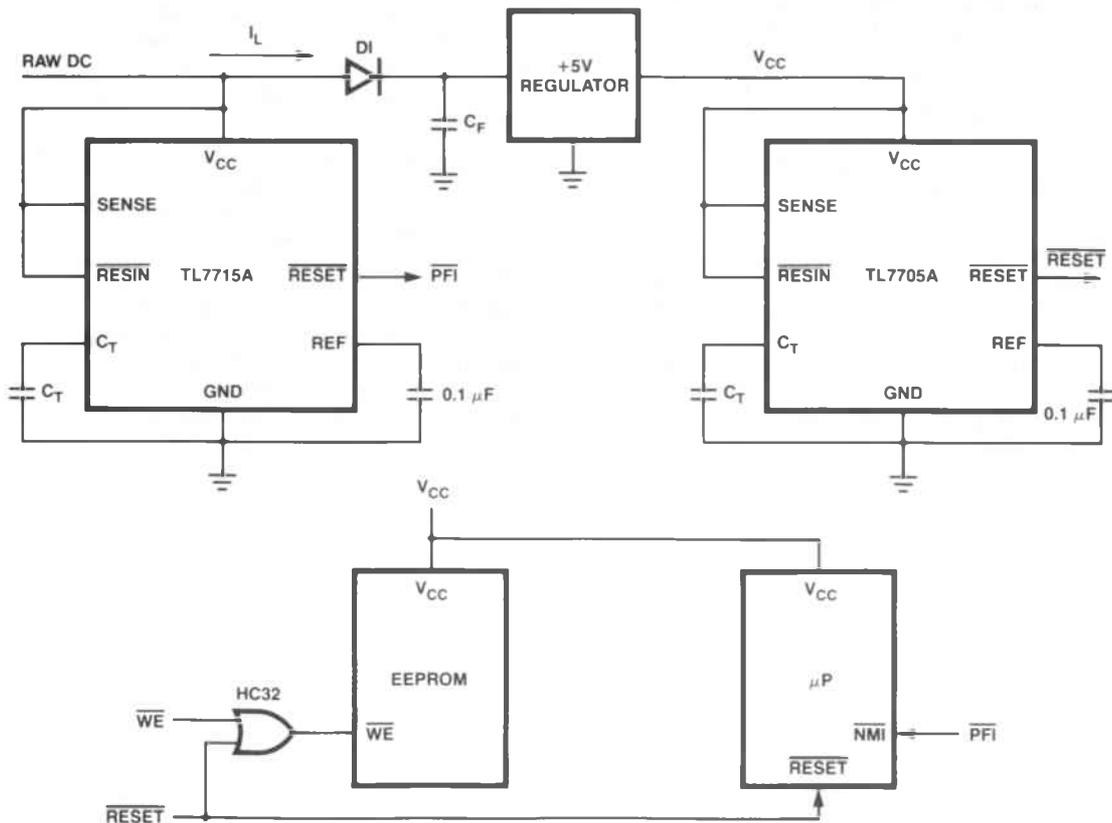


Figure 3.

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making  $C_f$  large enough (which is load dependent), PFI will warn the  $\mu P$  10 ms before  $V_{CC}$  fails. After being warned, the  $\mu P$  can initiate one more programming cycle. The EEPROM will then have enough time to complete its internal programming cycle before it is disabled.

In conclusion, the possibility of false writes can be totally eliminated if the system makes use of a RESET signal and a PFI signal in combination with SEEQ's on-board write-protection circuitry.

## A MONOLITHIC SOLUTION (SEE FIGURE 3)

An alternative to using op-amps and discrete components to produce the PFI and RESET signals can be seen in Figure 3. This circuit makes use of a monolithic supply voltage supervisor family from TEXAS INSTRUMENTS. These devices are useful to detect power-up, power-down, and brown-outs. In addition,  $C_f$  can be chosen to determine how long the RESET signals will remain active after  $V_{CC}$  is above threshold, which guarantees proper system initialization on power-up. The reader should refer to T.I.'s data sheet for details.

In this example, a TL7715 is used to produce PFI while a TL7705 is used to generate the RESET signal. This arrangement ensures that the EEPROM is disabled anytime  $V_{CC}$  is below 4.5 volts, and the PFI warning is issued anytime the raw DC powering the system falls below 13.2 volts. (See TL7705 and TL7715 data sheets for details).

Lets assume that:

- power is lost abruptly
- $V_f$  of D1 is 0.7 volts
- The drop-out voltage of the regulator is 2.0 volts

Then we can see that the voltage across  $C_f$  must take at least 10 ms to drop from 12.5 volts to 7.0 volts at the given load,  $I_L$ . ( $13.2 - 0.7 = 12.5$  and  $5.0 + 2.0 = 7.0$ ). Since  $I_L = C_f dv/dt$  and  $dv = 5.5$  volts,  $dt = 10ms$ , we have this relationship:  $I_L = 550 C_f$ .

In other words, if  $I_L$  is 550 mA, then  $C_f$  must be 1000  $\mu F$  for proper operation of the PFI protection.

## CONCLUSION

Designers must be careful to avoid false writes to a system's EEPROM during power-up, power-down, and brown-outs. This is especially true in CMOS systems where "brown-outs" are often entered purposely to achieve low  $V_{CC}$ /low power standby states.

We have seen that to completely eliminate the possibility of false writes, the system must monitor the voltages on both sides of the  $V_{CC}$  regulator. This is true whether software or hardware write-protection is used.

SEEQ Technology has incorporated all of the on-chip hardware write-protection needed to design a trouble-free system using EEPROMS. In addition, this form of write-protection is completely transparent to the system, making the software interface more convenient.

**Memory Products  
Application Note**



**24**

***EEPROM AS A  
SUBSTITUTE FOR  
BUBBLE MEMORY***

*October 1987*

APP. NOTES

**seeq**

*Technology, Incorporated*

As more systems designers are dropping bubbles, EEPROM—based designs are rapidly increasing. In the early to mid 80's, we were told bubbles would take over mass storage designs. Surely bubbles were the design of the future for core memories and even to replace disc memories. As many of these dreams fade, let us consider some of the pro's and con's of each technology.

Common design considerations include density, power consumption, weight, access time, data rate, and environmental susceptibility.

Density is certainly one issue that gets a lot of discussion. Commonly available 4 megabit bubble packs are approximately 1.25 cubic inches for the basic block. SEEQ Technology's 256K PLCC package has a volume of approximately .0125 cubic inches or 1% of the volume of the bubble pack. Therefore, an equivalent 4 megabit EE memory using 16 256Kbit devices has less than 20% of the volume of the bubble memory. Mounting of either device was not taken into consideration; neither was the volume of the required support chips. The EEPROMs would take more area mounted than was implied strictly with a volume specification. Spacing between packages could increase total volume, although the ratio between EE and bubble would still be substantial.

Additionally, the high profile of a bubble memory device would greatly increase overall board volume as boards cannot be spaced closer together than the tallest component height. Decoding of a 4 megabit EEPROM array can be done with a simple one-of-sixteen decoder such as the 74LS154. In comparison, that 1.25 cubic inch bubble pack required a series of controllers, coil drivers, current drivers, etc. In the final analysis, semiconductor EEPROM memory will occupy a fraction of the space of bubble memories.

Access time is the time from the issuance of the valid address or name of a file, datablock, word or byte until the first full size segment of data is available. A full size segment would be the first bit of a serial data stream or the first full byte or word in a parallel data bank. Common 4 megabit bubble memories today have average random access times on the order of 50 to 90 milliseconds. Some of the new small size modules have average access times less than 10ms, but specify maximums above 500ms. SEEQ Technology's 28C256 has a maximum access time of 250 nanoseconds. Comparing the two technologies, bubble memory's average access time is 200,000 times longer than the EEPROMs worst case; the EEPROMs could deliver 200,000 bytes of data while the bubble memory is accessing the first bit.

**FIGURE 1  
COMPARISON CHART  
BUBBLES TO EEPROMs**

	<b>BUBBLE</b>	<b>EEPROM</b>	<b>RATIO</b>	<b>REMARKS</b>
Power Consumption	5	.5	10/1	Considerable current would be drawn by bubble memory support circuitry
Access Time in microseconds	50,000	.25	200,000/1	
Average Data Rate (Read) K Bits/Second	125	32,000	1/256	
Data Rate (Write) K Bits/Second	125	800	1/6.5	4 Megabit bubble and sixteen 256K EEPROMs/ shown in fig. 3
Weight (Grams)	75	5	15/1	
1 Megabit Volume (Unit only) Cubic Inches	1.25	.2	6/1	Does not include bubble support chips

Weight is one area that seldom becomes an issue in most designs but does come up on occasion. Once again, the comparison is not straightforward. Basic bubble memory devices commonly have weights in the vicinity of 75 grams per 1 megabit device. This, of course, does not take the weight of support circuitry into consideration. The equivalent EEPROM bank of four 256K devices would have an approximate weight of 5 grams. With the bubble memory support devices also taken into consideration, the ratio would significantly surpass this 15 to 1 ratio.

Power consumption almost always warrants some consideration. Four megabit bubbles have power supply requirements around 4 watts typical and greater than 5 watts maximum. Sixteen (16) of the 256K type EEPROMs and a one-of-sixteen decoder under worst case conditions would draw less than 100 ma at 5 volts. This would be one-half watt or about 10 percent of the power of a bubble memory. While the sixteen 256K's only require a single decoding chip for support, the bubble requires numerous support chips. This support draws power too. To get a realistic feel for bubble power consumption, it becomes necessary to examine then at the board level where the host of necessary support devices are installed.

The boards considered for comparison were not expandable, that is to say they were fully stuffed, 4 megabit boards. Power consumption on these boards runs between 10 and 20 watts. Additionally, there were multiple power supplies required, not the single 5 volt supply required by the EEPROMs.

Data rate is the speed at which the data can be continuously delivered to the addressing device. In this area the bubble is specified at maximum (burst) and average. Burst data rates can be fast as 200,000 bits per second. Average data rates can be on the order of 125,000 bits per second. Making the EE comparison, data rates are the same as access times, and therefore 250 nanoseconds per byte (8 bits). Putting this in perspective, after the bubble has taken 88 milliseconds to get started (initial access time), while the bubble is fetching 256 bytes the EEPROM could deliver 65,536 bytes.

Data rate does not imply direction. This is to say that data rate does not apply only to reads of data but also to data writes. For a bubble memory, read and write data rates are equal, but the rates differ when EEPROMs are used. Read data rates were

discussed above. Write data rates in EEPROMs are a bit more complex. In high density EEPROMs, byte write times and page write times are the same. A "page" is 64 consecutive bytes of data. This page of data can be loaded as fast as 350 nanoseconds per byte, thus a page load would take 22.4 microseconds. After this time, a maximum of 10 milliseconds is required for the write cycle to complete.

The microprocessor's write data process must halt during this 10 milliseconds until the device is again ready to load another page and begin the 10 millisecond write sequence again. This would imply a write data rate of 350 nanoseconds per byte "burst-mode" with a maximum of 64 bytes or an over all rate of 6400 bytes per second. This 6400 bytes per second rate is comprised of one hundred 10 millisecond write sequences of 64 bytes. While 6400 bytes per second (this would be 51.2K bits per second) is about half the speed of the bubble's write data rate it can be improved many fold for systems using multiple EE Devices.

In the case of medium to large arrays, which would be the case in mass storage applications, the common approach is to decode chip selects from the high-order address inputs (see figures 2 and 3). But positioning the chip select decoder in the address space immediately above the page address inputs would allow each consecutive device to store the next logical page.

Applying this approach to a 4 megabit array, system addresses  $A_0$  to  $A_5$  would go directly to  $A_0$  to  $A_5$  inputs of the EEPROMs. For an array of 16  $E^2$  devices, requiring 4 address inputs to select the 16 devices, system addresses  $A_6$  -  $A_9$  would go to a 4 to 16 decoder network, providing the 16 chip selects required. System address  $A_{10}$  would go to address  $A_6$ , system address  $A_{11}$  to address  $A_7$ , continuing thru system address  $A_{18}$  to address  $A_{14}$ . The 10 msec write cycle would continue independently in each device while the system was continuing to write logically consecutive pages in the other devices. This makes the page size 1024 bytes, thus the system should stop writing and wait for the write cycle to complete after 1024 sequential bytes had been written.

For a 4 megabit array (sixteen 256K EEPROMs), this design approach would produce a data rate in write mode of greater than 100,000 bytes per second or  $6\frac{1}{2}$  times the bubble's write data rate.

Temperature sensitivity is often a major design consideration. This is very true for military, industrial and space applications. These designs often require operation or at least storage down to  $-55$  degree C and as high as  $125$  degree C. Bubble memories have problems at temperature extremes and often specify their minimum temperature for operation a few degrees above  $0$  C. This does not comply with standard commercial grade temperature ranges and falls far short of either military or industrial grade temperature ranges. Similar problems exist at high temperature. We commonly see maximum temperature for operation between  $+30$  degree C and  $+50$  degree C. Even

the  $+50$  degree C falls for short of the commercial temperature specification of  $+70$  degree C. Needless to say both military and industrial temperature ranges are completely missed. EEPROMs operate over the entire commercial, industrial and military temperature ranges.

Clearly, EEPROMs share the intrinsic non-volatility of bubble memories without the disadvantages in speed, power consumption and temperature range. Figure 1 compares the important attributes of the two technologies. Complete technical information is contained in Seeq's 28C256 datasheet.

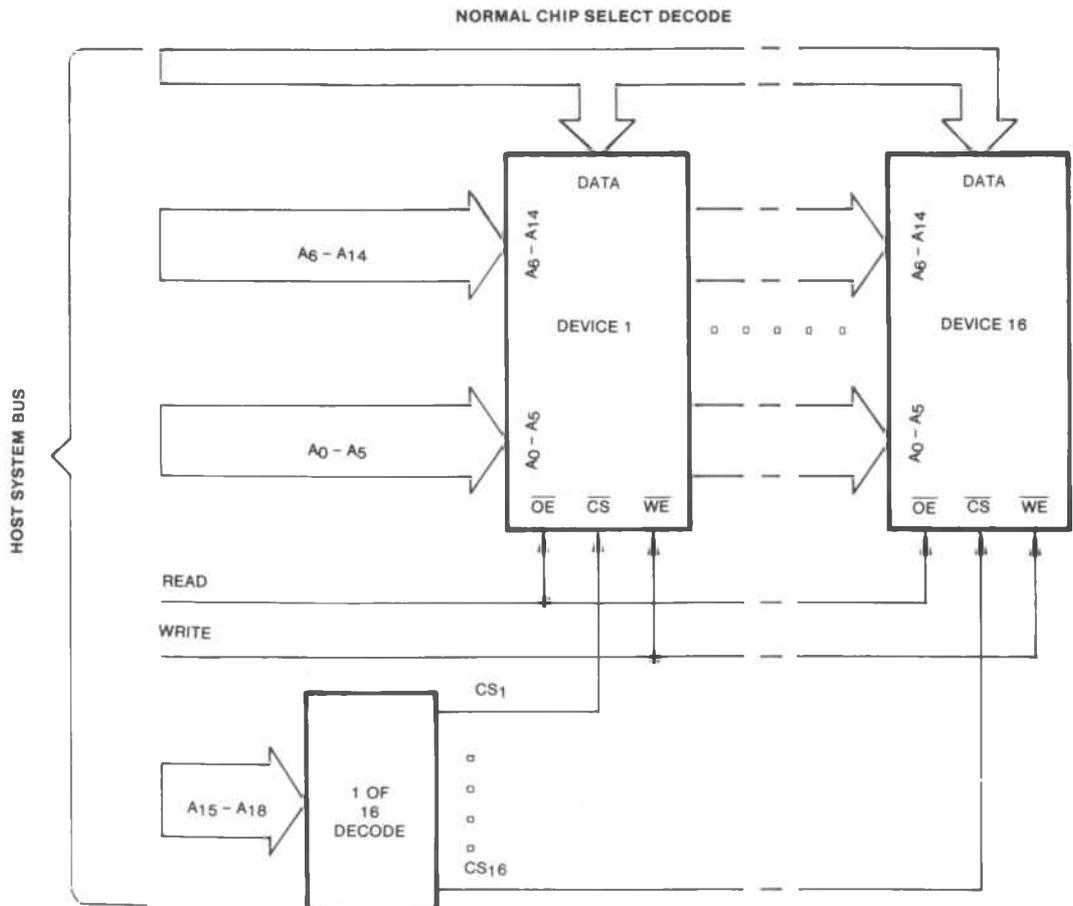


Figure 2.

DECODING METHOD TO ENHANCE  
WRITE CYCLE DATA RATE

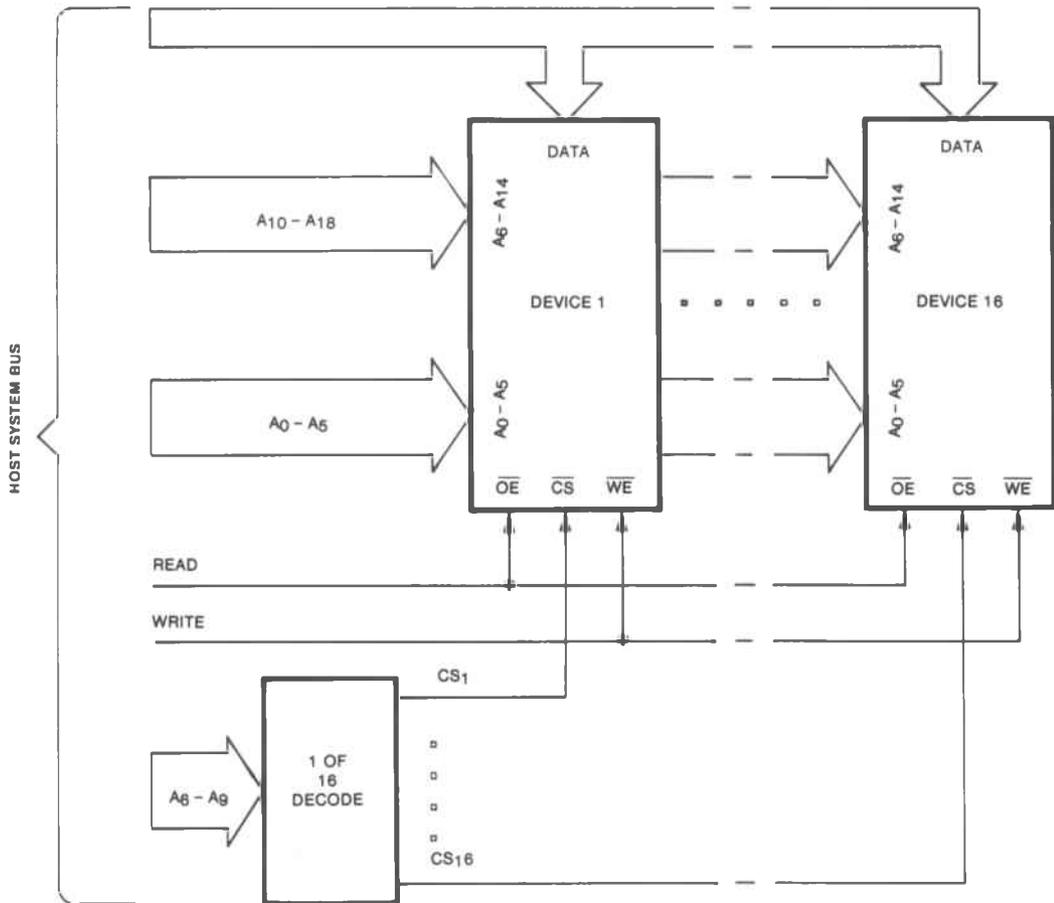
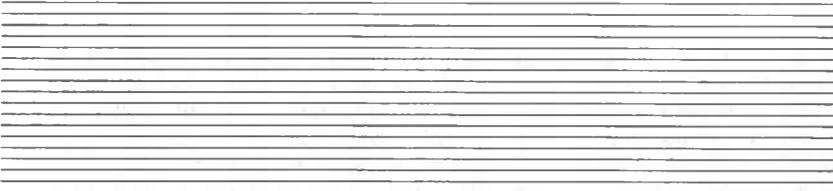


Figure 3.



**Memory Products  
Application Note**



**27**

**USING HIGH SPEED  
CMOS EEPROMS WITH  
HIGH PERFORMANCE  
MICROPROCESSORS.**

*October 1987*

APP. NOTES

**seeq**

*Technology, Incorporated*

# Using High Speed CMOS EEPROMs with High Performance Microprocessors.

Satisfying ever increasing demands on microprocessor throughput can be achieved in several ways, the simplest of which is to increase system clock frequency. However, this technique yields higher performance only if the remainder of the system is capable of operating at the higher rate. Memory devices on the system must be able to respond to the accelerated transfer rate to avoid insertion of wait states. Speeding up clock rates without decreasing access times will generally cause the microprocessor to wait faster. The 38C16 and 38C32 high speed CMOS EEPROMs from SEEQ technology are designed to satisfy the performance requirements of high performance microprocessors.

The 38C16 and 38C32 are 2K x 8 and 4K x 8 bit CMOS EEPROMs manufactured using SEEQ's advanced 1.25 micron CMOS process. Seeq's

proprietary oxynitride process and patented differential 'Q' cell design give the parts fast access times and high endurance. The 38C16/32 are ideal for high speed applications requiring non-volatility and in-system reprogrammability. Both commercial and military temperature range products are available.

## Device Features:

### Read Operation:

38C16 and 38C32 are available in access times ranging from 35 ns to 70 ns. The operational mode table is shown in Table 1. Read operation for the devices is similar to any standard memory device. Chip enable access times are faster than address access times (see data sheet) which can be a significant advantage in high speed microprocessor designs.

**38C16/32 OPERATIONAL MODES**

MODE PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	D <sub>OUT</sub>
Standby	$V_{IH}$	X	X	HI Z
Write	$V_{IL}$	$V_{IH}$	$V_{IL}$	D <sub>IN</sub>
Write Inhibit	X	X	$V_{IH}$	HI Z/D <sub>OUT</sub>
	$V_{IH}$	X	X	HI Z
	X	$V_{IL}$	$V_{IH}$	HI Z/D <sub>OUT</sub>
	$V_{IL}$	$V_{IL}$	$V_{IL}$	No Operation (HI Z)

X: Any TTL level

Table 1.

### Write Operation:

The write operation is similar to static RAM. Because of the fast address and data latches, the write data latch cycle is as fast as a read cycle. The address is latched on the falling edge of  $\overline{CE}$  or  $\overline{WE}$  whichever occurs last and data is latched on the rising edge of  $\overline{CE}$  or  $\overline{WE}$  whichever occurs first. After the data is latched the built-in timer completes the non-volatile write cycle within a maximum time of 5 ms. A typical device has a write cycle time faster than the maximum specified 5 ms. The 38C16/32 feature DATA polling to enable the user to optimize write time. During the internal write cycle, the complement of bit 7 of the data byte written is presented at the output I/O, when a read is performed. Once the write cycle is completed, true data is presented at the outputs. A software 'polling' routine (see fig. 1) can be used to determine write cycle completion. The data bit 7 polling cycle specifications are the same as a read operation. During data polling, the addresses are a don't care.

### Write data protection:

38C16 and 38C32 provide protection against false write during powerup/down using on chip circuitry. Writing is prevented under any one of the following conditions:

1. When  $V_{CC}$  is below write inhibit voltage  $V_{WI}$ .
2. A high to low write enable transition has not occurred when  $V_{CC}$  is between  $V_{WI}$  and  $V_{CC}$  min.
3.  $\overline{WE}$ ,  $\overline{CE}$  or  $\overline{OE}$  are in TTL logical states other than those specified for byte write in the mode table (Table 1).

38C16 and 38C32 feature an on-board bandgap voltage level detector. The detector disables the EEPROM write circuitry whenever  $V_{CC}$  falls below write inhibit voltage  $V_{WI}$ . The internal charge pump (voltage multiplier) is disabled, preventing the high voltages which are necessary for the programming cycle from being generated. It is impossible for data corruption to occur when the charge pump is disabled. Seeq's EEPROMs are guaranteed to be write disabled when  $V_{CC}$  falls below write inhibit voltage  $V_{WI}$ .  $V_{WI}$  is between 3.8 to 4.25 V over the military temperature range.

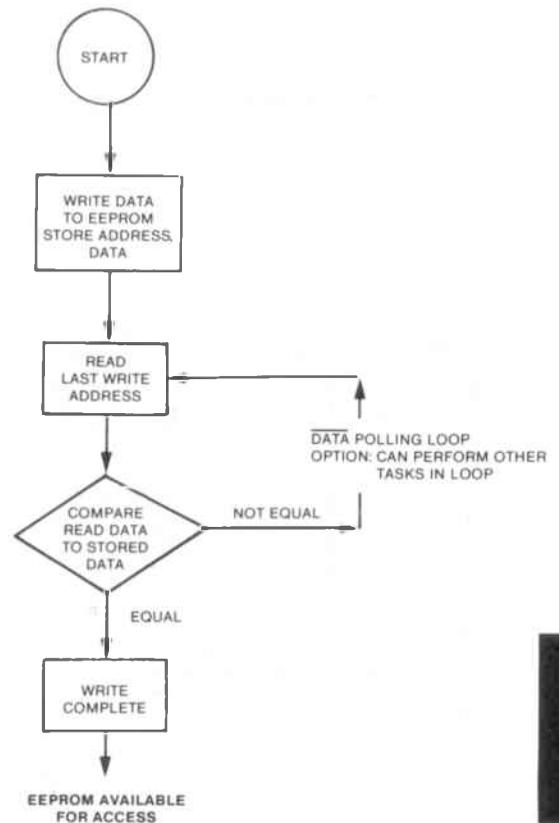


Figure 1. BYTE WRITE WITH DATA POLLING.

Since present day systems employ a mixmatch of both TTL and CMOS components, it is recommended that external hardware write protection circuitry be used in addition to the on-board protection circuitry just described. This is needed to eliminate false writes when  $V_{CC}$  is between 3.8 to 4.5 V (see Application Note 11). Absolute protection from false writes can be thus achieved while having the added benefit of being totally transparent to the system software.

### System Interface examples:

MIL-STD-1750A is the U.S. Air Force's instruction set for 16-bit microprocessors embedded in avionic weapon systems. This standard is also used by the Navy, Army and NATO. Typical 1750A applications involve real-time avionic applications in systems incorporated into aircraft, missiles and even ships or ground vehicles. The standard specifies the microprocessor architecture and instruction set. Also defined are two memory addressing modes, a standard mode of

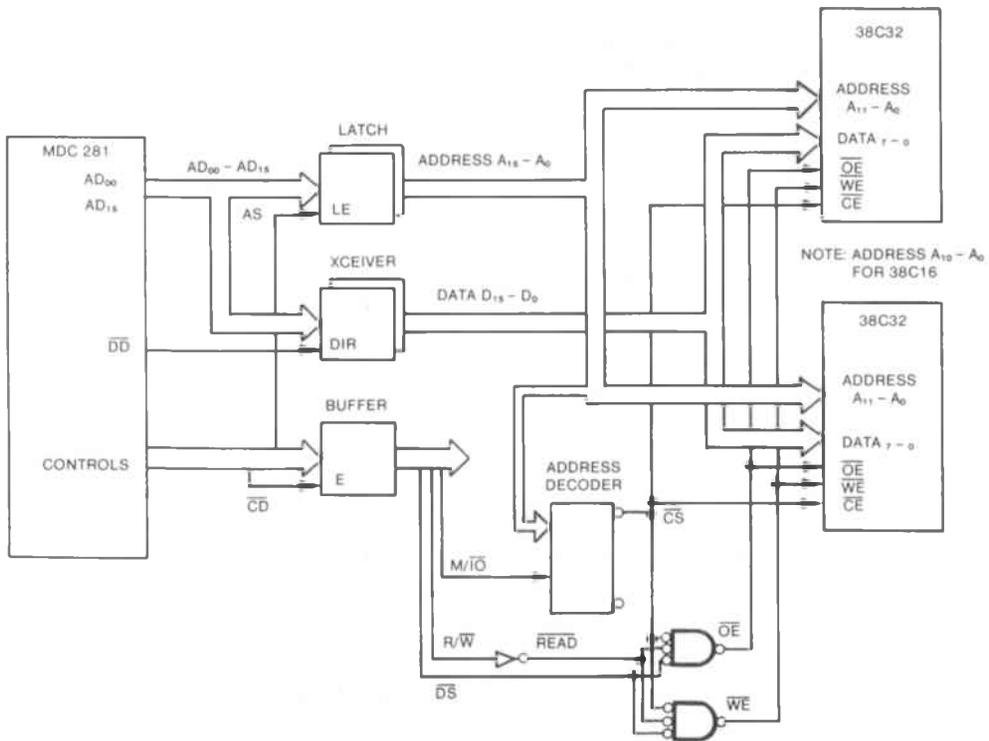


Figure 2. MDC281 INTERFACE TO 38C16/32

64K-word direct addressing and an optional expansion mode of 1-Mword direct addressing. The latter mode is segmented into 256 blocks of 4K-words each. The 38C16 and 38C32 offer an excellent fit for 1750A processors and give system designers/programmers a wider array of choices to come up with the next generation of flexible and more powerful adaptive systems.

### MDC281 MIL-STD-1750A CPU Module:

The McDonnell Douglas MDC281 is a certified MIL-STD-1750A (Notice 1) 16-bit CPU consisting of three custom CMOS/SOS LSI chips MDC17501 (Execution unit), MDC 17502 (Control unit) and MDC 17503 (Interrupt unit) mounted on and interconnected within a ceramic substrate. The MDC281 CPU is designed for military avionics applications like sensor data processing, operation and control of weapons systems. The CPU is particularly suitable for embedded applications requiring less than 64K-words of memory.

### 38C16/32 Interface:

A typical MDC281 interface to 38C16/32 memory is shown in fig 2. 38C16-70 or 38C32-70 with a maximum address access time of 70 ns can be used without wait states in the memory subsystem for a 20 MHz MDC281. For a complete description of pin assignments and signal functions refer to the MDC281 data sheet. Each machine cycle consists of a minimum of 5 OSC periods. The synchronization clock ( $\overline{\text{SYNC}}$ ) output high to low transition signals the start of a new machine cycle and is used as the timing reference.  $\overline{\text{SYNC}}$  low indicates that address is on the AD bus. The AD bus is a bidirectional multiplexed Address and Data bus ( $\text{AD}_{00} - \text{AD}_{15}$ ). This bus is shared between the external system and the internal module resources and hence to avoid bus contention, the AD bus must be isolated from the external system using a bidirectional transceiver. Data Direction signal  $\overline{\text{DD}}$  is used for transceiver

direction control.  $\overline{\text{DD}}$  low indicates read transfer, while high indicates a write transfer. High to Low transition of the address strobe AS is used to latch Address into a transparent latch during AD bus de-multiplexing.

All transfers between the module and the memory are referenced to the AS and  $\overline{\text{DS}}$  bus control signals and are characterized by  $\text{IN}/\overline{\text{OP}}$  low and  $\text{M}/\overline{\text{IO}}$ ,  $\overline{\text{CD}}$  high. Control Direction signal  $\overline{\text{CD}}$  is used to control direction of the control signal transceiver. This signal goes high to indicate that the module is driving the AS,  $\overline{\text{DS}}$ ,  $\text{M}/\overline{\text{IO}}$ ,  $\text{RD}/\overline{\text{WR}}$  and  $\text{IN}/\overline{\text{OP}}$  signals.

### Read Operation:

Read transfers begin with address being placed on the AD bus immediately following  $\overline{\text{SYNC}}$  high to low transition. This address is assured to be valid for the cycle by latching it in a transparent latch on the high to low transition of AS. The  $\overline{\text{DD}}$  signal is high during this portion of the transfer.  $\text{RD}/\overline{\text{W}}$  indicates direction of transfer. During read (fig. 3) the AD bus drivers are placed in a high impedance state at the low to high transition of  $\overline{\text{SYNC}}$  to give the memory access to the bus. Next  $\overline{\text{DS}}$  signal goes low and is used by the memory system to generate output enable ( $\overline{\text{OE}}$ ).  $\overline{\text{DD}}$  also goes low shortly after  $\overline{\text{DS}}$  goes low and this signal reverses the direction of the AD bus transceivers. The memory then pulls  $\overline{\text{RDY}}$  low to conclude the transfer. Read data from the 38C16/32 is latched into the module on the  $\overline{\text{SYNC}}$  high to low transition.

### Write Operation:

Write is indicated by  $\text{RD}/\overline{\text{W}}$  going low (fig. 4). The address is replaced by data when  $\overline{\text{SYNC}}$  transitions from low to high. Next, the  $\overline{\text{DS}}$  signal goes low and is used by the memory system to generate  $\overline{\text{WE}}$ . Data is valid at the low to high transition of  $\overline{\text{DS}}$  and is latched into the 38C16/32.  $\overline{\text{DD}}$  stays high for the duration of a write transfer. The memory system pulls  $\overline{\text{RDY}}$  low to conclude the transfer.

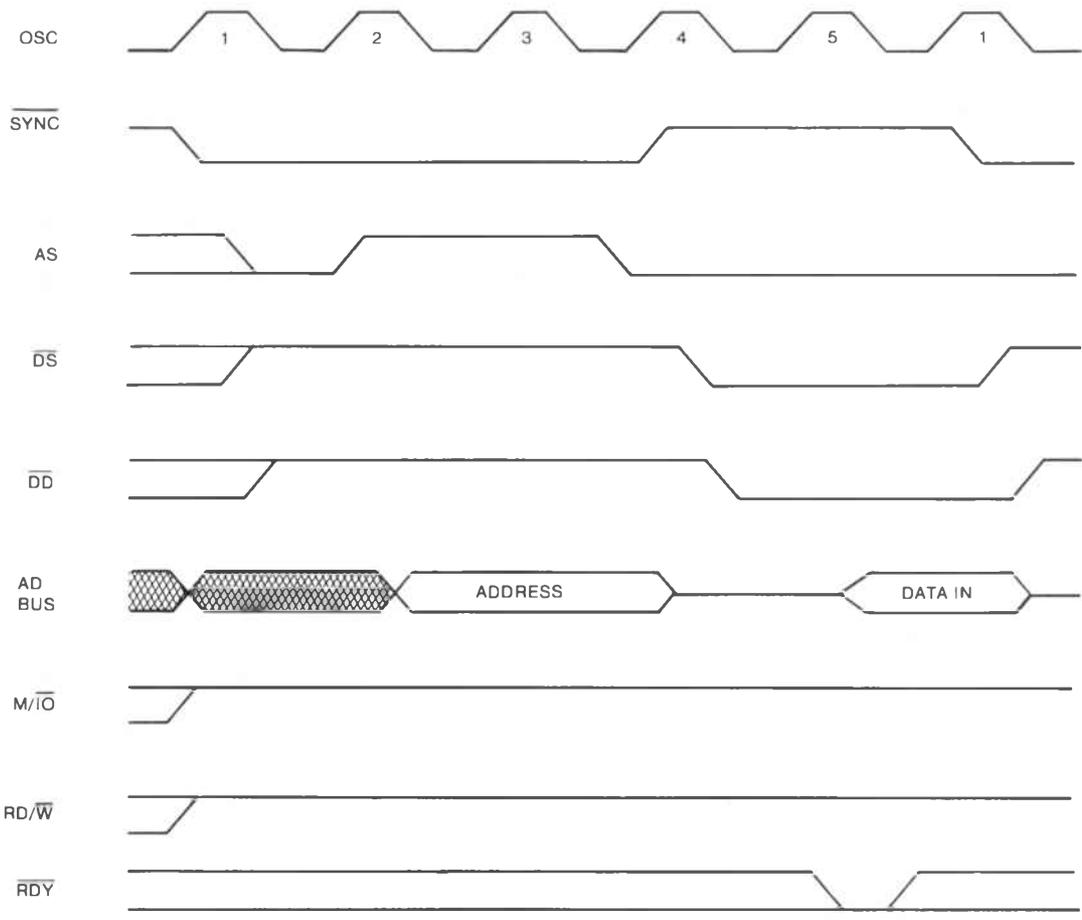


Figure 3. MDC281 READ CYCLE

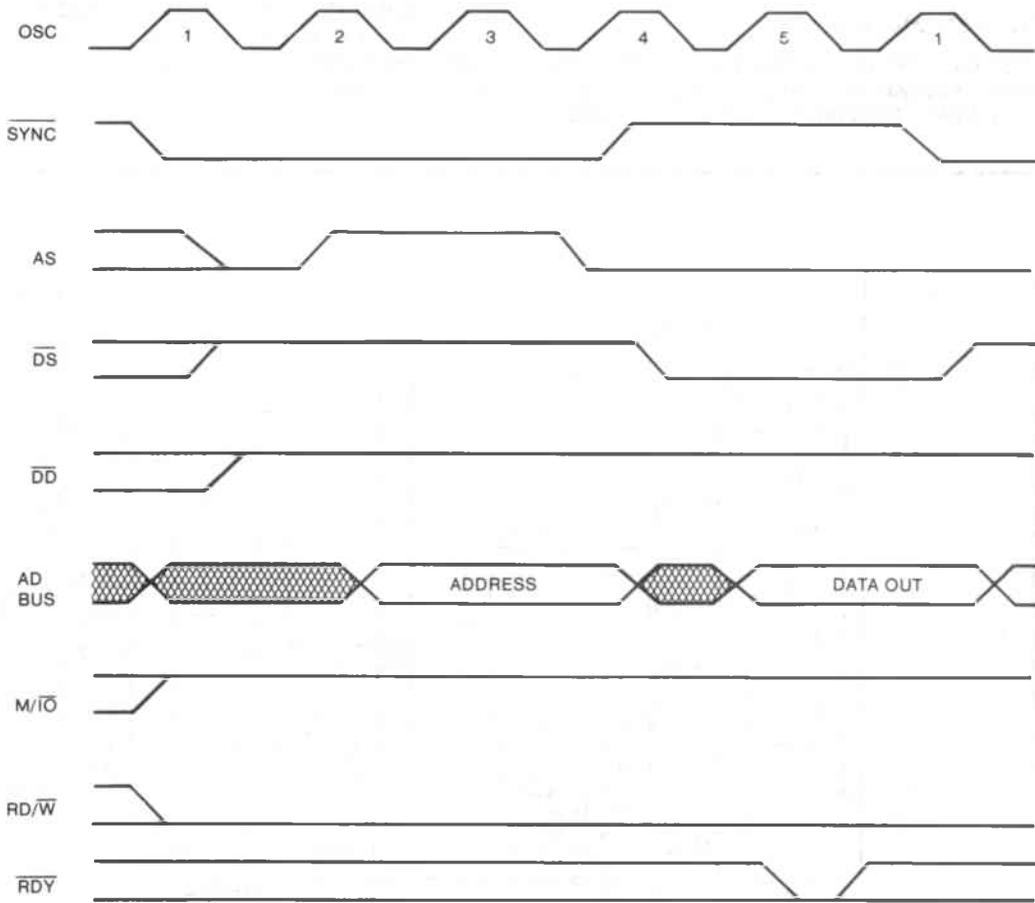


Figure 4. MDC281 WRITE CYCLE

### Fairchild 9450:

Fairchild 9450 is single chip solution implementing the complete MIL-STD 1750A instruction set architecture (ISA) and its floating point standard. It allows addressing of up to 2M words of memory and with the addition of the F9451 Memory management unit (MMU), up to 16M words of memory.

### 38C16/32 Interface:

A typical minimal configuration 38C16/32 memory subsystem interface is shown in fig. 5. The 20 MHz F9450 provides for a 90 ns memory

access time without wait states. Hence, 38C16-70 or 38C32-70 with a maximum address access time of 70 ns can be used in the memory subsystem. Bus cycles are a minimum of 4 or 5 states long. Memory and  $\overline{I/O}$  cycles are identical and the status of the  $M/\overline{I/O}$  line distinguishes the two cycles. State  $S_0$  is used for bus acquisition. This state is followed by  $S_1$  state. After the start of  $S_1$  state, the CPU outputs the address after a delay. At the end of  $S_1$ , RDYA input is sampled. If RDYA is low the CPU stays in  $S_1$ , extending the address phase of the bus cycle. Otherwise, it proceeds to states  $S_2$  followed by  $S_3$ .

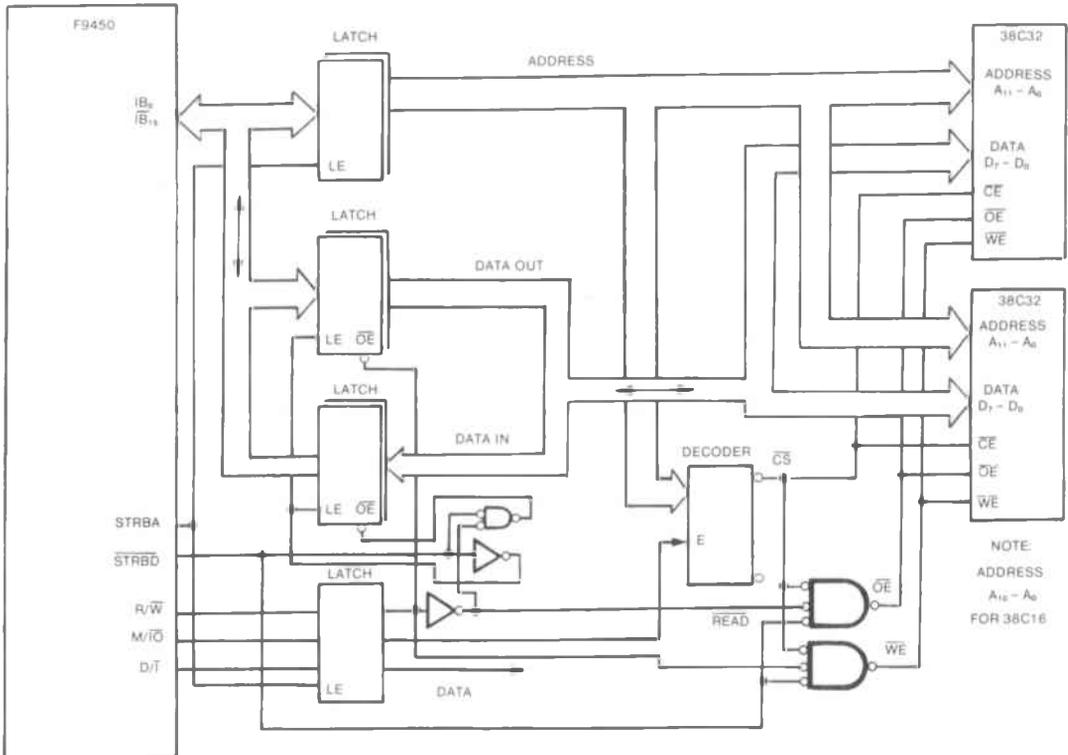
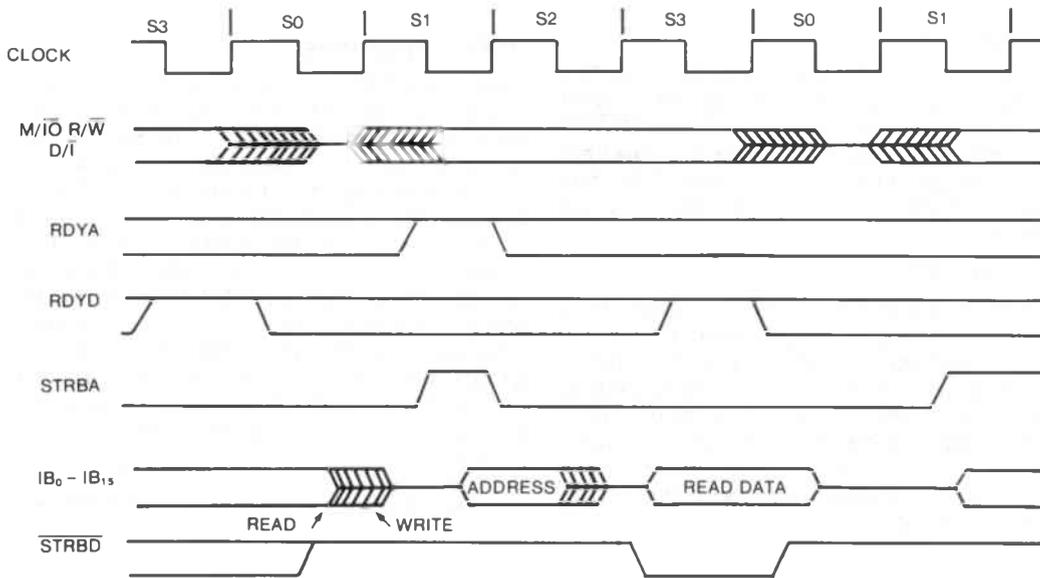
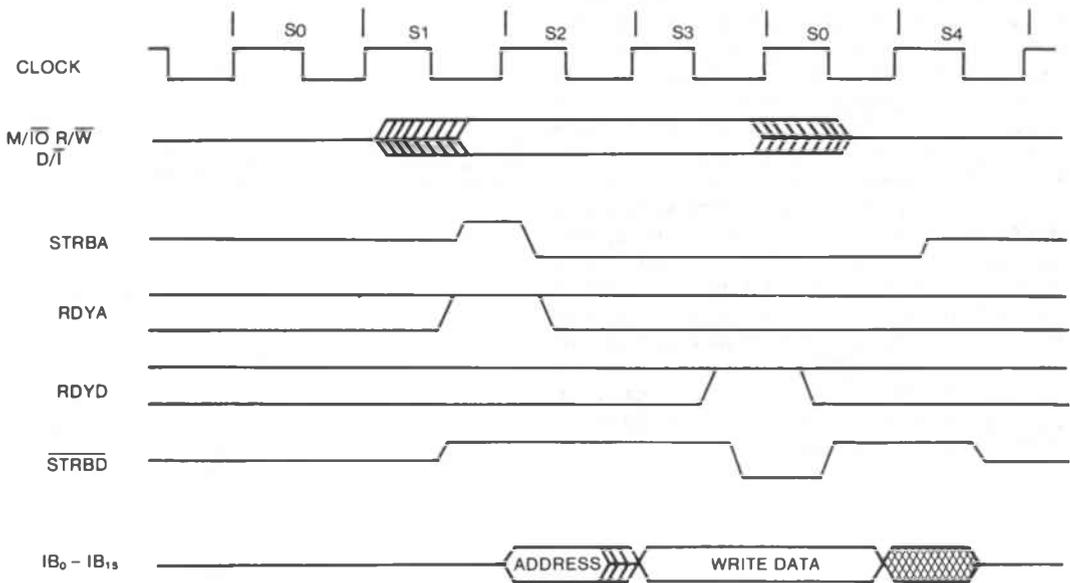


Figure 5. F9450 MEMORY INTERFACE



**Figure 6. F9450 READ CYCLE**



**Figure 7. F9450 WRITE CYCLE**

### Read Operation:

STRBA signal is pulled low in state  $S_2$  (fig. 6). The high to low transition of this signal is used to latch the memory address. The CPU then pulls STRBD output low and prepares to receive read data from 38C16/32 by turning the address/data bus around. STRBD is used to enable data from the memory.

### Write Operation:

During write cycles the CPU starts driving the bus with the write data immediately after the address (fig. 7). STRBD signal is activated during  $S_3$ , allowing enough write data setup time to STRBD falling edge and hold time for the rising edge of STRBD to write data. At the end of  $S_3$  RDYD is sampled, and if low, state  $S_3$  is continued extending the data phase. If the signal is sampled high the write cycle is terminated.

### Software Considerations:

Examples of hardware interface of MIL-STD-1750A microprocessors to 38C16/32 have been shown. 38C16/32 have a built-in timer to control the internal non-volatile write cycle. The parts feature an automatic erase before write. The write cycle takes a maximum of 5ms/byte. System software has to take into account this byte write time of the EEPROM. The system writes to the EEPROM and then follows the write with a polling routine as shown in fig. 1 to determine the end of the EEPROM internal write cycle. If the system application demands that the 5ms write time be utilized usefully, the technique shown in fig. 8 can be used. The on-board timers A or B can be used. These timers can be used to timeout the 5ms write time of the EEPROM and programmed to interrupt the CPU. The CPU can thus carry out other tasks while the internal write cycle of the EEPROM is in progress.

### DSP Applications:

Present day DSP processors are finding a wide range of applications like Encryption/Decryption, voice-band, precision servo control, pattern recognition, adaptive control and intelligent filtering. Most of today's applications use ROM or EPROM based memories to store algorithms and as a result use is restricted to applications that utilize fixed algorithms and co-efficients. Adaptive algorithms must use RAM, thus forcing the processor to repeat its adaption sequence each time power is turned on. Seeq's high speed CMOS EEPROMs 38C16 and 38C32 present an excellent fit for many of today's DSP processors and open the door for system designers and programmers.

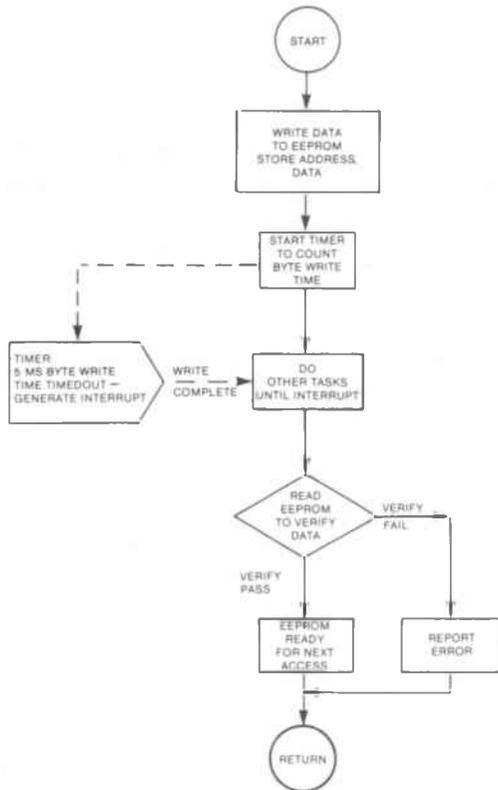


Figure 8. EEPROM BYTE WRITE SEQUENCE USING SOFTWARE CONTROLLED TIMER

### TMS320C25:

The TMS320C25 is a high performance digital signal processor featuring a single accumulator and a Harvard type architecture in which program and data are implemented in separate address spaces. The processor features on-chip data RAM of 544 words, on-chip program ROM of 4K words and supports direct addressing of up to 64K words of external program memory and 64K words of external data memory. An on-chip serial port provides direct communication capabilities with serial devices.

For prototyping, system expansion, external memories may be required. The 38C16/32 can be used as program memory and offer the ability to implement adaptive algorithms because of their reprogrammability.

### 38C16/32 Memory Interface:

The TMS320C25 distinguishes between program memory and data memory spaces using  $\overline{PS}$  and  $\overline{DS}$  signals. For a detailed description of pin assignments and their functions refer to the 320C25 data sheet. The crystal or external clock source is divided internally by the 320C25 to produce a four phase clock. All bus activity is referenced to the four-phase clock. The interface discussed here is for a TMS320C25 running at 40 MHz. Fig. 9 shows 38C32-35 used as program memory. The 35ns maximum address time of the 38C32 satisfies the memory performance requirements of the 320C25.

### External Read Cycle:

During the beginning of machine cycle (fig. 10) clock quarter-phase1, the 320C25 begins driving

the address bus and one of the memory space select signals  $\overline{PS}$  or  $\overline{DS}$ .  $R/\overline{W}$  is driven high to indicate a read cycle. At the beginning of quarter phase2,  $\overline{STRB}$  goes low to indicate valid address.  $\overline{STRB}$  is used with  $R/\overline{W}$  to state memory read enable signal. After decoding the address, the memory system must set up  $READY$  during quarter-phase2.  $READY$  is sampled by the 320C25 at the beginning of quarter-phase3. If  $READY$  is sampled high, read data from the memory is clocked in at the end of quarter-phase3.  $Ready$  can be pulled high permanently, if the system components used do not require wait states. At the beginning of quarter-phase4  $\overline{STRB}$  is deasserted. The read cycle is terminated with the de-activation of the address bus and  $\overline{PS}$ ,  $\overline{DS}$ . Care must be taken to avoid bus conflicts when a read cycle is followed by a write cycle. The 38C32 has a 15ns max disable time and hence will not cause bus conflict.

### External Write Cycle:

The external write cycle is similar to the read cycle described above, with the following differences:  $R/\overline{W}$  is driven low indicate an external memory write.  $\overline{STRB}$  is used with  $R/\overline{W}$  to gate write enable signal. Write data is placed on the bus at the start of quarter-phase2.  $\overline{STRB}$  is deasserted at the beginning of quarter-phase4 and the write cycle ends with the de-activation of address bus and  $\overline{PS}$ ,  $\overline{DS}$ . As before, care must be taken to avoid bus conflict when a write cycle is followed by a read cycle. Since  $\overline{STRB}$  is used to enable the 38C32, potential bus conflict is avoided.

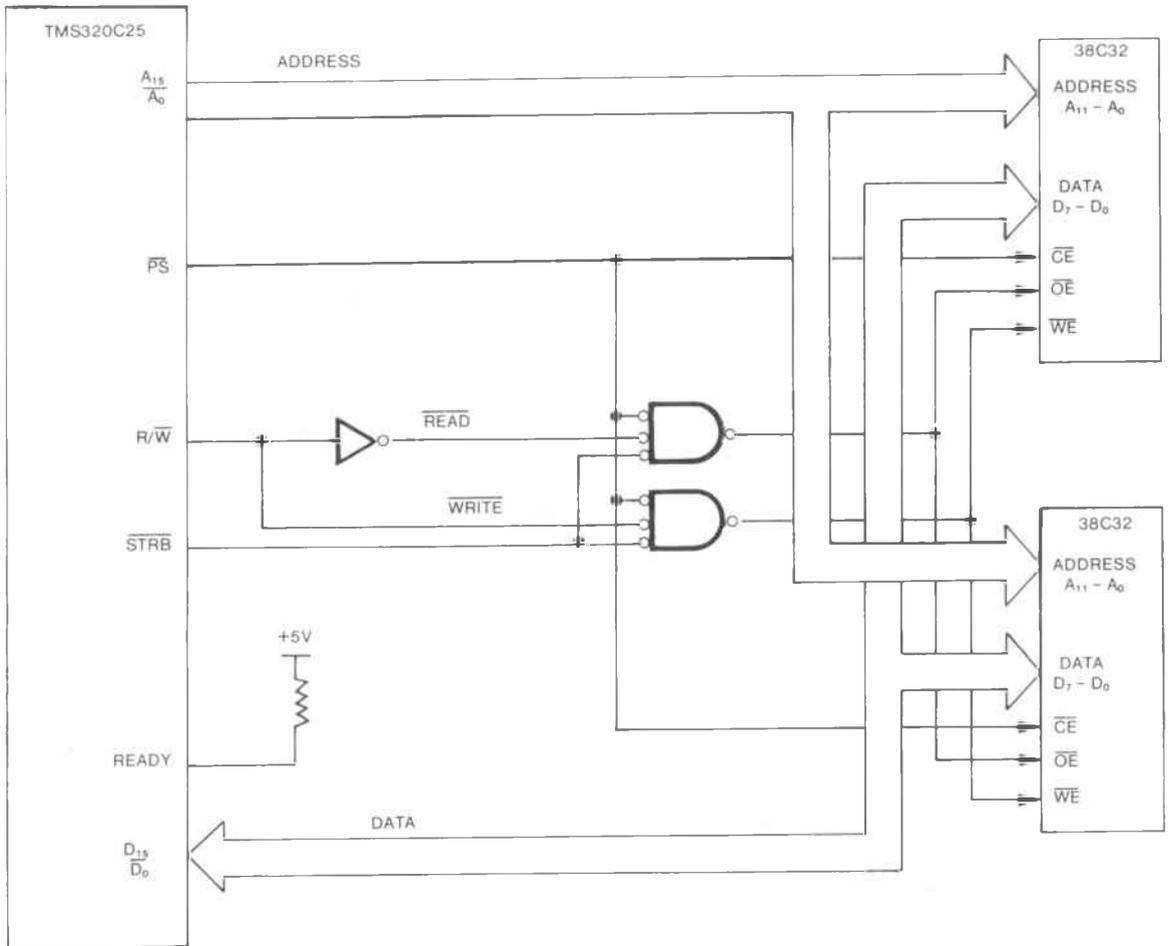


Figure 9. TMS320C25 MINIMAL EXTERNAL MEMORY INTERFACE

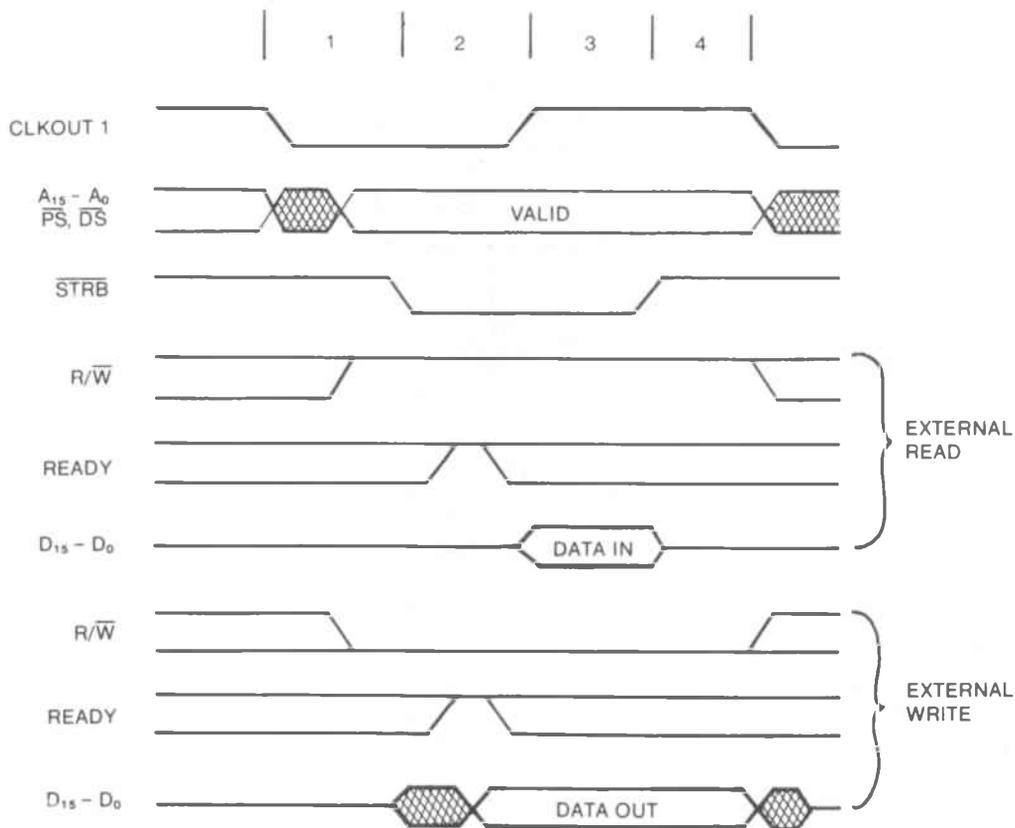


Figure 10. TMS320C25 READ AND WRITE CYCLES

**Software Considerations:**

When 38C16 or 38C32 are used as program memory, the system can take advantage of the easy reprogrammability of these devices. Code or Program coefficients can be easily altered to implement adaptive systems. The 38C16/32 byte write time of 5ms max should be accommodated by the system software (fig. 11). The on-chip timer can be utilized to timeout the byte write time. A timer interrupt is generated every time the timer decrements to zero. The period register (PRD)

can be used if necessary, so that interrupts can be programmed to occur at regular intervals.

Using the 38C16/32, remote down-load capabilities can be provided to the system using the on-chip serial port. Object code can be downloaded into RAM at high speed and then written into the EEPROMs from the RAM. Typical DSP algorithm implementations need up to 4K words of program space. Using the 38C16 or 38C32 only two packages are required thus minimizing package count.

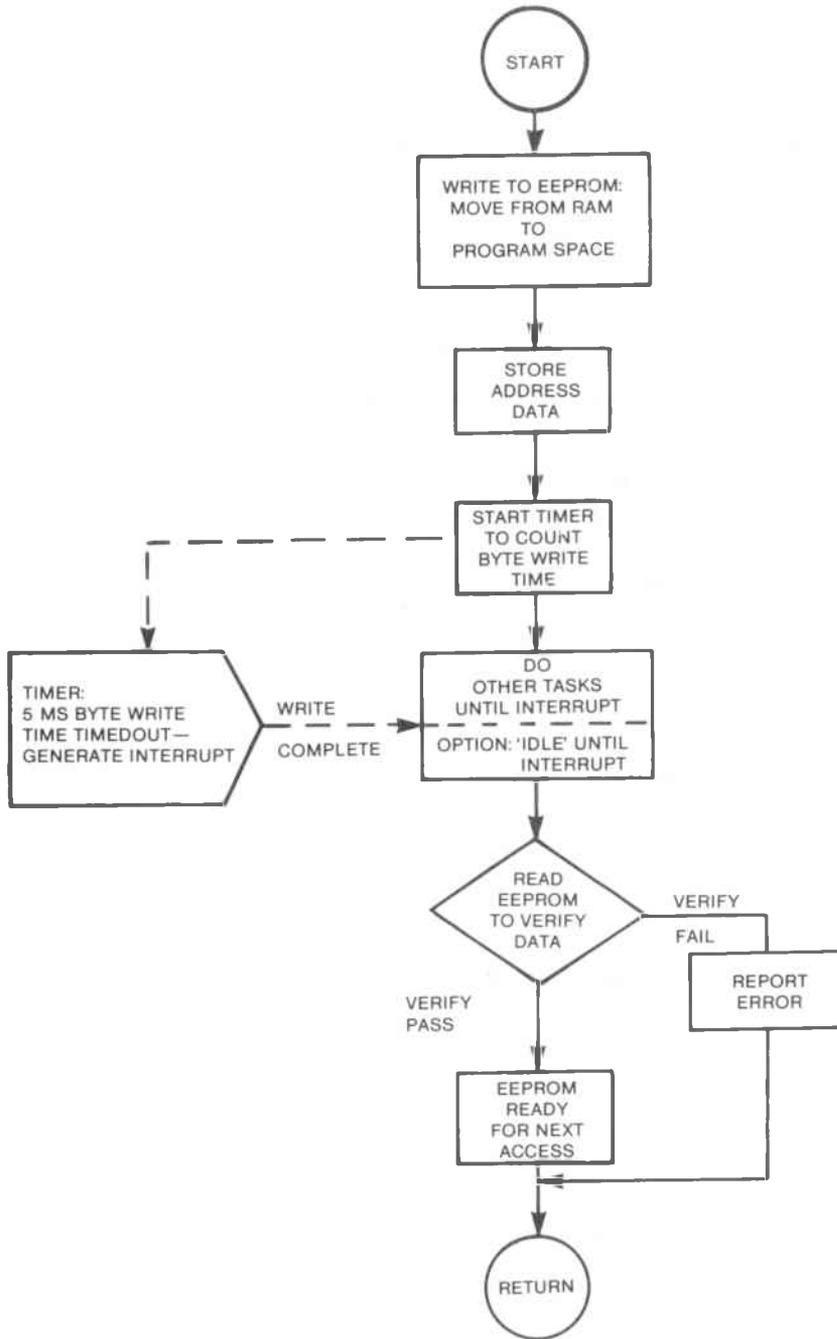


Figure 11. TMS320C25 WRITE SEQUENCE FOR 38C16/32 EEPROM WRITE.

7

***ARTICLE REPRINTS***



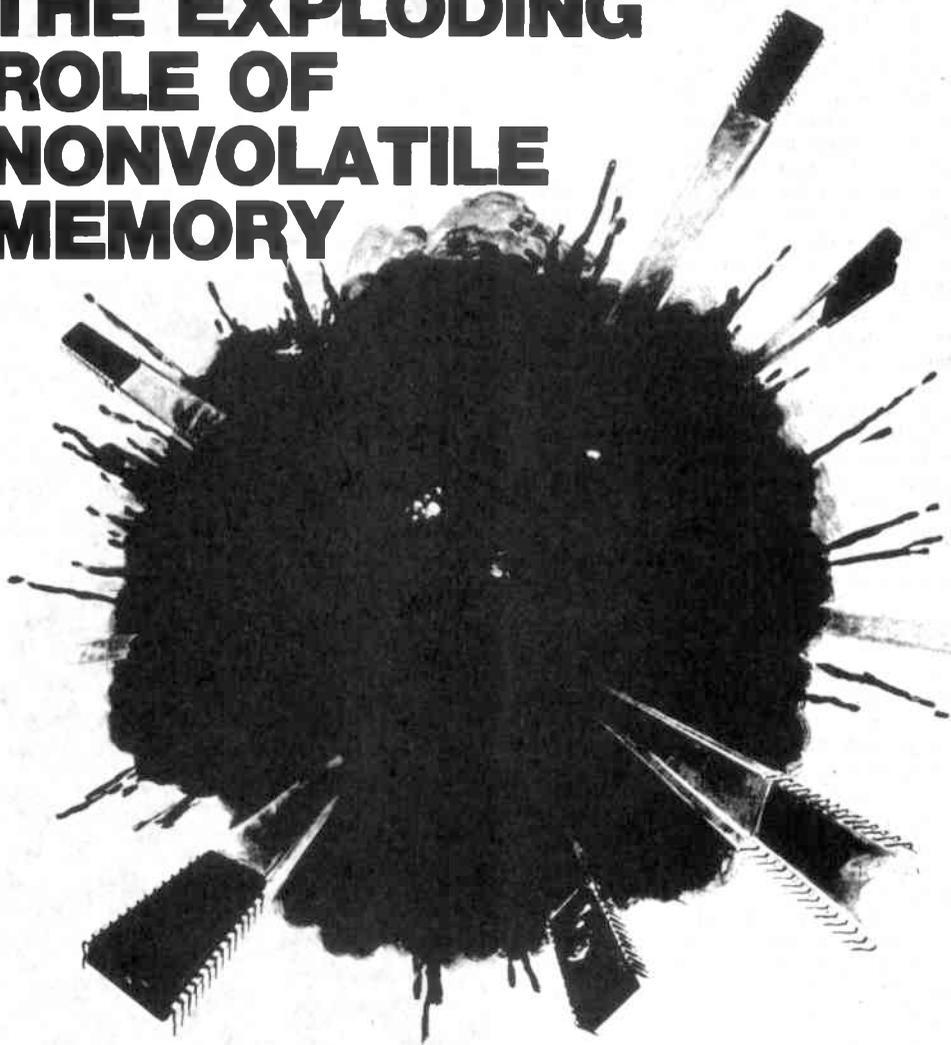
**HOW SEEQ IS PUSHING EEPROMs TO 1-Mb DENSITIES/53**  
**ISDN FINALLY STARTS TAKING OFF/57**

A McGRAW-HILL PUBLICATION

AUGUST 21, 1986

# Electronics

## THE EXPLODING ROLE OF NONVOLATILE MEMORY



ARTICLE  
REPRINTS

**T**he 1-Mb electrically erasable read-only memory has come a step closer, now that Seeq Technology Inc. is going into production with its version of a flash EEPROM. This device, so named because the contents of all the array's memory cells are erased simultaneously by a single field emission of electrons from the floating gate to an erase gate, combines the advantages of ultraviolet-erasable EPROMs and floating-gate EEPROMs. It unites the high density, small cell size, low cost, and hot-electron write capability of an EPROM and the easy erasability, on-board reprogrammability, high endurance, and cold-electron tunneling erasure of floating-gate EEPROMs. In doing so, Seeq's single-transistor 16-K-by-8-bit memory paves the way for high-density EEPROMs.

"No longer will EEPROMs trail EPROMs in density," says director of marketing Michael Villot. EPROM arrays have a 4:1 density advantage over the EEPROM, whose array densities still hover at the 256-K level. And even though EEPROM cells are now as small as  $57 \mu\text{m}^2$ , the EPROM cell remains one third its size with attendant cost advantages. But because flash EEPROMs are made with the same processes as EPROMs, says Gheorghe Samachisa, project manager, their prices will be competitive—and considerably lower than comparable two-transistor EEPROMs.

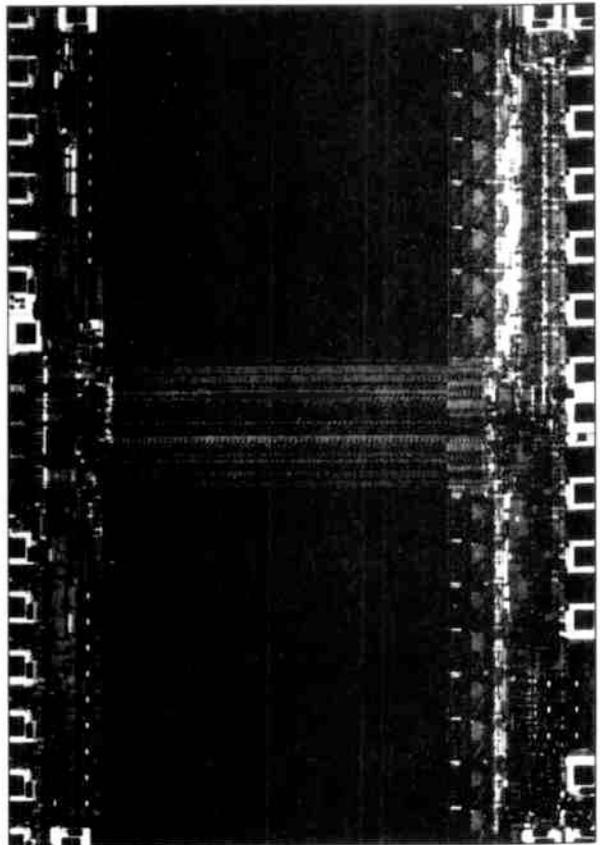
"In addition, because the flash EEPROM can track the density path of the EPROM very closely, it resolves a dilemma for those users who required the high density of EPROMs but also wanted the ease of erasability of EEPROMs," Samachisa says. The San Jose, Calif., company's first commercially available flash EEPROM (Fig. 1) is the  $2\frac{1}{2}\text{-}\mu\text{m}$  n-MOS 42128 QPROM, for quick EEPROM. It is based on a proprietary  $44\text{-}\mu\text{m}^2$  single-transistor cell half the size of standard EEPROMs (Fig. 2). It will be followed soon by versions in the 512-K to 1-Mb range, says Villot.

Flash EEPROMs have two functional advantages over EPROMs—fast erasure and in-circuit reprogrammability. "Flash EEPROMs erase in about 1/60th of the time—no more than 20 seconds," says Samachisa. It takes a design engineer about 1 minute to erase and reprogram a flash EEPROM, compared with 20 minutes or more for an equivalent EPROM. These advantages cut the time needed to design a system and upgrade it in the field.

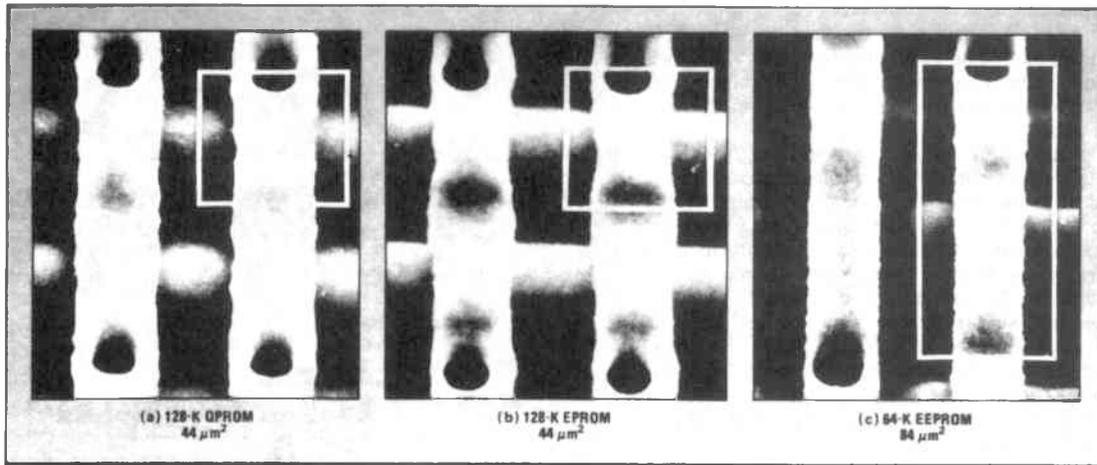
Even if in-circuit reprogrammability is not

## HOW SEEQ IS PUSHING EEPROMs TO 1-Mb DENSITIES

*Combining the fast programming techniques of EPROMs with the erasure mechanism of EEPROMs results in a high-density device with the best of each*



**1. FLASHY.** Seeq's n-MOS 128-K 48128 QPROM is a flash EEPROM whose cells are erased simultaneously by a single field emission of electrons from a floating gate to an erase gate.



**2. SMALL CELL.** At  $44 \mu\text{m}^2$ , the cell size of Seeq's QPROM (a) equals that of an EPROM cell (b) and is half that of an EEPROM cell (c).

used, Samachisa says, the flash EEPROM still comes out ahead of the EPROM because it can be upgraded in the field. This eliminates the need for an inventory of EPROM spares; it also ends the waste when replaced memories are discarded rather than returned for reprogramming. Further, as with less-dense traditional EEPROMs, the high-density flash chips can be soldered into the equipment. Erasing and reprogramming in the field are done either by removing cards and placing them in a special programmer or by programming them without removal from the system when the required high-voltage programming and erasure voltages are available.

### EPROMs vs. EEPROMs

An EPROM cell is relatively simple in structure. It is a true single-transistor cell, usually consisting of two polysilicon gates. The upper one, connected to row decoders, is the control gate, and the bottom one is a floating gate between the control gate and the substrate, isolated in the surrounding silicon dioxide. Programming, or writing, is done by avalanche injection of hot electrons from the substrate through the isolating oxide under the influence of a high applied drain voltage. This causes an electrical charge to be collected on the floating gate. The electrons must gain enough energy to jump over, rather than through, the potential energy barrier between the silicon substrate and the silicon dioxide. When the high programming voltage is removed, the charge is trapped on the floating gate by the surrounding oxide insulator.

To pull the electrons toward the floating gate requires application of a high positive select voltage. As the gate becomes more charged, the electrons in the oxide field are repelled from the floating gate and move back to the substrate.

An EPROM cell is erased through internal photoemission of hot electrons from the floating

gate to the control gate and the substrate. Incoming UV light increases the energy of the floating-gate electrons to a level at which they jump the potential energy barrier between the floating gate and the  $\text{SiO}_2$ . This avalanche injection can occur with oxides as thick as 1,000 Å, which makes the devices relatively easy to fabricate. However, they can be used only to write and have no deprogramming mechanism. This necessitates the use of an alternative method, such as UV light, to discharge the gate. In addition, says Samachisa, there's a tradeoff for the EPROM's small size (about  $20 \mu\text{m}^2$  at the 1-Mb level) and low cost. Designers have had to settle for low endurance—no more than 100 to 1,000 erase/program cycles.

EEPROMs' chief advantages are significant system flexibility, thanks to on-board programming capabilities, and an endurance of 10,000 to 1 million cycles. To achieve this, most manufacturers use a two- to three-element cell with two transistors and one tunneling dielectric element per cell. One transistor is used for reading, the other for programming and erasure. Standard EEPROMs are erased by means of the Fowler-Nordheim effect, in which cold electrons are tunneled through, rather than over, the energy barrier at the silicon- $\text{Si}_2\text{O}$  interface and into the oxide conduction band.

The advantage of the Fowler-Nordheim approach is that it can be reversed and used for programming. Its disadvantage is that it depends on the manufacturer's ability to process thin-oxide layers (100 Å or less, depending on the technology) that have high reliability. Processing gets more difficult as device geometries shrink.

The program-erase operation of the EEPROM cell depends on the ability to apply a large reversible electric field to the thin oxide separating the floating gate from the substrate. This field must be strong enough to produce a measurable

current through the thin oxide by indirect tunneling. At the same time, the field in the interpoly-silicon oxide has to be maintained at a relatively low value to prevent unwanted transport of electrons between the floating gate and the control gate.

During programming and erasure, the thin-oxide field is controlled by the relative voltage applied to the control gate and the drain overlap region, resulting in much lower programming voltages than EPROMs. Erasure is performed by charging the floating gate, resulting in a logical-1 state in the cell. It occurs when the source, drain, and substrate are grounded and the control gate is raised to a high voltage. Programming is done by tunneling electrons from the floating gate to the  $n^+$  drain diffusion by grounding the control gate and applying the programming voltage to the drain diffusion. This produces a logical-0 state in the cell.

Unlike an EPROM cell, in which the control gate also acts as the select transistor, an EEPROM cell requires a separate select transistor linked in series with the floating-gate transistor to read the device. During a read operation, the cell's state is determined by current sensing by means of the select transistor.

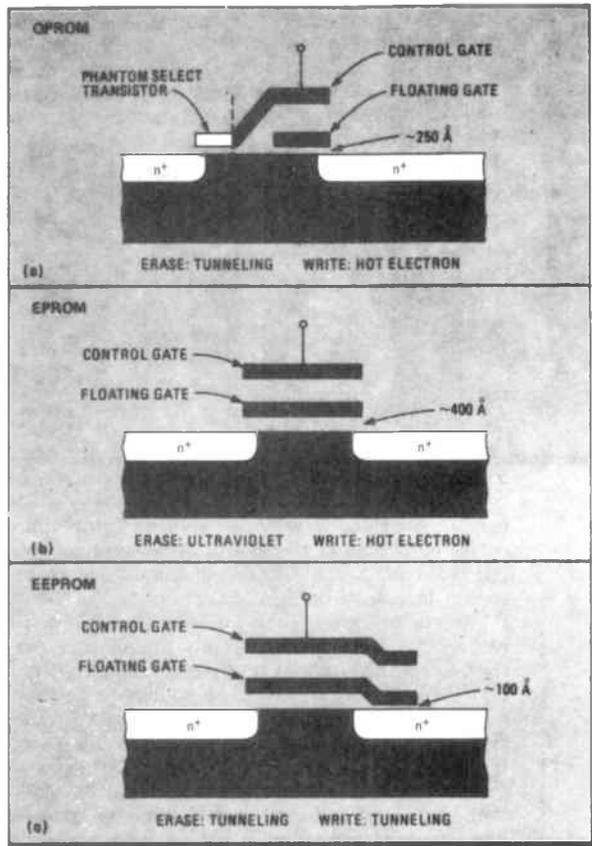
### ENTER THE FLASH EEPROM

In contrast, the flash EEPROM combines the programming, write and erase, and read-select functions in a single-transistor structure (Fig. 3). Frustrated by the high cost and low density of traditional EEPROMs, a number of companies recently have investigated single-transistor structures for flash EEPROMs (see story, p. 47). In other companies' approaches, though, an important functional problem remains, says Samachisa. "In the erased state, the cell's floating gate is depleted of electrons and behaves like a depletion-mode transistor. What this means is that a nonaddressed cell in the erased state leaks current. This leakage can cause false data reads and/or a failure to program."

Seeq's design, however, modifies the basic EPROM so that the poly gate controlling the channel between it and the floating gate extends beyond the floating-gate edge, creating a "phantom" select transistor. This eliminates the need for another transistor.

The cell is self-aligned at both the drain and source sides. The section of the channel under the influence of the control gate forms an n-channel select transistor that operates in the enhancement mode, in effect linked to the floating-gate transistor in series. This prevents leakage during read and programming through an erased cell that has not been addressed.

The QPROM cell programs like an EPROM cell, using hot-electron injection in the channel between the control gate and the floating gate. During programming, the phantom select transistor is on only in the addressed cell. In all



**3. EPROM/EEPROM.** The QPROM cell (a) merges the EPROM write mechanism (b) and EEPROM erase mechanism (c) with the read-select transistor into a single structure.

nonaddressed cells, the select transistors are off.

The QPROM is erased by Fowler-Nordheim tunneling of electrons from the floating gate to the drain diffusion, during which the control gate is grounded and the drain raised to a high voltage. The erase speed depends on the oxide thickness and the potential voltage difference between the floating gate and the drain. It can be improved by decreasing the oxide thickness or increasing the drain voltage, but both approaches have disadvantages. Scaling the oxide requires similar scaling in the horizontal direction, increasing the complexity of the process and increasing cost. Increasing the drain voltage adds the risk of breakdown and reduces reliability. In the Seeq approach, thin oxides are used only at the drain electrode in the overlapping area between the drain diffusion and the floating gate, which makes it easier to manufacture than devices using thin oxides throughout.

Built with a relatively conservative 2.5- $\mu\text{m}$  process, a 128-K QPROM cell measures about 44  $\mu\text{m}^2$ , the same as a cell in the company's 27128

EPROM. The device can be erased and reprogrammed in less than 1 minute, versus 20 minutes or so for an equivalent EPROM: 20 seconds to raise the program voltage pin to 21 V in order to reset all memory locations to logic-1 states, and 32 seconds for programming. A 90- $\mu$ s programming pulse is then applied on a byte-by-byte basis after data is validated; the pulse is repeated for all addresses to be written.

### BEYOND 128-K

Moving from 2.5 to 2  $\mu$ m, Samachisa says, will allow densities in the 512-K range. And scaling to about 1.5  $\mu$ m will push flash EEPROM densities beyond 1 Mb.

More importantly, if the flash EEPROM cell is scaled, the 21-V programming and erasure voltages can also be scaled to the 5- and 12-V levels typical of standard EEPROMs. "This will extend the applicability of flash-erase EEPROMs to systems that might have used standard EEPROMs if they were more cost-effective," Samachisa says. "With scaling, additional EEPROM-like features

can be added, such as page-mode erase and programming, latches, and on-chip timers."

Currently, the endurance of the company's first flash EEPROM is about 100 erase/program cycles, approximately equivalent to that of an EPROM. However, says Samachisa, it should be possible to improve endurance considerably with a combination of process enhancements and circuit-design improvements. And because the double-poly process used to fabricate the QPROMs is similar to that used in high-endurance EEPROMs, nonvolatile memory combinations merging the low cost and high density of the former with the high endurance and byte erasability of the latter are also possible, he says. □

*TECHNOLOGY TO WATCH is a regular feature of Electronics that provides readers with exclusive, in-depth reports on important technical innovations from companies around the world. It covers significant technology, processes, and developments incorporated in major new products.*

## THE QUEST FOR A HIGH-DENSITY EEPROM BEGAN OVER A CUP OF COFFEE

The EPROM grew out of a conversation that Gheorghe Samachisa, project manager, held in late 1984 over coffee with several members of Seeq Technology Inc.'s research and development group.

"We were talking about the technical papers that had been appearing describing various approaches to building high-density megabit EEPROMs," he says. "A number of them were highly imaginative designs. But all had critical flaws." One had small enough cells, but the process and transistor structure were too complex. Another had a simple structure but still was prohibitive to make. A third had the right balance of all these factors, but it was not reliable.

Samachisa remembers that at one point he groaned in frustration and burst out: "There has just got to be a simple way to design an easily erasable, nonvolatile memory cell that is as cost-effective as an EPROM but has all the features of an EPROM." At that point, he began scribbling ideas on pieces of napkin and passing them to coworkers George Smarandoiu, Chien Su, and Ting Wong. It was several weeks before he came up with a scheme he thought might work, and several months working with staff process engineer Su to determine if the device could be fabricated.

Samachisa, 50, is a 1977 graduate of the Polytechnical Institute in Bucharest, Romania, with a doctorate in semiconductor physics. He was a professor of semiconductor devices there until joining Seeq three years ago to work on standard EEPROMs.

Smarandoiu, 41, is an engineering department manager for EPROM development. Before joining Seeq five years ago, he headed the semiconductor R&D Institute in Bucharest. From 1975 to 1977, he worked at Siliconix Inc., where he developed the first monolithic MOS codec. A 1969 graduate of the Polytechnical Institute, he received a master's degree in engineering from the University of California at Berkeley in 1978.

Su, 37 and a graduate of the University of New Mexico in 1982 with a doctorate in electrical engineering, spent two years in the EPROM department at Intel Corp. before joining Seeq in 1984. The 36-year-old Wong, director of engineering in charge of special projects, has been with the company for four years. A 1977 graduate of the University of Pennsylvania with a doctorate in electrical engineering, he worked for six years in nonvolatile memory and static RAM development at Fairchild Semiconductor Corp. and Intel.

"The idea for the QPROM would not have occurred if we had only had experience in EEPROMs or just in EPROMs," Samachisa says. "What it required was an understanding of both, as well as a number of other memory technologies. It also required a company willing to take a risk on a new approach to nonvolatile memory."

Also contributing to the development of the flash EEPROM was Chenning Hu, professor of electrical engineering and computer science at UC/Berkeley, who served as project consultant.

For good ideas to come to fruition, says Samachisa, it "takes the right mix of expertise, within the company and within the design group. And that is what we had."



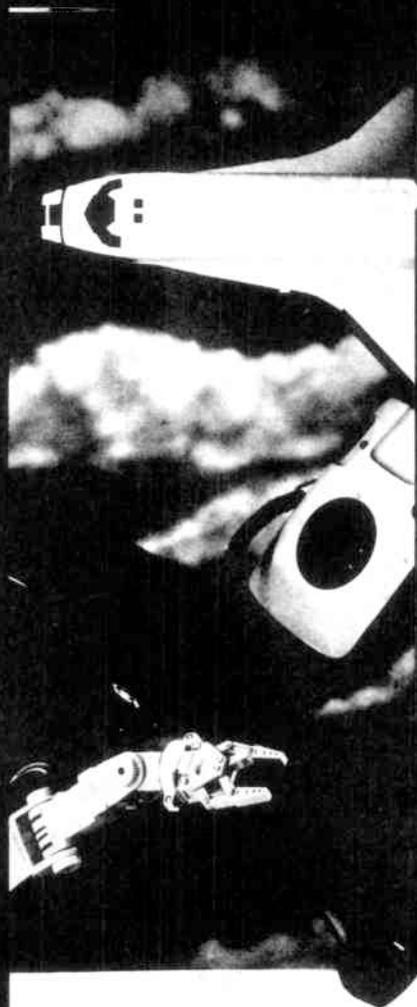
**RIGHT MIX:** Su, Wong, Smarandoiu, and Samachisa (from left) took Seeq's flash EEPROM from development to production.

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# DIGITAL DESIGN

MARCH 1986

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# 256K EEPROM Opens NEW DOORS For Designers

by Massoud Shamsirian and  
Ching Jenq, Seeq Technology

Since 1981, the bit densities of Electrically Erasable Programmable Read Only Memories (EEPROMs) have increased 16 times. Today's 64K EEPROMs allow a typical program memory size of 128 Kbytes. However, next generation 256K EEPROMs will make it feasible to design a single board containing memory of 1 Mbyte or more.

With these larger systems, data load time becomes critical. Because the write time of existing EEPROMs is specified at 10 msec/byte, updating current systems can take 3 hours.

At the current 64K level, programming time can be reduced two ways. First, individual byte write times can be reduced from 10 msec to 2 msec, simply by using faster 2-msec byte write EEPROMs. No additional hardware or software is required when replacing the 10-msec part. The second method is to use page mode. This can decrease the overall write time by a factor equal to the page size (the larger the page, the lower the average byte write time). However, there are two problems with the existing page mode. First, the page size and timing vary among the EEPROM manufacturers. Second, the specifications often limit the designer's ability to utilize the full page size and to maximize system data transfer rates.

ARTICLE  
REPRINTS

Seeq Technology's (San Jose, CA) CMOS 28C256 EEPROM is an attempt to address and overcome these difficulties (Figure 1). System implementation of the page mode feature has been simplified, while maintaining compatibility with existing 64K EEPROMs (both page and nonpage mode parts). The write time is reduced in both the single byte and page modes. The byte write time is specified at 2.5 msec, a 4 times improvement over the 10-msec byte write EEPROMs. The page size is 64 bytes, consequently, the "effective" byte write time is 160  $\mu$ sec/byte. In addition, the 28C256's extended page load cycle and improved page load timing optimizes system data transfer rate and timing compatibility with the existing page mode.

**Window Constraints**

First generation page mode devices were introduced a year ago, with a page size 16-bytes long and a 150- $\mu$ sec fixed-page load time. The page buffer required a minimum of 3  $\mu$ sec between two writes.

Unfortunately, only a handful of applications could use this feature because specifications on page load time, as well as time between two writes to the page buffer, were too complex to make interfacing with most microprocessors easy.

To use this feature and reduce write time, as many bytes as possible had to be loaded in a fixed specified time (i.e., page load time). Since the load time was fixed, the maximum number

of bytes that could be loaded at one time depended on the system's data transfer speed. Full page utilization was only possible if the system had a minimum data transfer rate of 9  $\mu$ sec/byte (150  $\mu$ sec/16 bytes). Slower systems could only load a portion of the page. The slower the transfer rate, the fewer number of bytes available.

For example, an 8085-based system with an operating frequency of 3 MHz can only load 9 bytes in 150  $\mu$ sec, since the time between two writes is about 16  $\mu$ sec. In this example, an EEPROM program subroutine is called as a result of an interrupt. In the subroutine, the 8085's D and E register pair in the register array is used to point to the EEPROM destination address, while the H and L register pair contains the source address. A byte of data is first moved into accumulator A and then transferred out to the EEPROM. Register B is initialized at the beginning of the subroutine with the number of bytes (maximum of 16) that need to be transferred. This register is decremented each time a byte of data is loaded into the EEPROM. The processor exits the subroutine when the B register is zero. Figure 2 shows an 8085 assembly instruction required to load the EEPROM page. As shown, the page mode cannot be fully utilized in slow systems.

In faster systems, the page can be used effectively if additional software is written to overcome the 3- $\mu$ sec "time between two writes" specification. Since the time between two writes is less than 3  $\mu$ sec in some systems, the processor must wait before it can load another byte. The required software delay loop can be as long as 2  $\mu$ sec.

For example, an 8088-based system requires more than 1- $\mu$ sec delay time between a 2-byte load, since data can be trans-

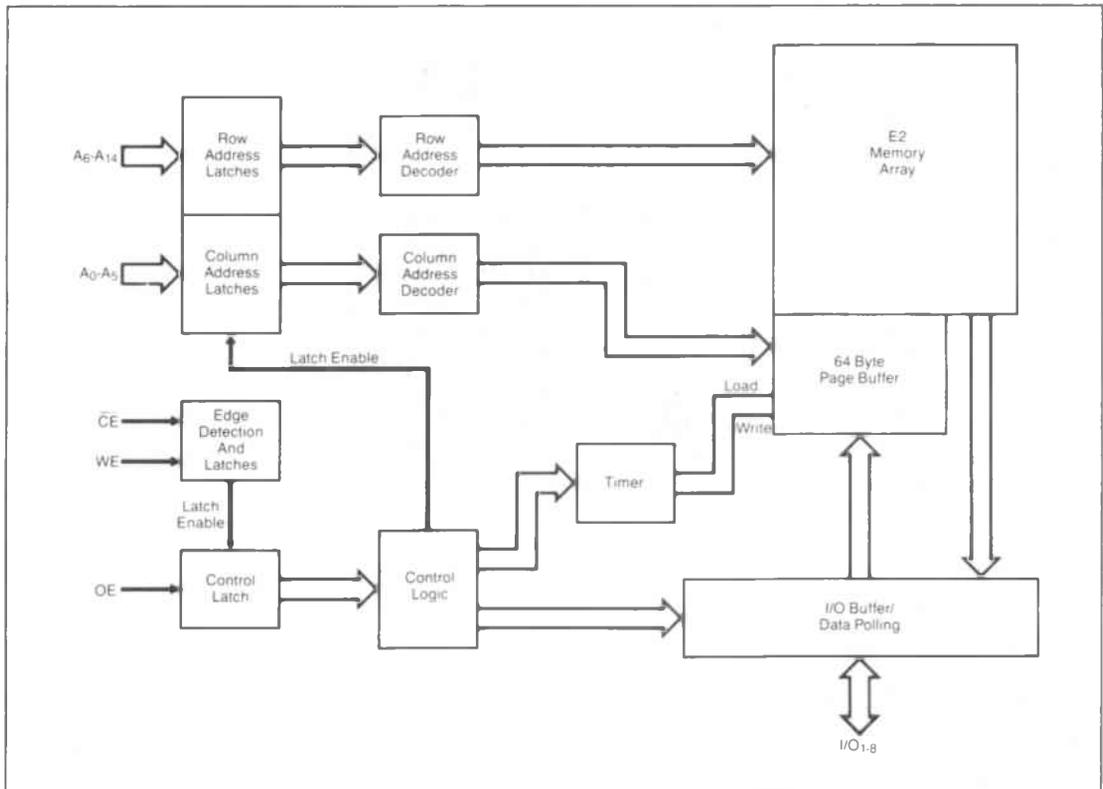


Figure 1: The 28C256 256K EEPROM from Seeq Technology is specified with an endurance of 10,000 cycles/byte.

ferred once every 2  $\mu$ sec. To fully use the 8088's capabilities in this example, a string instruction is used for data transfer. The EEPROM program subroutine uses the SI register in the execution unit to point to the source address, while the DI register, also in the execution unit, is used to point to the EEPROM destination address. The data transfer continues until the CX register (initialized earlier) is zero. The processor then returns to its original program.

68000-based systems also require the additional software delay. Figure 3 shows an 8088 assembly language software

## Refinements to the EEPROM page mode feature have eliminated the performance limitations of early page mode parts. The combination of fast byte write and page mode in a single part gives designers the best of both worlds.

routine used to load the page. In this subroutine, the software delay is not included. However, the page mode feature's implementation deficiencies, noted above, have prompted a new concept in page mode design.

### Turning A New Page

The 28C256 EEPROM has a 64-byte page that reduces writing time while simplifying system implementation. A retriggerable page mode eliminates the earlier page mode's fixed-page load time constraint, allowing designers to load as many bytes as desired (maximum of 64) as fast as 350 nsec/byte, or as slow as 300  $\mu$ sec/byte. The loading specifications provide compatibility with both fast and slow systems.

The page consists of 64 registers. Data is loaded into these registers, then written into the main memory. Upon the first byte write, an internal 300- $\mu$ sec timer starts counting. If an additional byte is loaded before the timer has timed out, the timer is reset and counts out another 300  $\mu$ sec. However, if no additional data has been loaded within this time, the part terminates the load cycle and starts the internal write. The preloaded page is written into the main array in a maximum of 10 msec. During this time, the device ignores any additional load attempts.

Data can be loaded into the page as fast as 350 nsec/byte. This is the time from the Write Enable (WE/) high to low transition to the next WE/ high to low transition. The short time between two writes simplifies microprocessor interfacing.

The first byte loaded determines the beginning of the page boundary. The 28C256 uses row addresses A6-A14 to determine the page boundary. Column addresses A0-A5 are used to address locations within the page. Once the page boundary is

		SOURCE STATEMENT	
INPUT	EQU	xxxxH	
OUTPUT	EQU	yyyyH	
NBLOAD	EQU	0zH	
	LHLD	OUTPUT	
	XCHG		: Load EE addr. into D reg.
	LHLD	INPUT	: Load Data addr. into H reg.
	LDA	NBLOAD	
	MOV	B,A	: load B reg. with the No. page byte write
RLOAD	LDAX	H	: load the data into reg. A
	STAX	D	: write the data into EE page
	DEC	B	
	JZ	RTMAIN	
	INC	H	
	INC	D	
	JMP	RLOAD	: load the next byte into EE
RTMAIN	POP		
	*		
	*		
	*		
	RET		

Figure 2: 8085 assembly language program subroutine to load a page. A 3-MHz 8085-based system can load only 9 bytes in 150  $\mu$ sec.

determined, the bytes within the page can be loaded in any order. The user can write into the same page location as many times as desired. Only the last byte loaded into a page location will be written into the main memory. While passing the page boundary (change in row addresses) is illegal, it will not affect the page contents, except for the byte pointed to by the column address. New data will be loaded into that location. Other locations will remain unchanged.

Only the bytes loaded are transferred to the EEPROM array. Bytes that were not loaded will not be written. The content of those locations in the memory array will remain unchanged. Consequently, endurance is conserved.

### Flexibility And Compatibility

Two write modes are available on the 28C256. The page mode is effective in applications with data block transfer requirements. In this mode, data must be transferred no slower than once every 300  $\mu$ sec/byte. However, in some applications, such as systems with a slow A/D converter, data transfer rates can be slower than 300  $\mu$ sec/byte, but faster than 2.5 msec/byte.

		SOURCE STATEMENT	
DESTADD	EQU	ES:BYTE PTR [DI]	
SRSADD	EQU	DS:BYTE PTR [SI]	
SRSOFF	EQU	xxxxH	
DESOFF	EQU	yyyyH	
INPUT	EQU	zzzzH	
OUTPUT	EQU	kkkkH	
NBLOAD	EQU	0XH	
	MOV	BX,INPUT	the first 6 instructions are used to set the reg. to point to EE addr. and data source addr
	MOV	DS,BX	
	MOV	BX,OUTPUT	
	MOV	ES,BX	
	MOV	SI,SRSOFF	
	MOV	DI,DESOFF	
	MOV	CX,NBLOAD	
	REP	MOVS DESTADD , SRSADD	: continue page load until CX reg. is equ. to zero
	POP		
	*		
	*		
	RET		

Figure 3: 8088 assembly language software routine to load a page. The software delay is not included.

To simplify page mode system design, an extended page load feature allows the designer to suspend the load cycle as long as desired. Since the internal 300- $\mu$ sec timer is reset on the leading edge of the WE/ signal, it remains reset as long as the WE/ pin is low, and the other two control pins (Chip Enable and Output Enable) are at their proper states. Once the WE/ signal has made a low to high transition, the timer starts counting. The load cycle suspension can be performed on any of the page's bytes, including the first.

There are some applications where minimum software changes are required when upgrading system memory from a 64K to a 256K bits. The byte mode feature of the 28C256 not only meets these requirements, but it also improves total write time.

The 28C256's byte write mode feature reduces write time, without any major software changes, by a factor of 4 over the 10-msec EEPROM. The part automatically enters this fast byte write mode when no additional bytes have been loaded after the first byte. It waits for a maximum of 500  $\mu$ sec before terminating the load cycle. The loaded data is then written into the main memory array in a maximum of 2 msec.

### **End Of Write**

To determine the end of write cycle, the 28C256's data polling feature can be used. Since a write cycle is typically completed in less than the specified time, a software routine can be used to poll data. If the part is still busy writing, a read will result in the inverted data of the last byte written. When the write cycle is completed, a read from the last address written will result in true data. Data polling is address independent while the part is still busy, and the timing is the same as the read timing.

When designing in the data polling feature, designers must consider the time delay between the last byte loaded into the page and the availability of valid data polling information. This delay time, which is page mode related, varies between manufacturers. Since an internal timer (300  $\mu$ sec) is reset upon a byte load after the last byte loaded into the page, data polling is not available immediately. On the 28C256, the maximum time from last byte loaded to valid data polling is 500  $\mu$ sec. Hence, the device cannot be polled for the duration of this time. Polling the part during this time will result in tri-state (i.e., indeterminate output).

Today, the 256K EEPROM is a reality, and with this reality comes the first standardization of basic features among EEPROM manufacturers. Refinements to the EEPROM page mode feature have eliminated the performance limitations of early page mode parts and, for the first time, the combination of both fast byte write and page mode in a single part give designers the best of both worlds. The high density, low power CMOS technology of these devices now makes it feasible for large EEPROM systems to replace core, EPROM, bubble, and battery-backed RAM.

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# $\mu$ Cs with on-chip EEPROM provide system adaptability

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*Single-chip  $\mu$ Cs with on-chip EEPROM bring versatility and security to many applications. The EEPROM's nonvolatile storage especially suits data logging, and its remote programmability makes it the best choice for program storage in embedded applications. And you can use adaptive code to implement self-modifying machines.*

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Larry Goss and Mark Bagula,  
Seeq Technology Inc

Advances in EEPROM technology make it a viable candidate for program-storage on single-chip microcontrollers. Given the improvements in write-voltage requirements (5V rather than 21V) and lifetime (1 million read/write cycles instead of 10,000), EEPROMs are now competitive with other nonvolatile memory technologies, such as ROMs, EPROMs, and battery-backed RAMs.

On-chip EEPROM allows you to reprogram both code and data in circuit—a desirable feature in applications where there's a need to adapt to changing requirements—while maintaining complete security. In addition, on-chip EEPROM provides the advantages found in

systems that employ separate EEPROM and  $\mu$ P chips. Such advantages include data logging, configuration-parameter storage, and self-adaptive, nonvolatile code implementation.

The ability to implement self-adaptive code is perhaps the most interesting benefit. When the on-chip processor has a special write-to-program-memory instruction, EEPROM allows you to create adaptive algorithms that are impossible to develop with ROM or volatile control memory. Typically, this exercise involves the modification of look-up tables for self-calibration. In more sophisticated systems, the microcontroller with on-chip EEPROM can act as a long-time-constant filter to accommodate very slowly changing variables, such as wear of mechanical parts, drift in analog circuits, or seasonal changes that can affect operation. For example, the CPU could reliably maintain a 3-month rolling average of certain input variables, because this data will not be lost even if you remove the processor chip for servicing. Best of all, the processor can maintain the averages and perform other tasks automatically under software control, because it can write to EEPROM as if it were nonvolatile RAM.

When you're producing your system in very high volumes, it makes economic sense to implement only a portion of program code in EEPROM; using mask ROMs or EPROMs to hold the bulk of the necessary code can save money. In fact, you can use the 72720 with external ROM/EPROM in such cases.

However, this lower cost scheme exacts a penalty—a

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*On-chip EEPROM allows you to reprogram both code and data in circuit while maintaining complete security.*

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reduction in device and system flexibility. You can store initialization constants and accomplish some limited data logging with this approach, but if you desire in-circuit (or remote) reprogrammability, you must make some careful decisions about which code should reside in ROM and which in EEPROM.

The first issue to consider is what portion of the application program will be extensively modified during the life of the system and whether these changes

can benefit from an in-circuit reprogramming capability. Configuration parameters and look-up tables are examples of code that generally should reside in on-chip EEPROM. Any code that remains relatively static during the life of the system (debugged executable code, for example) can reside in mask ROM.

The second consideration involves code and data security. When you substitute external mask ROM or EPROM for on-chip EEPROM, you create a vulnerable

### The inside story

The 72720 is a single-chip  $\mu$ C with an integral  $2k \times 8$ -bit EEPROM. You can use the processor itself to erase and program the EEPROM, or you can program it under external control. In addition, expansion modes allow you to add external EEPROM easily.

Two programming modes are available: slave and CPU controlled. In the slave mode, the application of address, data, and read/write strobes allows you to program the 72720 like a standard EEPROM or EPROM. As a result, you can program the 72720 externally with standard PROM programmers, or in circuit with a master processor.

In the second mode, a PRG instruction uses any 16-bit register pair to program an EEPROM location. The design of the 72720's external read/write logic also allows you to program external EEPROM with the same instruction. This capability allows you to readily expand off-chip memory without affecting system software or timing.

In addition to the programming modes, the 72720 offers some expansion modes. The peripheral expansion mode, ac-

cessed as part of a 256-byte peripheral file, allows you to place all external ports and peripherals on an expansion bus that consists of port C, which acts as an 8-bit address bus, and half of port B, which provides the necessary address latch and read/write control lines. As a result, these ports use the same instructions and bus timing as the on-chip peripherals.

The full expansion mode uses the same scheme to support external devices, but it adds lines (dedicated to port D) to provide

the additional address lines necessary to gain access to the full 64k-byte address space.

To provide code and data security, a software-activated option locks the processor in single-chip mode to prevent external access to proprietary programs. Once it's set, this lock can only be reset by an external EEPROM block-clear operation that erases the entire memory. However, the processor still has read/write access to all internal memory locations (including EEPROM).

### 72720 PIN VOLTAGES

MODE	PIN VOLTAGES AT RESET				I/O CONTROL REGISTER	
	MODE CONTROL	B2'	A	A7	BIT 7	BIT 6
SINGLE CHIP	0V				0	0
PERIPHERAL EXPANSION	0V				0	1
FULL EXPANSION	0V				1	0
MICROPROCESSOR	12V	0V	5V	0V		
SLAVE PROGRAM EEPROM	5V		0/5V	5V		
BLOCK CLEAR EEPROM	12V	5V	5V	5V		

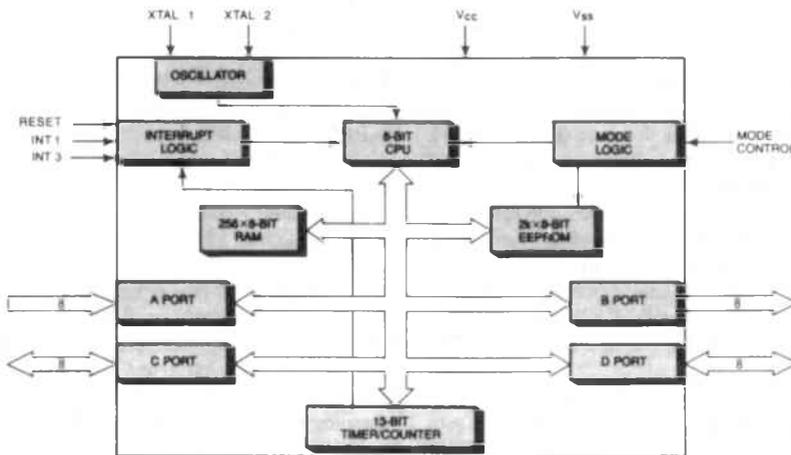
\*PIN B2 SHOULD BE DRIVEN THROUGH A 5-K $\Omega$  RESISTOR  
NO ENTRY INDICATES DON'T-CARE STATE

memory system. You can easily decipher the contents of a mask ROM, for example, because you can visually determine its patterns after opening the chip. Any code stored externally is visible to any casual observer who monitors the data lines between the processor and memory.

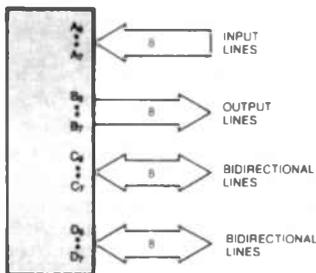
On the other hand, instructions do not appear on the processor's I/O pins when all program codes exist on chip. This arrangement renders the code invisible.

Furthermore, when the processor fetches instructions only from on-chip memory, you have no external way to instruct the processor to dump the contents of internal registers or memory locations.

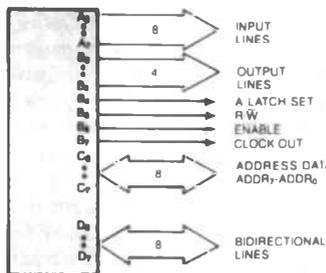
Implementing a microcontroller's entire program code in on-chip EEPROM whenever possible provides the same benefits as on-chip EPROM (easy prototyping), and the EEPROM doesn't require a quartz window for erasing. In addition, you won't have to remove



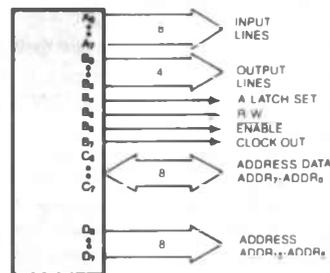
SINGLE-CHIP MODE



PERIPHERAL EXPANSION MODE



FULL EXPANSION MODE



*This full-function, single-chip  $\mu$ C, the 72720, features an integral 2k x 8-bit nonvolatile EEPROM. Available expansion modes significantly increase device flexibility.*

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*When you plan to produce your system in very high volumes, it makes economic sense to implement only a portion of program code in EEPROM.*

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the chip to reprogram it. You can also use any portion of the EEPROM not used for program code storage as slow-write/fast-read nonvolatile data memory for storing constants or logging data.

#### **Factor in the disadvantages**

EEPROM has one major disadvantage when compared with ROM or EPROM—high cost. However, this disadvantage diminishes somewhat when you take reprogramming time and inventory costs into account. You can reprogram an EEPROM much more quickly than you can an EPROM, and the ability to reprogram means you don't have to replace whole parts—as you do when you employ ROMs—when you need to implement system changes.

Compared with RAM devices, EEPROMs have another disadvantage, hinted at earlier: a relatively slow write time. Write-cycle times for current EEPROM devices range from 1 to 10 msec, while write-cycle times are typically 200 nsec for dynamic RAMs and 55 nsec for static RAMs. This long writing time limits the amount of data that can be stored when the power fails.

Despite these disadvantages, on-chip EEPROM can be very beneficial. To better understand the adaptability of single-chip  $\mu$ Cs with on-chip EEPROM, consider the following design examples, which employ the 72720 microcontroller.

The 72720 is a single-chip microcontroller that's capable of implementing self-adaptive algorithms. You can erase and reprogram its 2k-byte on-chip EEPROM using the processor itself, or you can treat the EEPROM as if it were a standard memory device and program it under external control. Expansion modes allow you to add external EEPROM easily, so you can expand programs and data when necessary.

#### **Simplifying PROM programmer design**

Universal PROM programmers often need new programming algorithms for each PROM adapter. Conventional approaches either store the programming algorithm in a PROM housed in the adapter itself, or they require that the user insert PROMs with the new algorithm in the main programming unit.

Using a 72720 microcontroller with 2k bytes of on-chip EEPROM simplifies the design. A program in the EEPROM directs the CPU to communicate with a host computer through an RS-232C link. The EEPROM also contains time delays and PROM programming utilities for address and data manipulation. Another routine in the EEPROM holds the instructions that control the

actual data transfer from the host to the target PROM. This approach allows you to change parameters and programming algorithms easily.

When downloading a new algorithm from the host into the on-chip EEPROM, the 72720 operates in peripheral-expansion mode and initially configures ports B, C, and D for simple output to control the programmer (Fig 1). It then stores the first 64 bytes, received serially from the host via one line of the A port, in internal registers. The A port is always configured as input. The 72720's 256-byte RAM buffers downloaded data, and this data is then written into on-chip EEPROM whenever the baud rate of incoming data is faster (>600 baud) than the EEPROM write cycle.

#### **Transfer to EEPROM is efficient**

The 72720 can transfer data from the buffer to its EEPROM very efficiently using its PRG program instruction. PRG stores the Accumulator Indirect instruction with slower-than-normal timing to accommodate the EEPROM. Stored data is placed in the accumulator, and any register pair in the on-chip RAM can serve as an address pointer.

The complete update procedure repeats for remaining data plus any additional downloaded code segments. With each new algorithm, the host supplies a jumpable address so that the 72720 will know where to begin executing as a particular device is selected for programming. Because the EEPROM is nonvolatile, you only have to download each programming algorithm once.

To program a PROM, the host merely sends the destination address and data to the universal programmer through the serial link. The 72720 stores the data in a 4k $\times$ 8-bit RAM buffer. It then transfers this data to the PROM in the device adapter by executing the related program stored in the on-chip EEPROM.

The ability to reprogram code and data at will makes systems more adaptable and easier to use. For example, custom programming protocols allow you to configure a dumb CRT terminal to suit your specific needs.

Fig 2 shows a keyboard-controller circuit that you can implement in any CRT terminal design. It uses the 72720 to convert the normal ASCII character transmitted for a particular keystroke into a sequence of ASCII characters that have been stored in EEPROM. Although the EEPROM is initialized to supply a single-character equivalent to the original keyboard character, you can program it with any multiple command sequence required by a particular software package.

The use of EEPROM offers an important benefit: You can develop command sequences while the terminal is being used in a transparent learn mode. The terminal requires no external modifications to the keyboard to implement this scheme.

To set the learn mode, simply type "control-clear" to store new response strings in EEPROM. The first keyboard combination entered identifies the new string and is not transmitted to the CPU. However, subsequent keystroke combinations are both sorted and transmitted for action. To terminate the learn mode, simply depress the delete key.

EEPROM availability is the only limiting factor on the number of ASCII codes that you can generate with a single keystroke. The 72720 provides 2k bytes for storing programs and the tables that can translate keystrokes. You'll need about 512 bytes for the keyboard scanning and translation routines and about another 256 bytes to hold the look-up table for the single-keystroke translations. The remaining memory locations can act as a series of pointers to the 256-byte table that holds the key codes you want to transmit.

The size of the transmitted key sequence determines the number of storable sequences. For example, you can store 16 key sequences in 256 bytes if each key sequence is 16 characters long. Any delimiter character—attached to the end of each key sequence if you require variable-length sequences—will obviously reduce the number of storable sequences. However, you can easily add external EEPROM to the 72720 if necessary.

To see how the keyboard controller actually operates,

look at the sequence required to execute a Basic interpreter. First, you simultaneously enter "control-clear" to effect the learn mode and "control-2" to set the identifier string. You then, in order, type "basic," hit the carriage return, and depress the delete key to terminate the learn mode. Because the "basic" string is transmitted as it's entered, Basic should be running when you perform the subsequent actions. To run Basic in the future, you simply enter "control-2"; this action will transmit the "basic-carriage return" string to the CPU.

A disabled mode (entered by typing the "clear" and "repeat" keys simultaneously) allows the terminal to operate without any key redefinition. The enabled mode overrides the previous mode to intercept each keystroke combination stored in the corresponding EEPROM locations. You enter this mode by depressing the "control" and "repeat" keys simultaneously while the terminal is displaying the data actually received (either the transmitted character sequence or the CPU response).

This controller scheme can also support multiple users (each using a different set of custom key sequences) on the same terminal. For example, several operators sharing a word processor can use some of the stored key sequences as a unique ID number. Each operator can reconfigure the keyboard to suit specific needs and make the configuration parameters inaccessible to unauthorized users.

You can also develop self-adaptive routines to compensate for different levels of user proficiency. For example, the processor can monitor the operator's

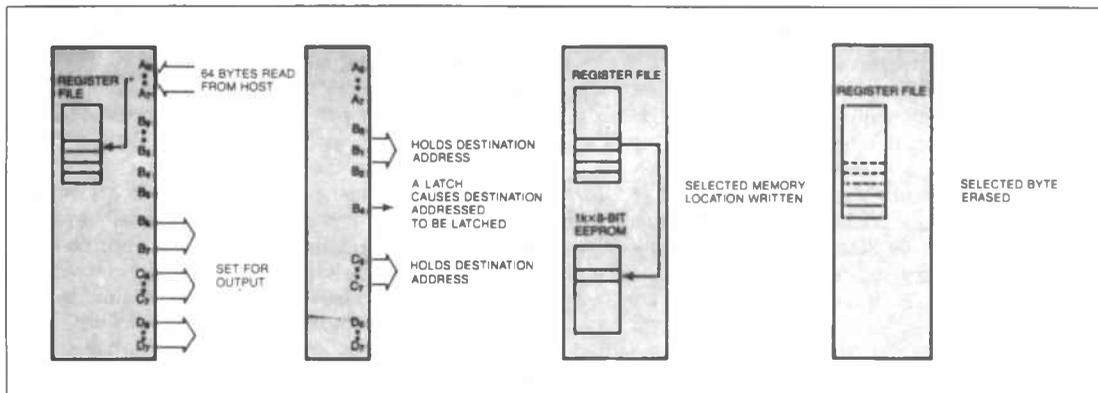


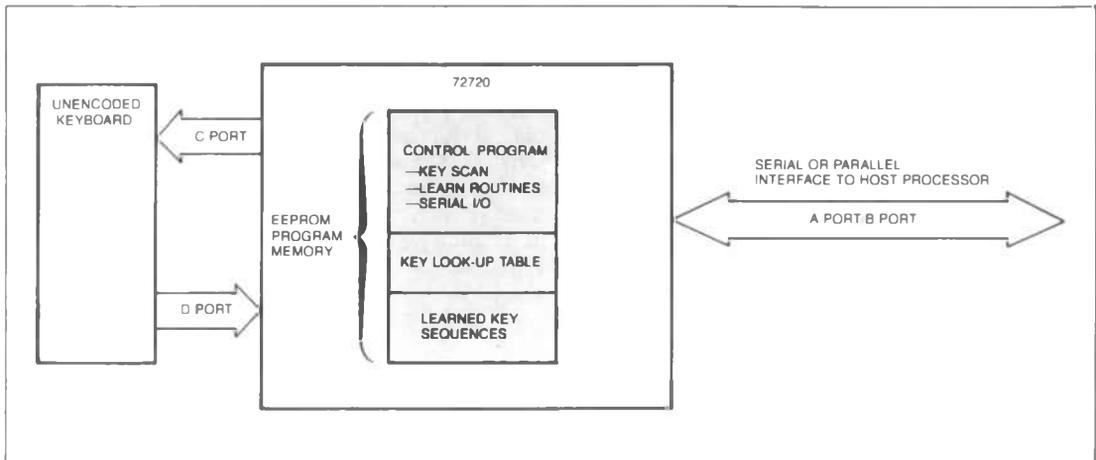
Fig 1—To download a new algorithm into its on-chip EEPROM, the 72720 microcontroller initially configures ports B, C, and D for simple output service to control the programmer. Via one line of the A port, it then stores the first 64 bytes from the host in internal registers.

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*The 72720 can efficiently transfer data from the buffer to its EEPROM using its PRG program instruction.*

---



*Fig 2—In this keyboard-controller circuit, the 72720 converts the normal ASCII character transmitted by a particular keystroke into a sequence of ASCII characters that have been stored in EEPROM.*

typing speed and accordingly adjust the n-key rollover algorithm that determines the number of adjacent keys the processor will recognize when those keys are depressed simultaneously. As a result, beginning operators don't have to worry about typing mistakes during the learning process. On the other hand, the program will allow expert operators to type at a much faster speed.

#### **EEPROM stores diagnostic information**

The ability to intercept keystroke combinations is only one data-logging application. With its ability to support remote programming, a single-chip microcontroller that includes on-chip EEPROM can be a powerful troubleshooting tool.

When functioning as a diagnostic processor, the microcontroller can monitor a system and record in EEPROM any errors that occur before the system fails. You can then execute diagnostic programs from on-chip memory, or download them from a remote host CPU that uses the results stored in the EEPROM to pinpoint the exact problem. You can also use the downloading capability to upgrade existing on-chip diagnostic routines. This flexibility increases the effectiveness of on-site repairs, because service personnel will have immediate access to the diagnostic information stored in the EEPROM when they arrive at the site.

In addition, the on-chip EEPROM can store product warranties, configuration information (serial numbers,

revision history, and special options), and service records for easy reference. In fact, the diagnostic processor can detect product misuse and void the on-chip warranty information if necessary.

#### **Data logging and storage on chip**

Fig 3 shows the 72720 acting as a diagnostic processor for a computer system. In this example, on-chip and external EEPROM provide a data-logging function and also store the diagnostic routines and other application programs. This particular configuration is closely coupled to the system under test via a bus-activity monitor (composed of random logic or gate arrays) to synchronize the 72720 with the transactions occurring on the address, data, and control lines.

When it's functioning as a dynamic refresh controller, the 72720 looks for potential errors by processing the error-checking and -correction codes (CRC or Hamming) generated for the various data transactions that occur to and from memory. During refresh operations, the 72720 can also correct any single-bit soft errors it detects. It can also tally the number of uncorrectable soft errors and issue a message to the host computer if the number of warnings reaches a critical threshold.

This tightly coupled design provides the ability to discover and correct errors that occur on single bus transactions. This scheme does have some disadvantages, however. For one thing, the interface logic is somewhat complex. More important, the scheme will

*The ability to reprogram code and data at will makes systems more adaptable as well as easier to use.*

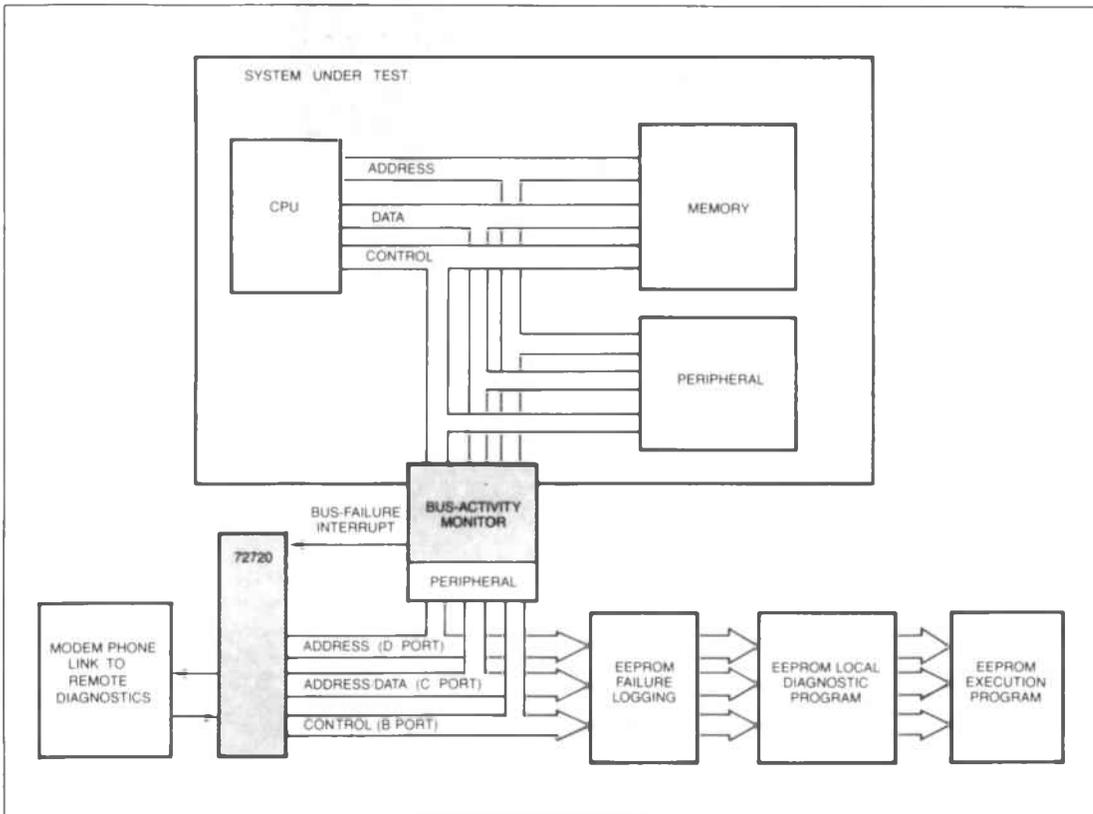
slow bus transactions if diagnostics are not handled as background tasks, because the diagnostic processor will have to make more computations on the fly to correct errors on a cycle-by-cycle basis.

#### Loose coupling would speed operation

A more loosely coupled approach would forego the bus-activity-monitoring logic altogether and have the 72720 act as a CPU peripheral that would request the host to schedule diagnostic routines to run in background mode. The results could be stored in the error-logging portion of the on-chip EEPROM and transmitted to a remote service facility. Such an approach would be very useful for monitoring the operations of other CPU peripherals, such as disk drives and printers.

The loosely coupled scheme does more than reduce the complexity of the diagnostic processor. For example, it has no effect on bus transactions, because diagnostic programs are scheduled as a user task. Unfortunately, the loosely coupled approach cannot pinpoint exact problem sources, because it is collecting and processing large amounts of data in a timeshared fashion. You'll have to provide some extra logic (similar to that required in a tightly coupled processor) to allow the loosely coupled processor to take an active role in diagnosing and correcting errors. To take corrective action, you will also have to provide the means to interrupt the host processor.

Either scheme can take advantage of an EEPROM's self-adaptive capabilities, allowing the 72720 to antici-



**Fig 3—***Operating as a diagnostic processor, the 72720 can monitor a system and record any errors that occur prior to system failure. This particular configuration is closely coupled to the system under test via a bus-activity monitor, so the 72720 is synchronized with the transactions occurring on the address, data, and control lines.*

pate potential failures and take corrective action. For example, if you were to set up the 72720 as a memory controller, it would be able to determine when the number of soft errors reaches a critical threshold (by interrogating its error log) and map out those locations before the errors prove fatal.

To realize either scheme, you must have a good understanding of the system under test, so that you can program the scenarios (and their corresponding response) into the processor in advance. The exact parameters that determine each action will obviously depend on the specific application. **EDM**

---

### Authors' biographies

*Larry Goss is strategic marketing manager for microcomputers at Seeq Technology Inc (San Jose, CA). With the company three years, he was previously a field applications and product marketing engineer at Intel Corp. He has a BSEE degree from the University of Maine, and he lists photography as his hobby.*



*Mark Bagula is design manager of microproducts at Seeq Technology Inc. He directs the development of microcomputers, communications circuits, and ASIC designs. Mark has a BSEE degree from USC, has been granted a patent for a bus protocol, and is a member of the IEEE. In his spare time, he enjoys stamp collecting, gardening, graphic arts, and working on hot rods.*



# EEPROM Programs in a Flash

by Samba Murthy, Seeq Technology, San Jose, CA

he in-circuit erasability and programming features of flash EEPROMs clearly benefit the systems designer. Unlike UV EPROM parts that take 20 to 30 minutes to erase under UV light, flash EEPROMs erase in 20 seconds. Programming time for EEPROMs is 32 seconds versus 2 minutes for a UV counterpart. Further, UV devices must be removed from their sockets for each erasure, while EEPROMs can be soldered directly to the circuit board for improved contact reliability. Flash EEPROMs allow easy implementation of in-circuit changes to nonvolatile program and data storage.

Although the EEPROM read operation is similar to that of UV parts, the write operation is not. Since the write time per byte is 2 msec, there is an intrinsic timing difference between the memory and a microprocessor. Additional hardware is necessary to accommodate these timing differences.

Different approaches exist for microprocessor interfacing. One technique is to use a dedicated controller to take care of the write/erase operations independently of the microprocessor. The microprocessor can then run independently of the flash EEPROM controller during chip erase or write time. In a second approach, the microprocessor can be dedicated to the flash EEPROM chip erase/write operation. The two distinct interface approaches dictate the amount of hardware and software required to interface the flash EEPROM to the microprocessor. Information transfer efficiency depends on the type of interface approach taken.

The second approach is acceptable in many applications where erase/write is infrequent. This technique is easy to implement and does not require any software overhead in terms of I/O polling or

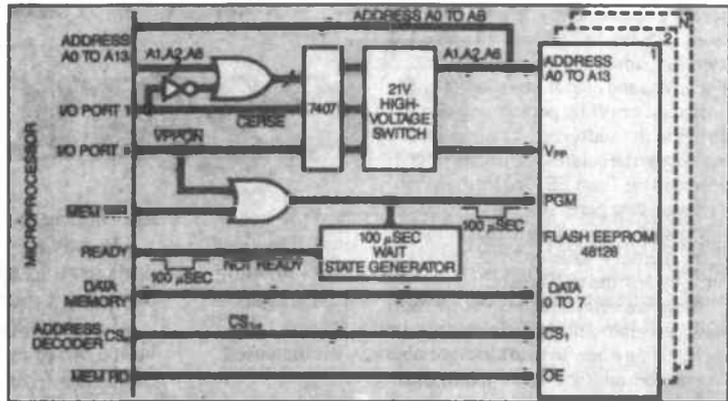


Figure 1: In this flash EEPROM microprocessor interface, both bus timing and software timing are used to gate the control signals to a microprocessor bus. The  $V_{PP}$  and chip erase high-voltage switches can be turned on or off through the processor's dedicated I/O ports. Alternatively, logic gates (and latches) can be employed, with dedicated memory addresses assigned for the switches.

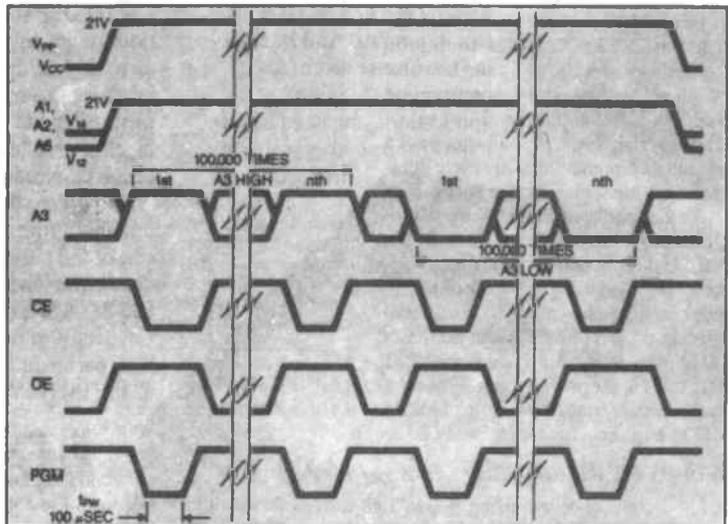


Figure 2: Chip erase on the flash EEPROM is accomplished by raising  $V_{PP}$  to high voltage (21V) with /OE held at a TTL high level. Address pins A1, A2 and A6 must also be set to high voltage. Wait states are inserted in the processor's write cycle to stretch /PGM active width to 100  $\mu$ sec. The erase cycle is then started by selecting the chip with /CE and pulsing /PGM. For complete erasure, the effective /PGM width should sum up or equal 10 sec each with A3 high and low, alternately.

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interrupt servicing. The scheme can be implemented by using the microprocessor's ready line. In this case, wait states are inserted in the microprocessor's cycle for as long as necessary to complete the chip erase or write operation.

Both bus timing and software timing are used to gate the control signals in the flash EEPROM interface to the microprocessor bus. Figure 1 depicts the control interface. The  $V_{pp}$  and chip erase high-voltage switches can be turned on or off through the processor's dedicated I/O ports. Another option is to use logic gates along with latches, and assign dedicated memory addresses for the switches. Then,  $V_{pp}$  and chip erase switches can be turned on or off by performing dummy writes to the addresses. The processor's memory write control line should be connected to the flash EEPROM/PGM pin. The wait state generator uses the microprocessor's ready line to insert wait states in the memory write cycle to extend the write cycle time to 100  $\mu$ sec.

There are several techniques to insert wait states into a microprocessor's write cycle. Using a one-shot or a retriggerable monostable multivibrator is a convenient approach. The one-shot's pulse output is used to negate the processor's READY line, thus inserting wait states into the write cycle. It is important to ensure that the RC time constant used to time the pulse output is temperature compensated. The flash EEPROM 48128 from Seeq Technology specifies a minimum pulse width of 90  $\mu$ sec and a maximum pulse width of 120  $\mu$ sec for the /PGM signal during write. Thus, the one-shot design should ensure that the write cycle duration does not violate device specs.

An alternative to the one-shot is a programmable digital timer, such as the 74LS294. The count modulo can be digitally controlled using the inputs provided. For example, using a 5-MHz clock, programming for  $2^9$  will give a period of 102.4  $\mu$ sec. Using this signal as the "NOT READY" to the processor, the write cycle time of /PGM width can be extended to a minimum of 102.4  $\mu$ sec. This satisfies the 48128 write specifications for /PGM width.

### Flash EEPROM Chip Erase/Write

Chip erase is done by raising  $V_{pp}$  to high voltage (21V) with /OE held at a TTL high level (Figure 2). Address pins A1, A2 and A6 must also be brought to a high-voltage level. The erase cycle is then started by selecting the chip with /CE and pulsing /PGM. During the erase cycle it is necessary to control address A3. Dummy writes to any two address locations can be per-

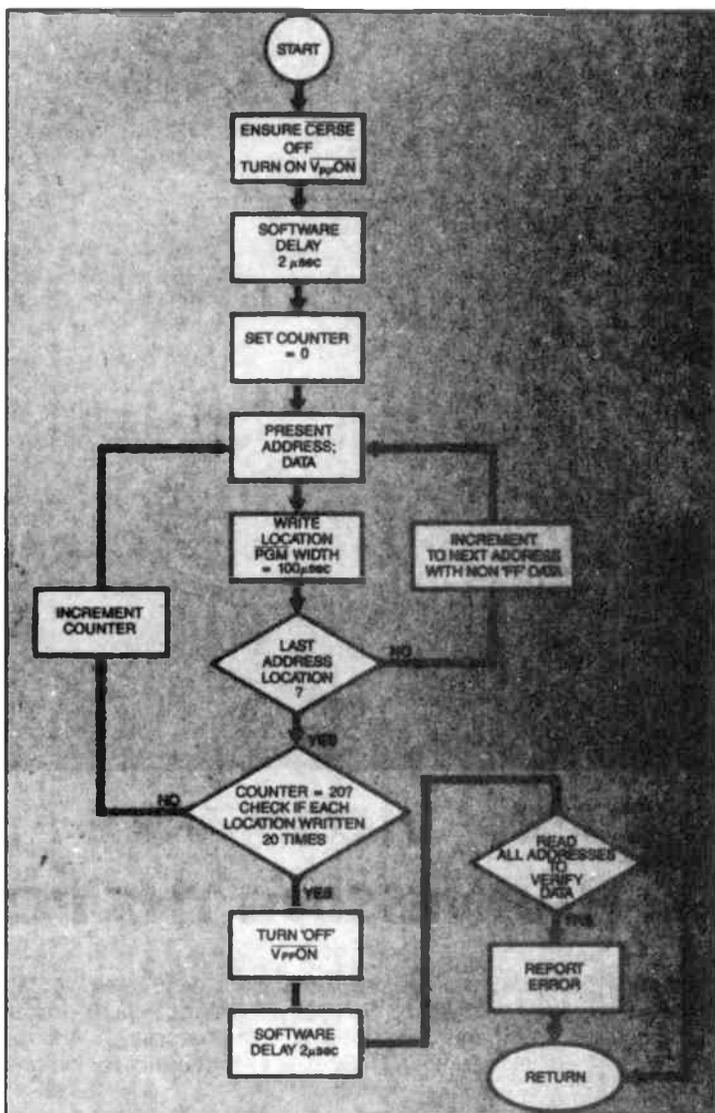


Figure 3: Flash EEPROMs allow easy implementation of in-circuit changes to nonvolatile program and data storage. Once the chip is fully erased, the flash EEPROM can be written by applying a high voltage to the  $V_{pp}$  pin (21V). Pulsing /PGM after presenting valid data at the inputs starts the write cycle. Write time can be optimized by only writing to those address locations in which data will be changed from the erased FF state. The cycle is repeated 20 times for all addresses to be programmed. Software delays are needed to satisfy setup and write/erase recovery times for the 48121 flash EEPROM.

formed to toggle A3 for chip erase; one with address bit A3 high and a second with A3 low. For example, the addresses can be 00FF hex and 00F7 hex. Wait states are inserted in the processor's write cycle to stretch /PGM active width to 100  $\mu$ sec. For complete erasure, the effective /PGM width should sum up or equal 10 sec each with A3 high and low, alternately. This can be achieved by repeating the 100  $\mu$ sec writes 100,000 times twice; first with address A3 high and then low.

Once the chip is fully erased, the flash EEPROM can be written by applying a high voltage (21V) to the  $V_{pp}$  pin. /OE should be held high. /CE then selects the device. Pulsing /PGM after

presenting valid data at the inputs starts the write cycle. A 100- $\mu$ sec write cycle is performed with the data and address for each memory to be programmed. This process is repeated 20 times for each memory location to be programmed. The /PGM low pulse width(s) should equal 2 msec for a successful byte write. Processor time can be saved by only writing to those address locations in which data will change from the erased state (FF hex).

The 2- $\mu$ sec delays shown in the software flowchart (Figure 3) are needed to satisfy the  $V_{pp}$ , chip erase (A1, A2 and A6) setup times and write/erase recovery time of the 48128 flash EEPROM. Other timing requirements of the flash EEPROM, like the address, data, /CE and /OE setup times, are satisfied using hardware techniques. The techniques outlined here use general control signals to permit adaptation to any microprocessor system's bus.

For in-circuit erase/write,  $V_{pp}$ , A1, A2 and A6 switching is key to the microprocessor interface. This necessitates that high-voltage signals be actively present in the microprocessing environment. The high-voltage signals are dynamic and need to be controlled over a wide temperature range. To generate the high-voltage pulses required for  $V_{pp}$ , A1, A2 and A6, a power supply with a capacity to supply output voltages up to 24V is needed. In a system environment where this voltage is not available, a dc-to-dc switching regulator can be used to convert 5V to 21V. The high-voltage circuit drivers for  $V_{pp}$  and chip erase (i.e., A1, A2 and A6) can be built using a high-voltage open collector buffer like the 7407 and a transistor like the 2N2222A for the high-voltage switch. Care should be taken during the high-voltage driver design to minimize overshoots.

Microprocessor system environments demand the capability to connect multiple devices. The 48128 flash EEPROM can be deselected using /CE during erase/write. Hence, from a system perspective,  $V_{pp}$  and chip erase (A1, A2 and A6) can be bused to multiple devices in the system. Using TTL-level control of only /CE, any flash EEPROM device can be selectively erased or written. This allows for control of multiple flash EEPROMs in the system. It should be noted that the  $V_{pp}$  and chip erase switches should supply the standby current of the deselected devices in addition to the selected device being programmed. The result is a design with only one  $V_{pp}$  and chip erase switch for the entire flash EEPROM memory array. As an option,

$V_{pp}$  can be tied to 21V, eliminating the need for a  $V_{pp}$  switch. The flash EEPROM interface described uses both hardware and software timing for chip erase and programming. An important point to keep in mind is that the trade-offs between hardware and software timing are system-dependent. **ESD:**

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# 8

## ***GENERAL INFORMATION***



# Thermal Resistance of SEEQ Products

March 1987

LEAD COUNT	PACKAGE TYPE	$\theta_{JA}$ (C/WATTS)	$\theta_{JC}$ (C/WATTS)
20	CERDIP (300 MILS)	60	22
	PLCC	60	UE
24	CERDIP (600 MILS)	58	21
	PLASTIC DIP (600 MILS)	49	UE
28	CERDIP (600 MILS)	45 – 55	21
	PLASTIC DIP (600 MILS)	40 – 50	UE
32	LCC	50 – 65	18
	PLCC	58	UE
40	CERDIP (600 MILS)	42	18

**NOTES:** 1. Actual Thermal Resistance of a given device may vary from the value on the table, this table contains the representative values for the package types specified.

2. All plastic package data refers to CU leadframe material.

3. All values are for socketed units.

4. UE = Under evaluation  
LCC = Leadless Chip Carrier  
DIP = Dual-In Line Package  
PLCC = Plastic Leaded Chip Carrier

## Packaging Information

### SEEQ Plastic Packages Incorporate:

- High thermal conductivity copper leadframe.
- Silver-filled epoxy die attach material.
- Gold bond wires.
- Low stress, moisture-resistant molding compound.

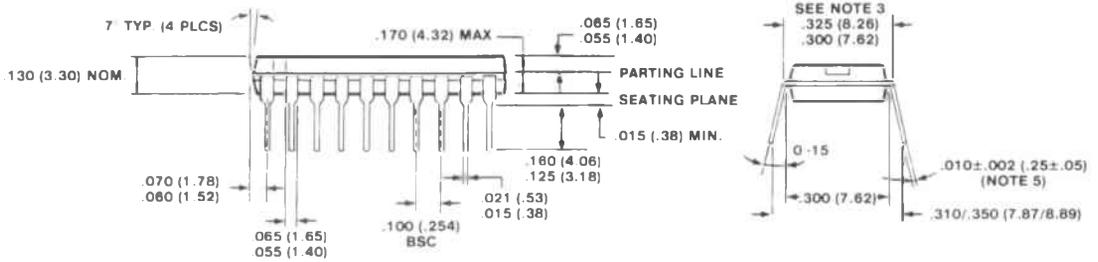
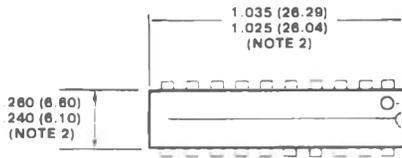
### SEEQ Cerdip Packages Incorporate:

- Thermal conductivity Alumina substrates.
- Gold Silicon Eutectic die attach.
- Alloy 42 leadframe.
- Aluminum bond wires.

GENERAL  
INFORMATION

# PLASTIC DUAL-IN-LINE PACKAGES

## 20 LEAD PLASTIC PACKAGE TYPE P

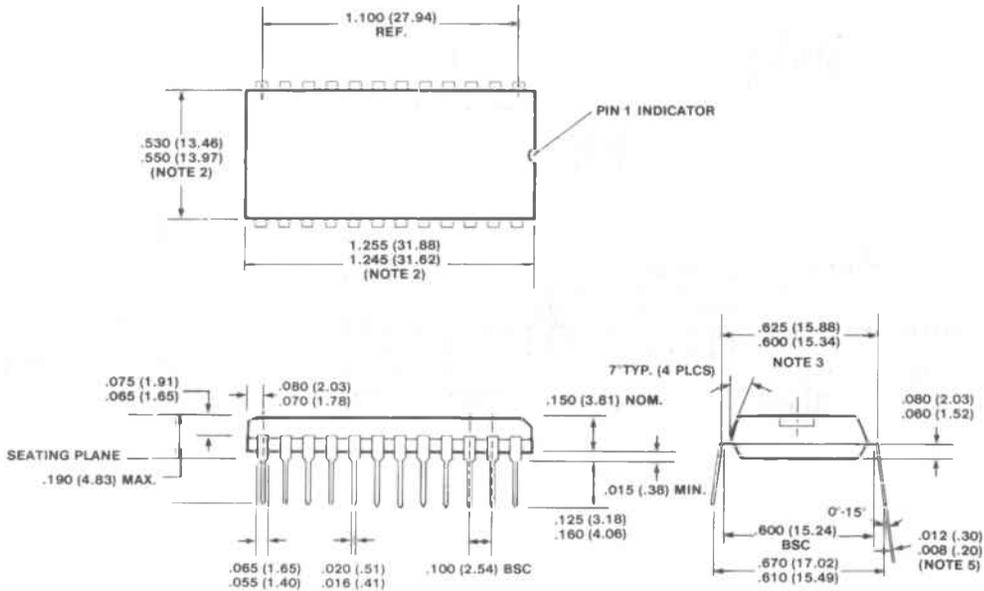


### NOTES

1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are ± .010 (.25) unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

# PLASTIC DUAL-IN-LINE PACKAGES

## 24 LEAD PLASTIC PACKAGE TYPE P



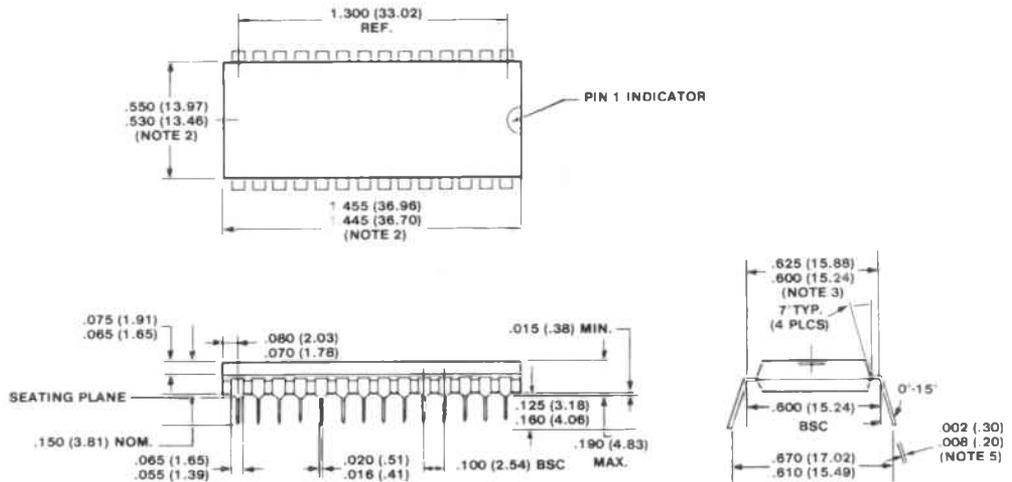
### NOTES

1. All dimensions are in inches and (millimeters)
2. Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder
4. Tolerances are  $\pm .010 (.25)$  unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max

GENERAL  
INFORMATION

# PLASTIC DUAL-IN-LINE PACKAGES

## 28 LEAD PLASTIC PACKAGE TYPE P

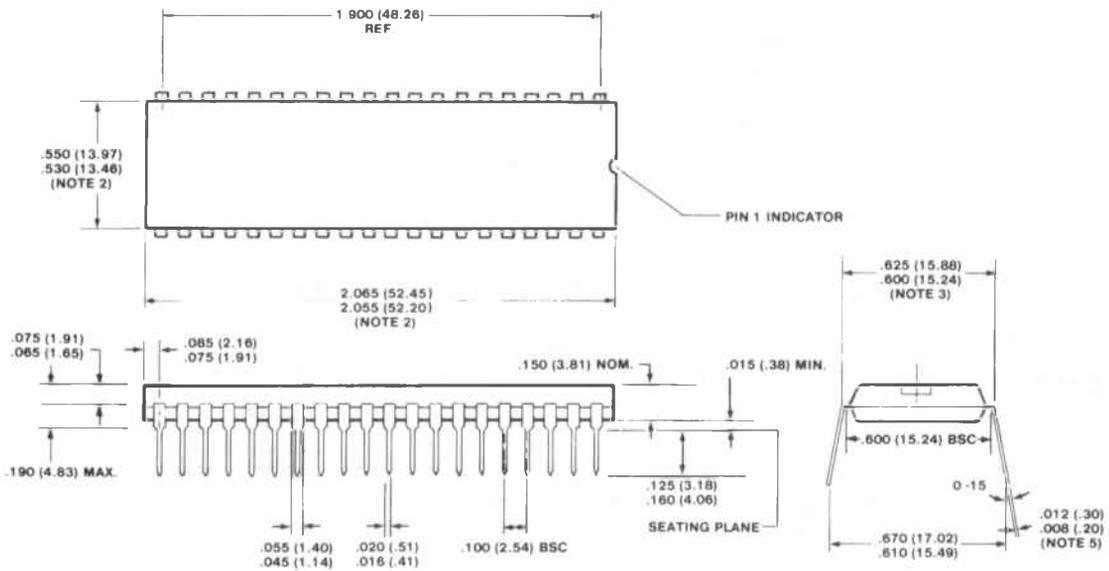


### NOTES

1. All dimensions are in inches and (millimeters).
2. Dimensions do not include mold flash. Max. allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are  $\pm .010 (.25)$  unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

# PLASTIC DUAL-IN-LINE PACKAGES

## 40 LEAD PLASTIC PACKAGE TYPE P

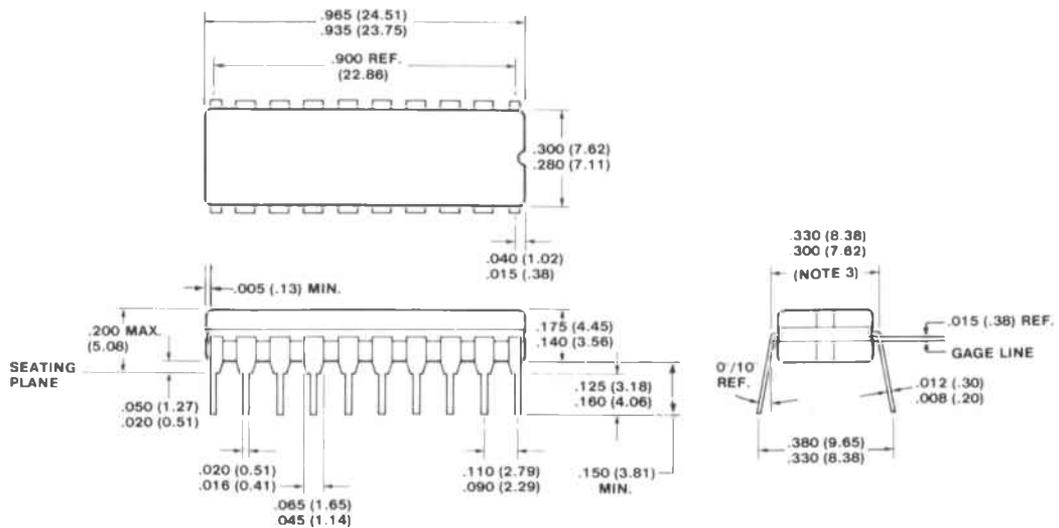


### NOTES

1. All dimensions in inches and millimeters.
2. Dimensions do not include mold flash. Allowable mold flash is .010 (.25).
3. Dimension is measured from shoulder to shoulder.
4. Tolerances are  $\pm .010 (.25)$  unless otherwise specified.
5. For solder dipped leads, thickness will be .020 (.51) max.

# CERAMIC DUAL-IN-LINE PACKAGES

## 20 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D

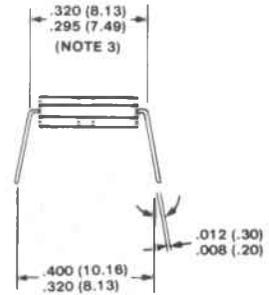
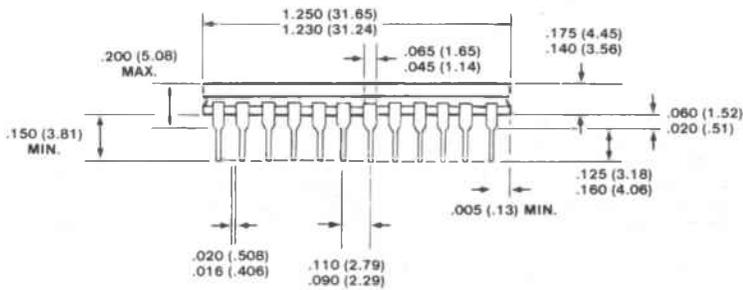
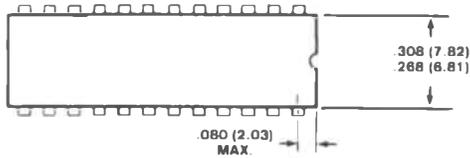


### NOTES

1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters)
3. Dimension is measured from outside shoulder to shoulder. This complies with Mil-M-38510, Appendix C, Dimension E<sub>2</sub> on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .290 (7.37) max. .320 (8.13).

# CERAMIC DUAL-IN-LINE PACKAGES

## 24 LEAD HERMETIC SLIM CERAMIC DIP PACKAGE TYPE D

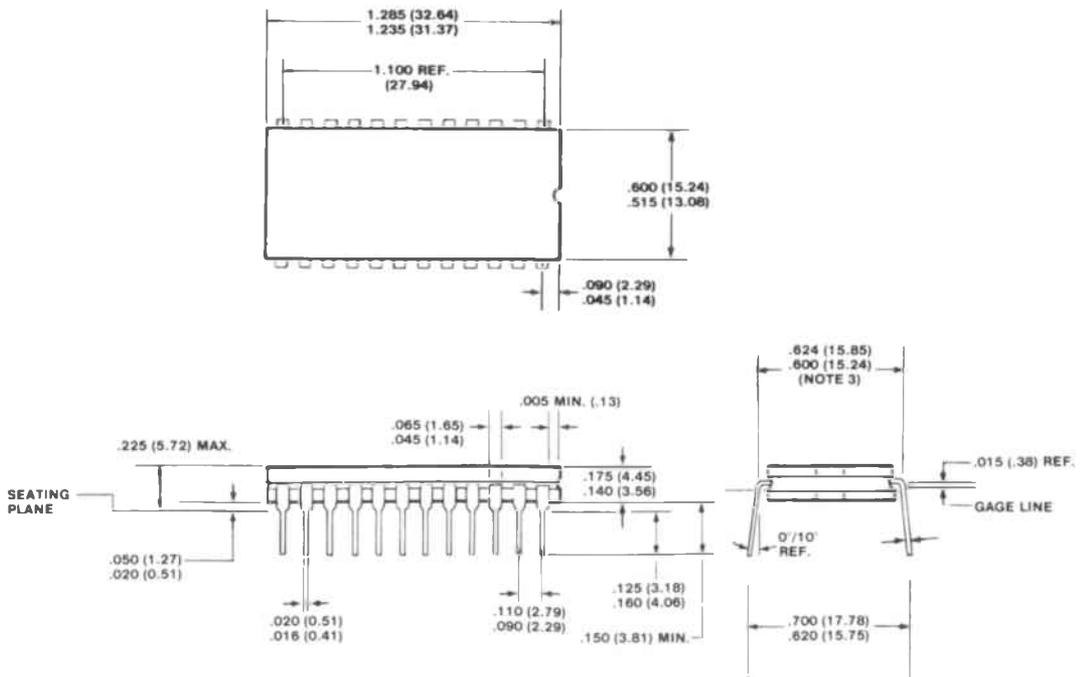


### NOTES

1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters).
3. Dimension is measured from outside shoulder-to-shoulder. This complies with MIL-M-38510, Appendix C, Dimension E<sub>2</sub> on D outline which measures from center of shoulder-to-shoulder per section 50c min. .280 (7.37) max. .320 (8.13).

# CERAMIC DUAL-IN-LINE PACKAGES

## 24 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D

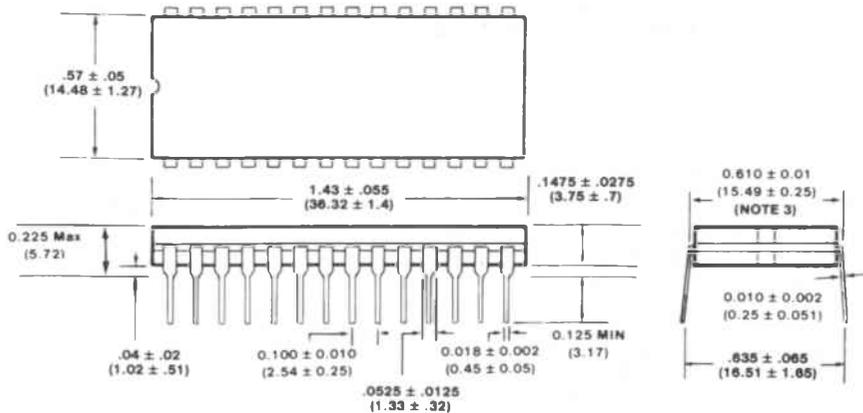


### NOTES

1. All dimensions in inches and (millimeters).
2. For solder dipped leads, thickness will be .020 (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with MIL-M-38510, Appendix C. Dimension E<sub>2</sub> on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

# CERAMIC DUAL-IN-LINE PACKAGES

## 28-LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D

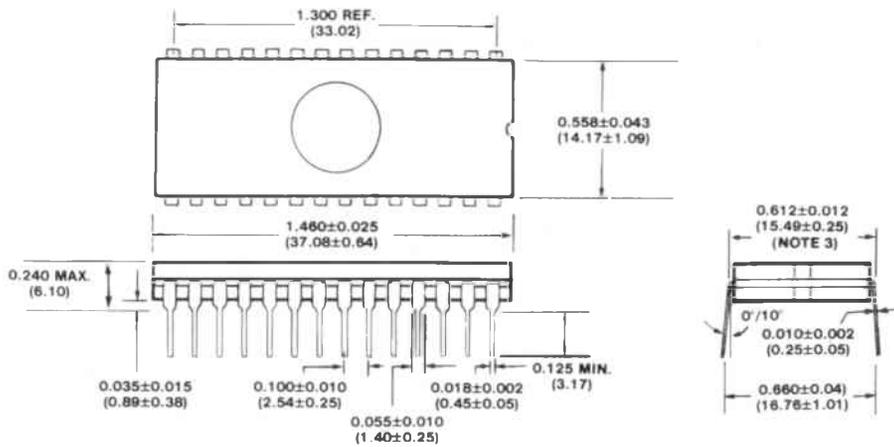


### NOTES

1. All dimensions in inches and (millimeters).
2. For solder dipped leads, thickness will be  $.020$  (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with MIL-M-38510, Appendix C, Dimension E<sub>2</sub> on D outlines which measures from center of shoulder-to-shoulder per section 50c min.  $.590$  (14.99) max.  $.620$  (15.75).

# CERAMIC DUAL-IN-LINE PACKAGES

## 28 LEAD HERMETIC WINDOWED CERAMIC DIP PACKAGE TYPE D

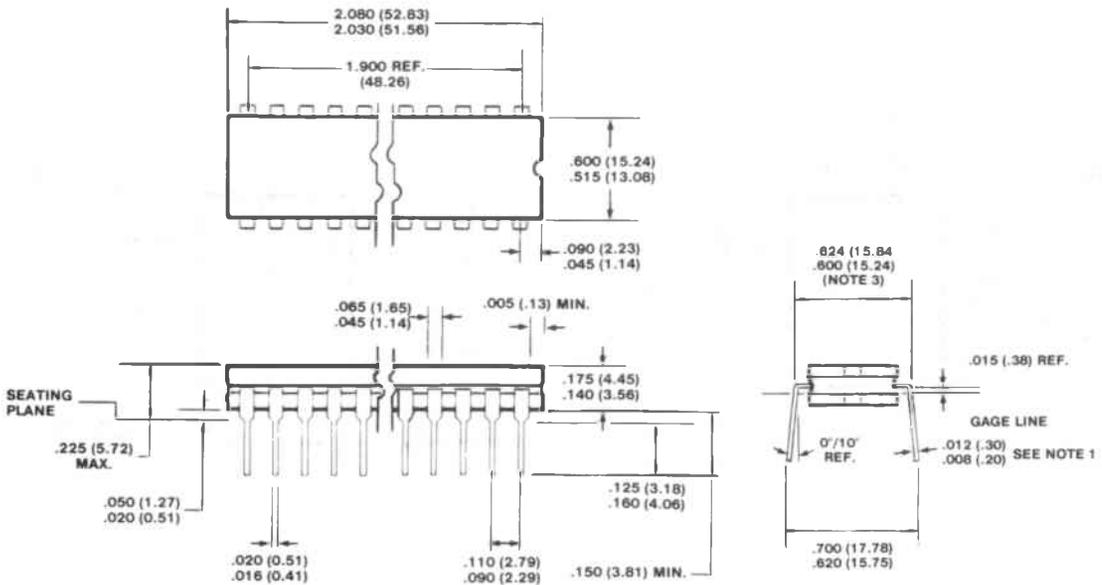


### NOTES

1. All dimensions in inches and (millimeters)
2. For solder dipped leads, thickness will be .020 (.51) max.
3. Dimension is measured from outside shoulder-to-shoulder. This complies with MIL-M-38510, Appendix C, Dimension E<sub>2</sub> on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.98) max. .820 (15.75).

# CERAMIC DUAL-IN-LINE PACKAGES

## 40 LEAD HERMETIC CERAMIC DIP PACKAGE TYPE D

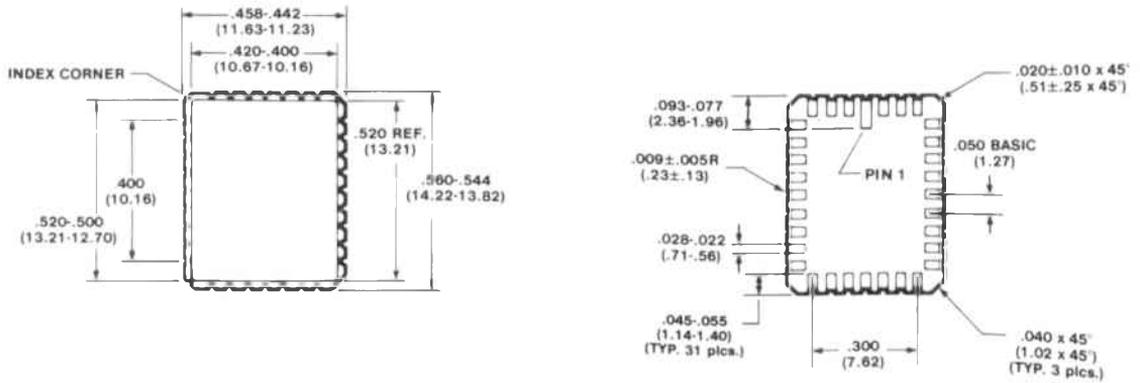


### NOTES

1. For solder dipped leads, thickness will be .020 max.
2. All dimensions in inches and (millimeters).
3. Dimension is measured from outside shoulder to shoulder. This complies with MIL-M-38510, Appendix C, Dimension E<sub>2</sub> on D outlines which measures from center of shoulder-to-shoulder per section 50c min. .590 (14.99) max. .620 (15.75).

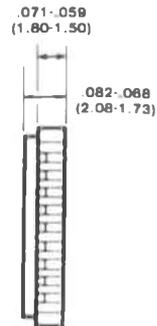
# SURFACE MOUNT PACKAGES

## 32 PIN CERAMIC LEADLESS CHIP CARRIER TYPE L



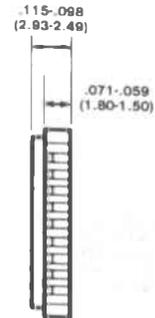
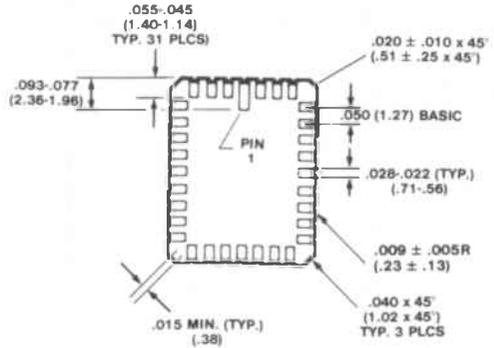
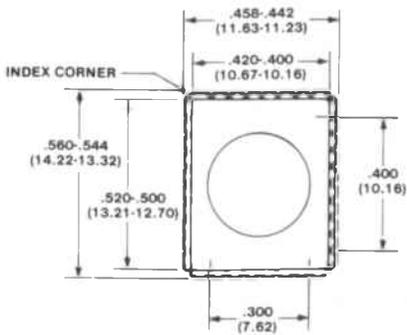
### NOTES

1. All dimensions in inches and (millimeters).
2. All tolerances shall be ± .010 (.25) unless otherwise specified.



# SURFACE MOUNT PACKAGES

## 32 PIN WINDOWED CERAMIC LEADLESS CHIP CARRIER TYPE L

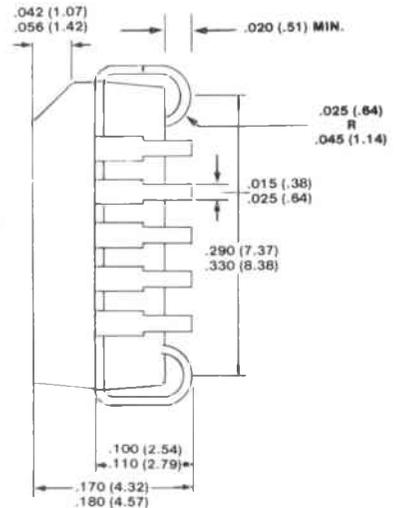
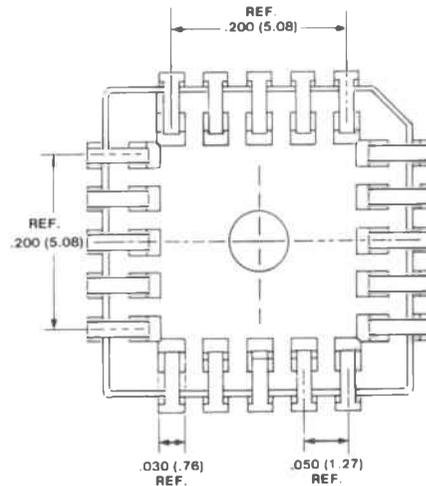
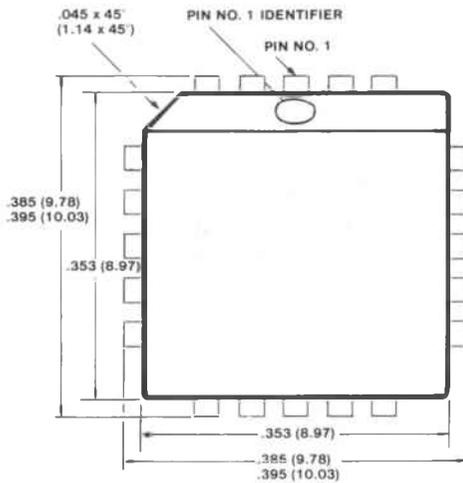


### NOTES

1. All tolerances shall be  $\pm .010$  (.25) unless otherwise specified.
2. All dimensions are in inches and (millimeters).
3. Drawing 295003 forms a part of this drawing.

# SURFACE MOUNT PACKAGES

## 20 PIN PLASTIC LEADED CHIP CARRIER TYPE N

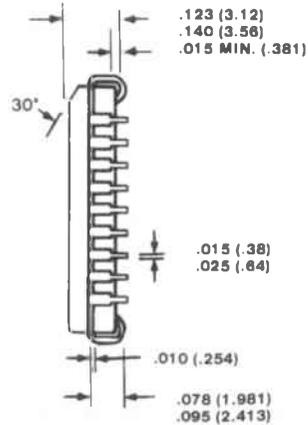
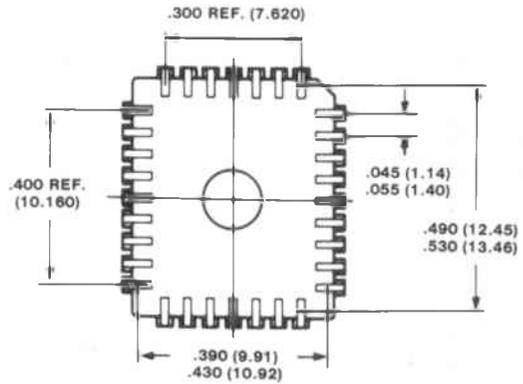
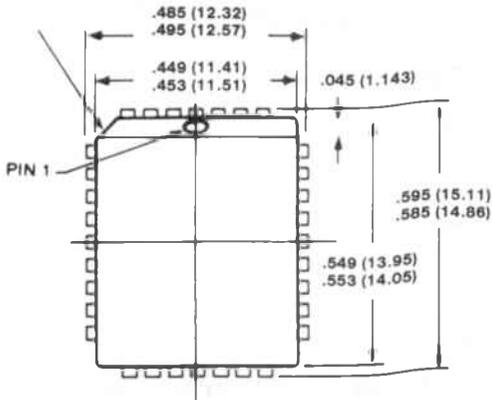


### NOTES

1. All dimensions in inches and (millimeters).
2. All tolerances shall be  $\pm .003$  (.08) unless otherwise specified.
3. Dimensions do not include mold flash. Max allowable flash is .008 (.20).

# SURFACE MOUNT PACKAGES

## 32 PIN PLASTIC LEADLESS CHIP CARRIER TYPE N

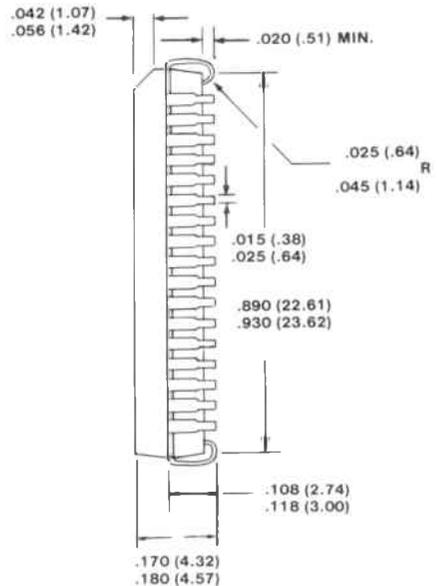
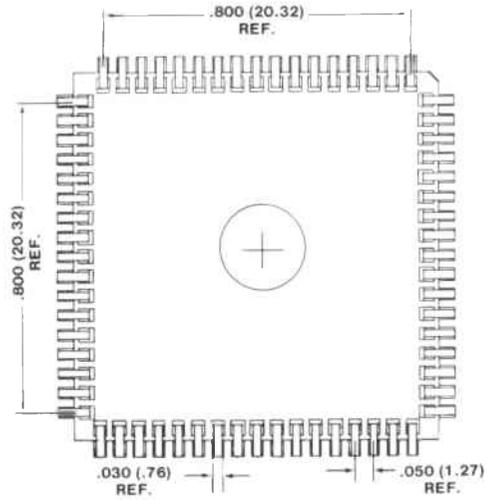
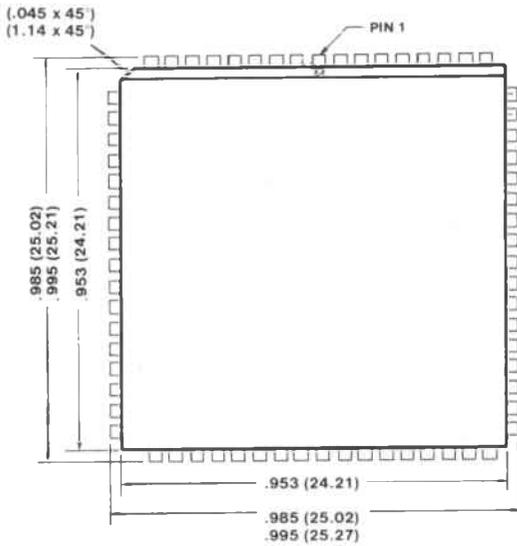


**NOTES**

1. All dimensions in inches and (millimeters).
2. All tolerances shall be  $\pm .003$  (.078) unless otherwise specified.
3. Dimensions do not include mold flash. Max allowable flash is .006 (.20).

# SURFACE MOUNT PACKAGES

## 68 PIN PLASTIC LEADED CHIP CARRIER TYPE N

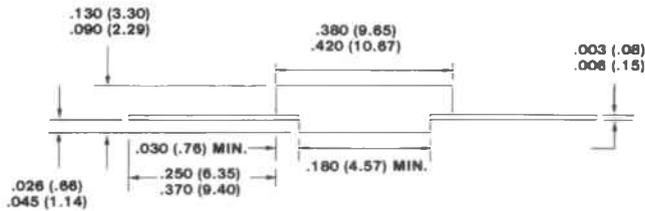
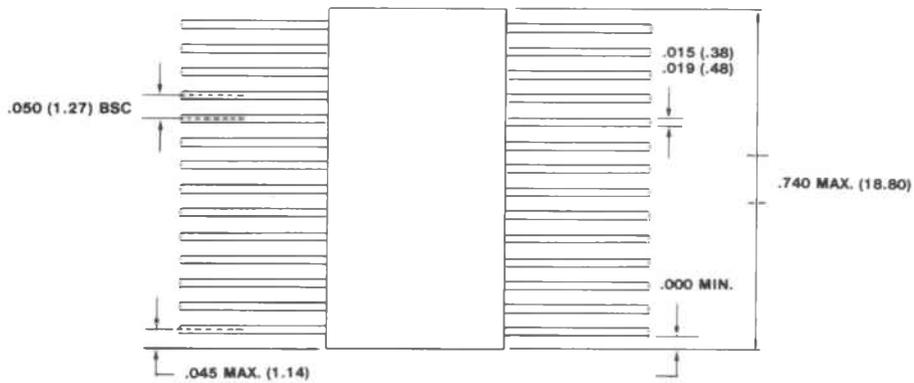


### NOTES

1. All dimensions are in inches and (millimeters).
2. Tolerances are  $\pm .003$  (.08) unless otherwise specified.
3. Dimensions do not include mold flash. Max. allowable flash is  $.008$  (.20).

# SURFACE MOUNT PACKAGES

## 28-LEAD HERMETIC CERAMIC FLATPACK TYPE F



### NOTES

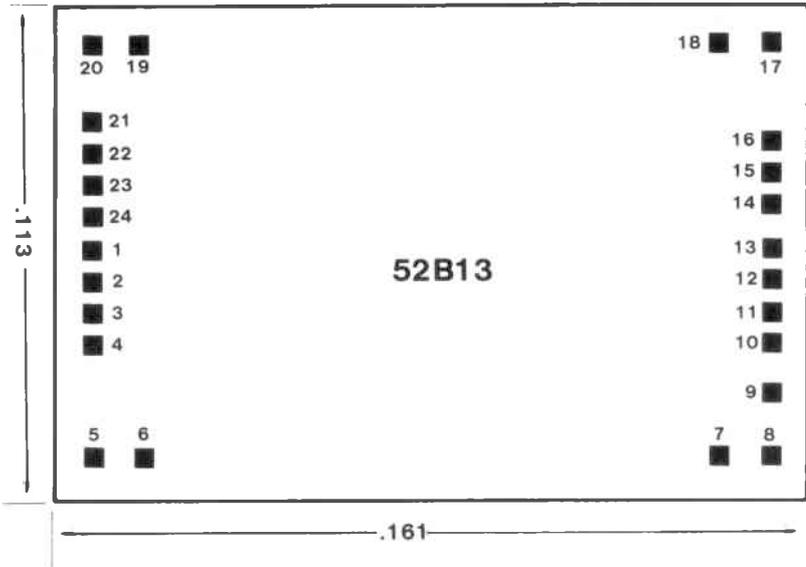
1. All dimensions are in inches and (millimeters).
2. Tolerances are  $\pm .003$  (.078) unless otherwise specified.

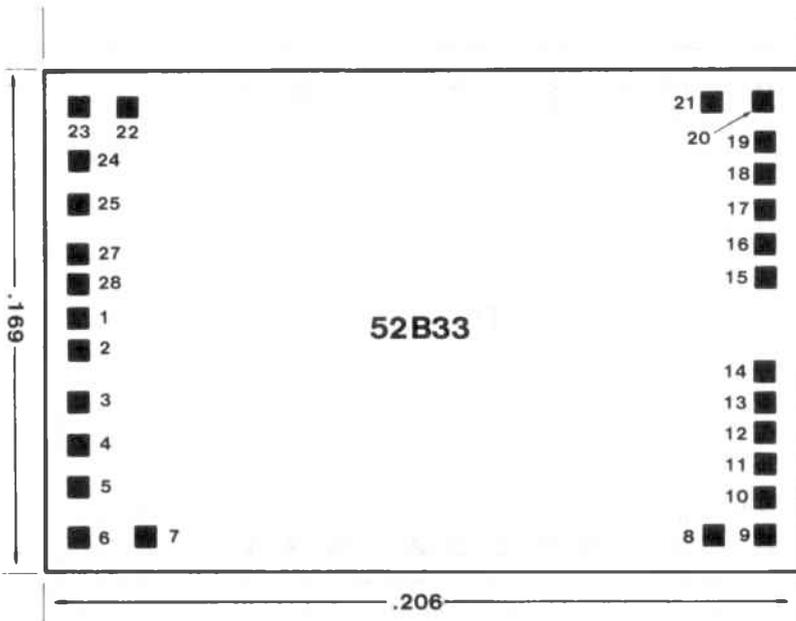


# SEEQ Die Sales

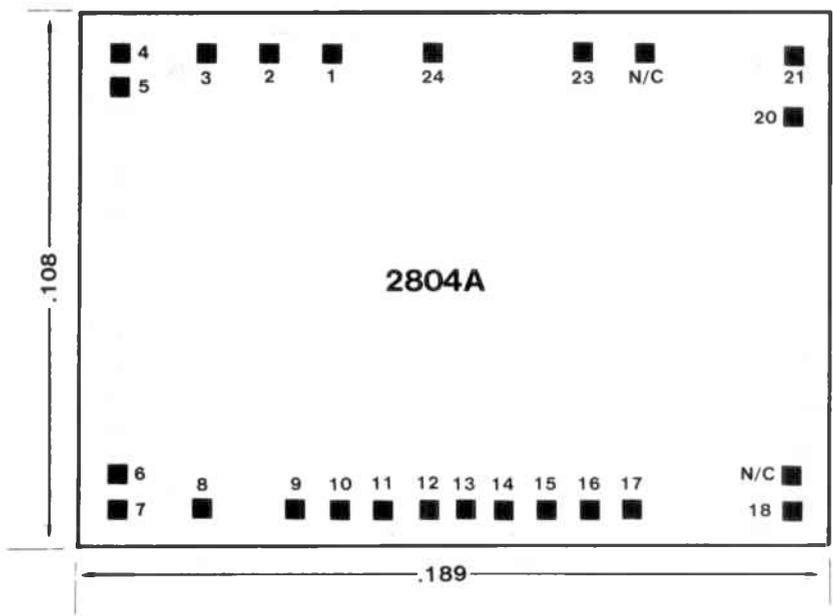
Many of the SEEQ Technology Products contained in this Data Book are available in unencapsulated die form. Products sold in die form have been specifically screened to a special die sales test flow and are ideally suited for hybrid and memory card applications. After screening, all die are optically inspected per method 2010 condition B of MIL-STD 883C. Die are then placed in waffle packs and enclosed in anti-static vacuum sealed bags prior to shipment.

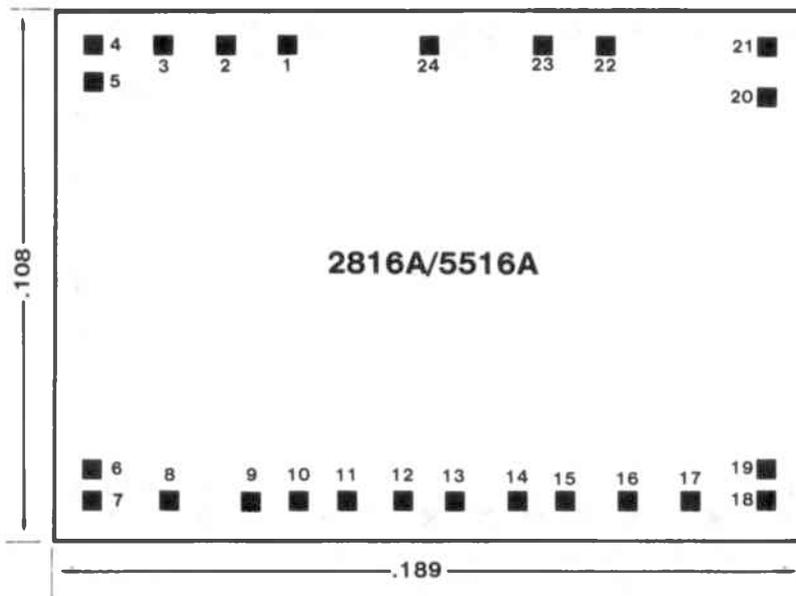
For your reference, the following pages detail product specific bond pad locations and die dimensions for the SEEQ products available in die form. Contact the factory or your local SEEQ representative for additional information.



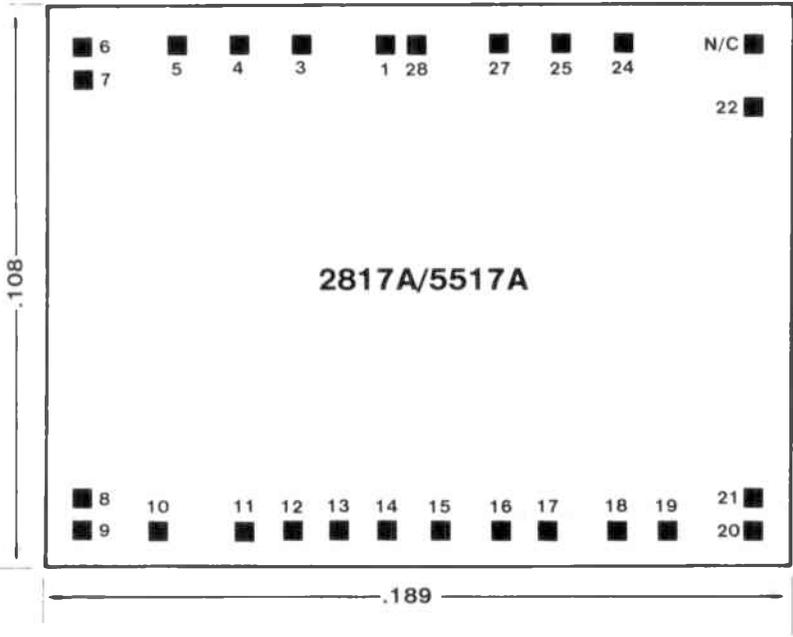


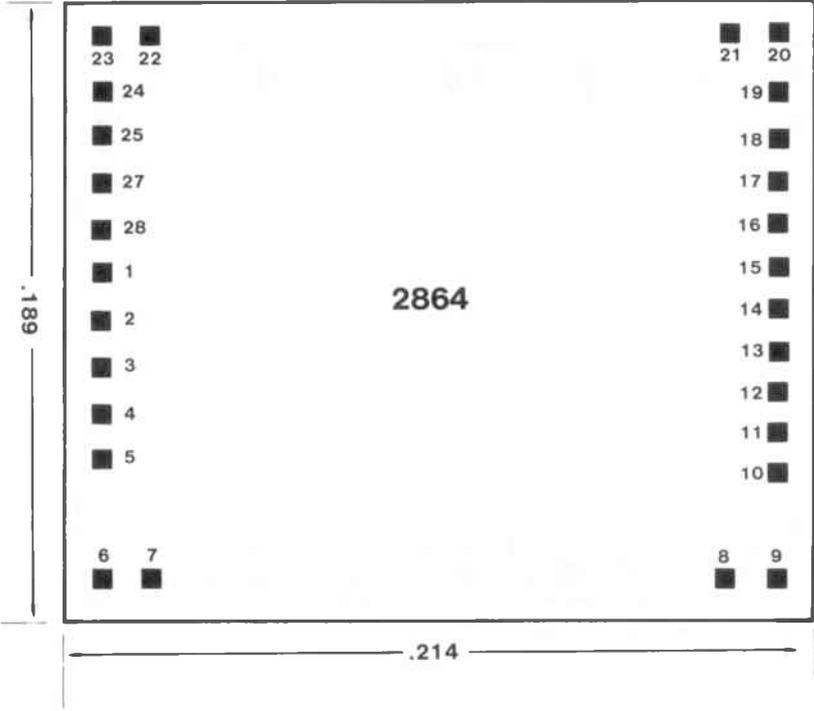
GENERAL  
INFORMATION



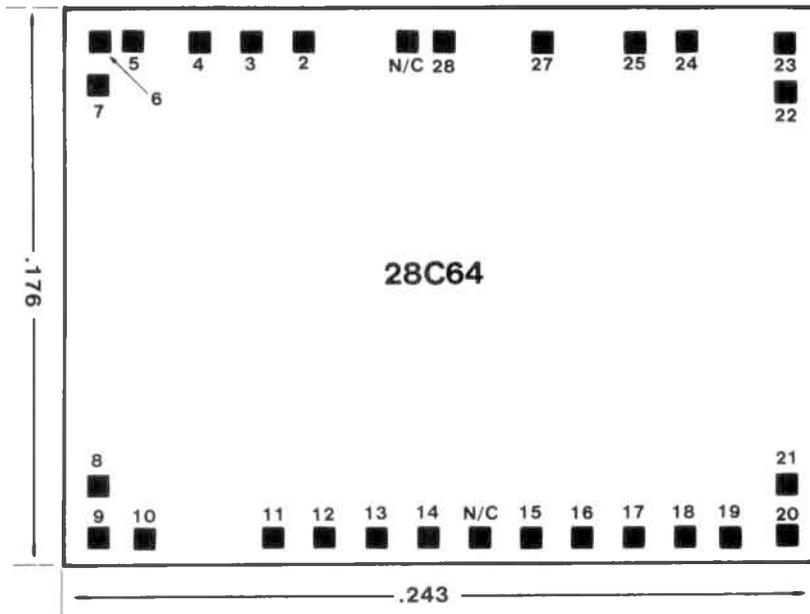


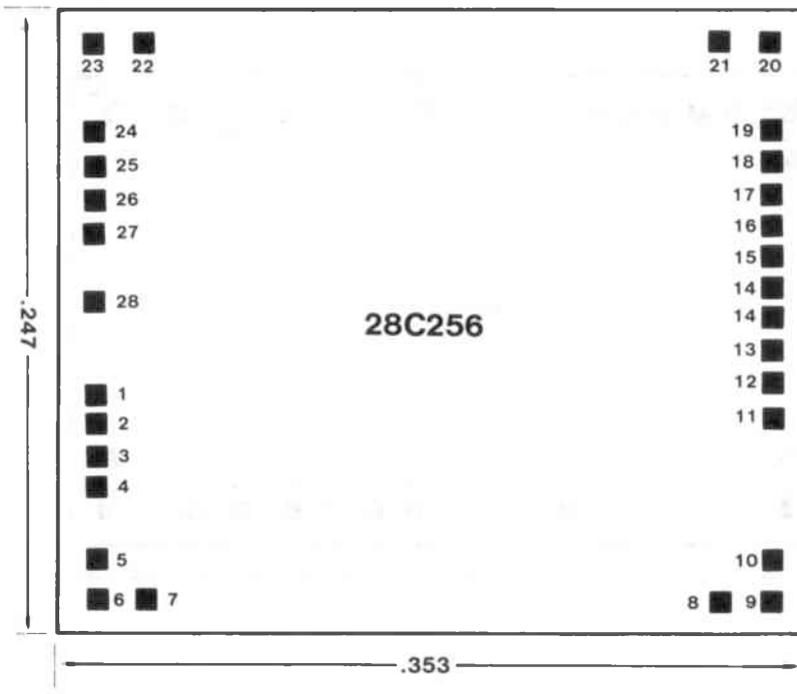
GENERAL  
INFORMATION



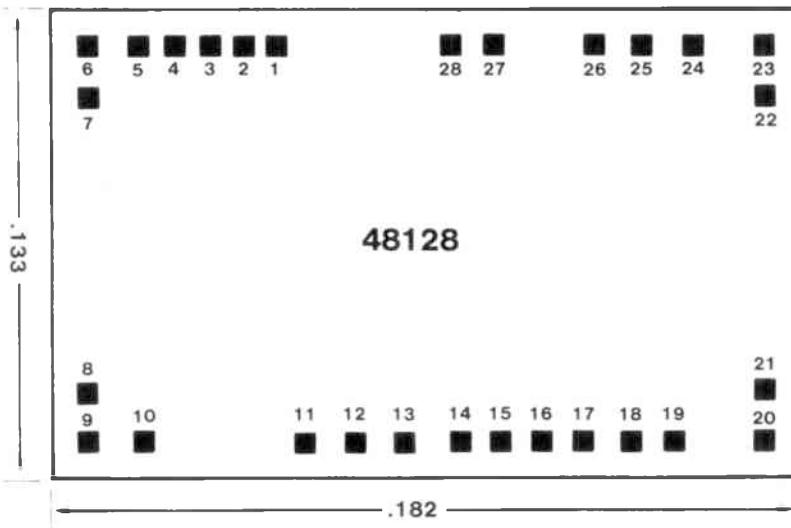


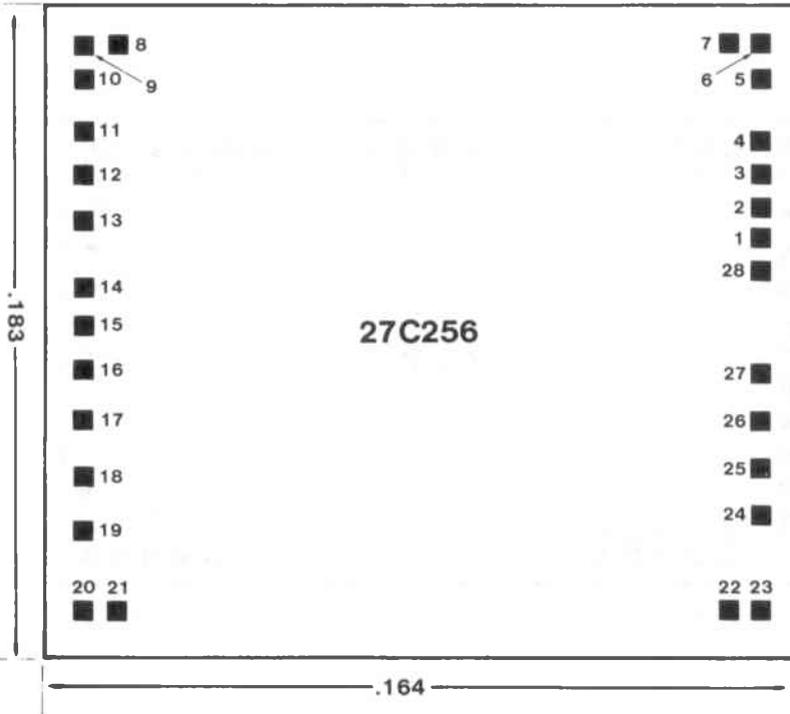
GENERAL  
INFORMATION





GENERAL  
INFORMATION





GENERAL  
INFORMATION



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Western High Tech  
Scottsdale AZ 85258  
(602) 860-2702

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Hadden Assoc.  
San Diego CA  
(619) 565-9444  
Taarcom, Inc.  
Mountain View CA  
(415) 960-1550

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Component Sales  
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Casselberry FL  
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Valentine & Assoc.  
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South Bend IN  
(219) 288-7070

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Grand Rapids MI  
(616) 942-5161

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(612) 646-7217

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Albuquerque NM 87111  
(505) 293-1399

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Rochester NY  
(716) 381-5159  
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Electronic Component Sales  
Tigard OR  
(503) 245-2342

**Pennsylvania**  
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Willow Grove PA  
(215) 657-7250

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Austin, TX  
(512) 835-5822

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Nepean, Ontario  
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Pointe Claire, Quebec  
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(205) 830-1881  
Schweber Elect. Inc.  
Huntsville AL  
(205) 895-0480

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(602) 966-6600  
Schweber Elect. Inc.  
Phoenix AZ  
(602) 997-4874  
Time Electronics  
Tempe AZ  
(602) 967-2000

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(714) 768-4444  
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(408) 432-7171  
Gardena CA  
(213) 327-8409  
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Anaheim CA  
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(818) 998-7200  
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Yorba Linda CA  
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(303) 790-4500

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Englewood CO  
(303) 799-8851

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(203) 748-7080  
Time Electronics  
Cheshire CT  
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Pompano Beach  
(305) 977-7511  
Time Electronics  
Ft. Lauderdale FL  
(305) 974-4800  
Orlando FL  
(305) 841-6565  
Zeus Components  
Oviedo FL  
(305) 365-3000

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Norcross GA  
(404) 449-9170  
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Norcross GA  
(404) 448-4448

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Elk Grove IL  
(312) 364-3750  
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Wood Dale IL  
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Overland Park KS  
(913) 492-2921

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Gaithersburg MD  
(301) 840-5900  
Time Electronics  
Columbia MD  
(301) 964-3090

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(617) 657-5170  
Schweber Elect., Inc.  
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(617) 275-5100  
Time Electronics  
Peabody MA  
(617) 532-6200  
Zeus Components  
Lexington MA  
(617) 863-8800

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Livonia MI  
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(612) 780-9123  
Schweber Elect., Inc.  
Edina MN  
(612) 941-5280  
Time Electronics  
Bloomington MN  
(612) 944-9192

### Missouri

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Earth City MO  
(314) 739-0526  
Time Electronics  
St. Louis MO  
(314) 391-6444

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Schweber Elect., Inc.  
Manchester NH  
(603) 625-2250

### New Jersey

Lionex  
Fairfield NJ  
(201) 227-7960  
Schweber Elect., Inc.  
Fairfield NJ  
(201) 227-7800  
Time Electronics  
Pinebrook NJ  
(201) 882-4611

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(516) 273-1660  
Schweber Elect., Inc.  
Rochester NY  
(716) 424-2222  
Westbury NY  
(516) 334-7474

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E. Syracuse NY  
(315) 432-0355  
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Schweber Elect., Inc.  
Raleigh NC  
(919) 867-0000

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Schweber Elect., Inc.  
Beachwood OH  
(216) 464-2970  
Dayton OH  
(513) 439-1800  
Time Electronics  
Dublin OH  
(614) 761-1100  
Zeus Components  
Dayton OH  
(513) 454-1225

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(918) 664-8812  
Schweber Elect., Inc.  
Tulsa OK  
(918) 622-8000

### Oregon

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Time Electronics  
Portland OR  
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Pittsburgh PA  
(412) 982-1600  
Time Electronics  
King of Prussia PA  
(215) 337-0900

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Austin TX  
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Sugarland TX  
(713) 240-2255  
Schweber Elect., Inc.  
Austin TX  
(512) 458-8253  
Dallas TX  
(214) 661-5010  
Houston TX  
(713) 784-3600  
Time Electronics  
Austin TX  
(512) 339-3051  
Carrollton TX  
(214) 241-7441  
Houston TX  
(713) 530-0800  
Zeus Components  
Richardson TX  
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Time Electronics  
Salt Lake City  
(801) 973-8181

### Washington

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(206) 881-0850  
Bellevue WA  
(206) 747-1515  
Time Electronics  
Redmond WA  
(206) 882-1600

### Wisconsin

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New Berlin WI  
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Future Electronics  
Edmonton, Alberta  
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Vancouver,  
British Columbia  
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Downsview, Ontario  
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Ottawa, Ontario  
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(514) 694-7710

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### Australia

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Sydney  
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St. Leonards  
Tel: (02) 439 7599  
Austimmer  
Tel: (02) 232 6933  
Perth  
Tel: (09) 470 2702

### Austria

Sieg-Electronic  
Vienna  
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### Brazil

Hitech  
Sao Paulo  
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### Denmark

Exatec A.S.  
Copenhagen  
Tel: 45 1 19 1022  
Farsoe  
Tel: 45 8 63 3311

### Finland

ITT Disti.  
Helsinki  
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### Federal Republic of Germany

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Kaltenkirchen  
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Dacom Elektronik  
Vertreibe GmbH  
Stuttgart  
Tel: 49 (711) 74 10 21  
Munche  
Tel: 49 (89) 60 98 031

### Federal Republic of Germany (cont.)

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Dusseldorf  
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Metronik GmbH  
Munche  
Tel: 49 (89) 611 080  
Stuttgart  
Tel: 49 (711) 76 40 33  
Hamburg  
Tel: 49 (40) 830 40 61

### France

Radio Television  
Francaise (RTF)  
Gentilly  
Tel: 33 (1) 46 64 11 01  
RepTronic  
Paris  
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### Hong Kong

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Kowloon  
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### India

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Kadcom  
Bangalore  
Tel: 365 648

### Israel

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### Italy

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Rome  
Tel: 39 (6) 84.50.117  
Eledra  
Tel: 39 (2) 81.82.1

### Japan

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Corporation (JMC)  
Kawasaki-City  
Tel (0/44) 711 0022  
Japan Macnics  
Corporation (JMC)  
Osaka City  
Tel: (0/6) 325-0880

### Korea

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Seoul  
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### The Netherlands

Techmation  
Electronics B.V.  
Haafden  
Tel: 31 (4189) 2222

### New Zealand

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Tel: 600 760

### Norway

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Fjellhamar  
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### Peoples Republic of China

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Tel: 81-5728  
Hong Kong  
Tel: 0-4161384

### South Africa

Advanced Semiconductor  
Devices (PTY) Ltd.  
Sandton  
Tel: (011) 802-5820

### Singapore/Malaysia

Desner Electronics  
(Far East) PTE Ltd.  
Singapore  
Tel: 3373188

### Spain

Semiconductores  
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ITT Multikomponent, AB  
Solna  
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Switzerland  
Anatec AG Electronische  
Bauteile  
Zug  
Tel: 41 (42) 31 54 77

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Pronto Electronic  
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Gants Hills/Essex  
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ITT Multicomponents  
Slough, Berkshire  
Tel: (0753) 824 212





